Data Sheet June 10, 2010 FN9213.2

5-Bit VID Single-Phase Voltage Regulator for IMVP-6+ Santa Rosa GPU Core

The ISL6263 IC is a Single-Phase Synchronous-Buck PWM voltage regulator featuring Intersil's Robust Ripple Regulator (R^3) Technology™. The ISL6263 is an implementation of the Intel® Mobile Voltage Positioning (IMVP) protocol for GPU Render Engine core power. Integrated MOSFET drivers, bootstrap diode, and droop amplifier result in lower component cost and smaller implementation area.

Intersil's R^3 Technology™ combines the best features of both fixed-frequency PWM and hysteretic PWM, delivering excellent light-load efficiency and superior load transient response by commanding variable switching frequency during the transitory event.

To maximize light load efficiency, the ISL6263 automatically transitions between continuous-conduction-mode (CCM) and discontinuous-conduction-mode (DCM.) During DCM the low-side MOSFET enters diode-emulation-mode (DEM.) DEM is enabled whenever a Render Suspend state has been set on the VID inputs. Optionally, DEM can be enabled for all VID states by setting the FDE pin high. The ISL6263 has an audio filter that can be enabled in any Render Suspend state by pulling the AF_EN pin high. The audio filter prevents the PWM switching frequency from entering the audible spectrum due to extremely light load while in DEM.

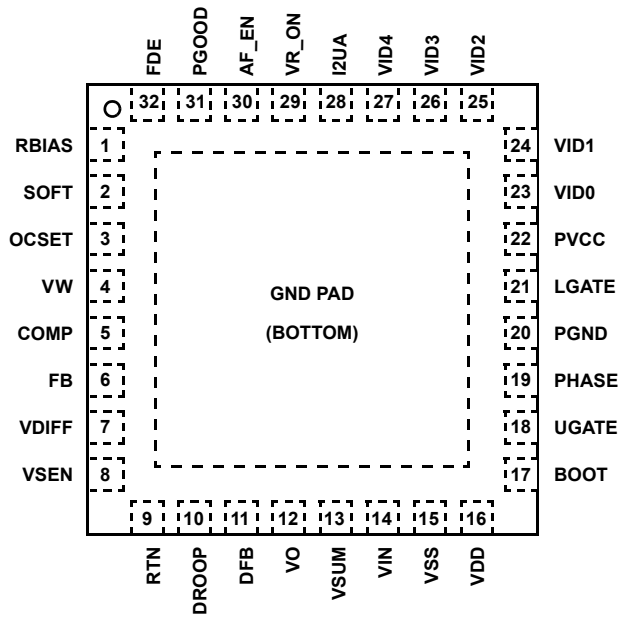
The Render core voltage can be dynamically programmed from 0.41200V to 1.28750V by the five VID input pins without requiring sequential stepping of the VID states. The ISL6263 uses the same capacitor for the soft-start slew-rate and for the dynamic VID slew-rate by internally connecting the SOFT pin to the appropriate current source. Processor socket Kelvin sensing is accomplished with an integrated unity-gain true differential amplifier.

Features

- Precision single-phase core voltage regulator
  - 0.5% system accuracy 0°C to +100°C
  - Differential remote GPU die voltage sensing
  - Differential droop voltage sensing
- Applications up to 25A
- Input voltage range: +5.0V to +25.0V
- Programmable PWM frequency: 200kHz to 500kHz
- Pre-biased output start-up capability
- 5-bit voltage identification input (VID)
  - 1.28750 to 0.41200V
  - 25.75mV steps
  - Sequential or non-sequential VID change on-the-fly
- Selectable diode emulation mode
  - Render Suspend mode only
  - Render Performance and Render Suspend mode
- Selectable audio filter in render suspend mode
- Integrated MOSFET drivers and bootstrap diode
- Choice of current sensing schemes
  - Lossless inductor DCR current sensing
  - Precision resistive current sensing
- Overvoltage, undervoltage, and overcurrent protection
- Pb-free plus anneal available (RoHS compliant)

Pinout

ISL6263 (32 LD 5x5 QFN)
TOP VIEW



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6263CRZ	ISL 6263CRZ	-10 to 100	32 Ld 5x5 QFN	L32.5x5
ISL6263CRZ-T (Note 1)	ISL 6263CRZ	-10 to 100	32 Ld 5x5 QFN Tape & Reel	L32.5x5

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6263. For more information on MSL please see techbrief TB363.

Block Diagram

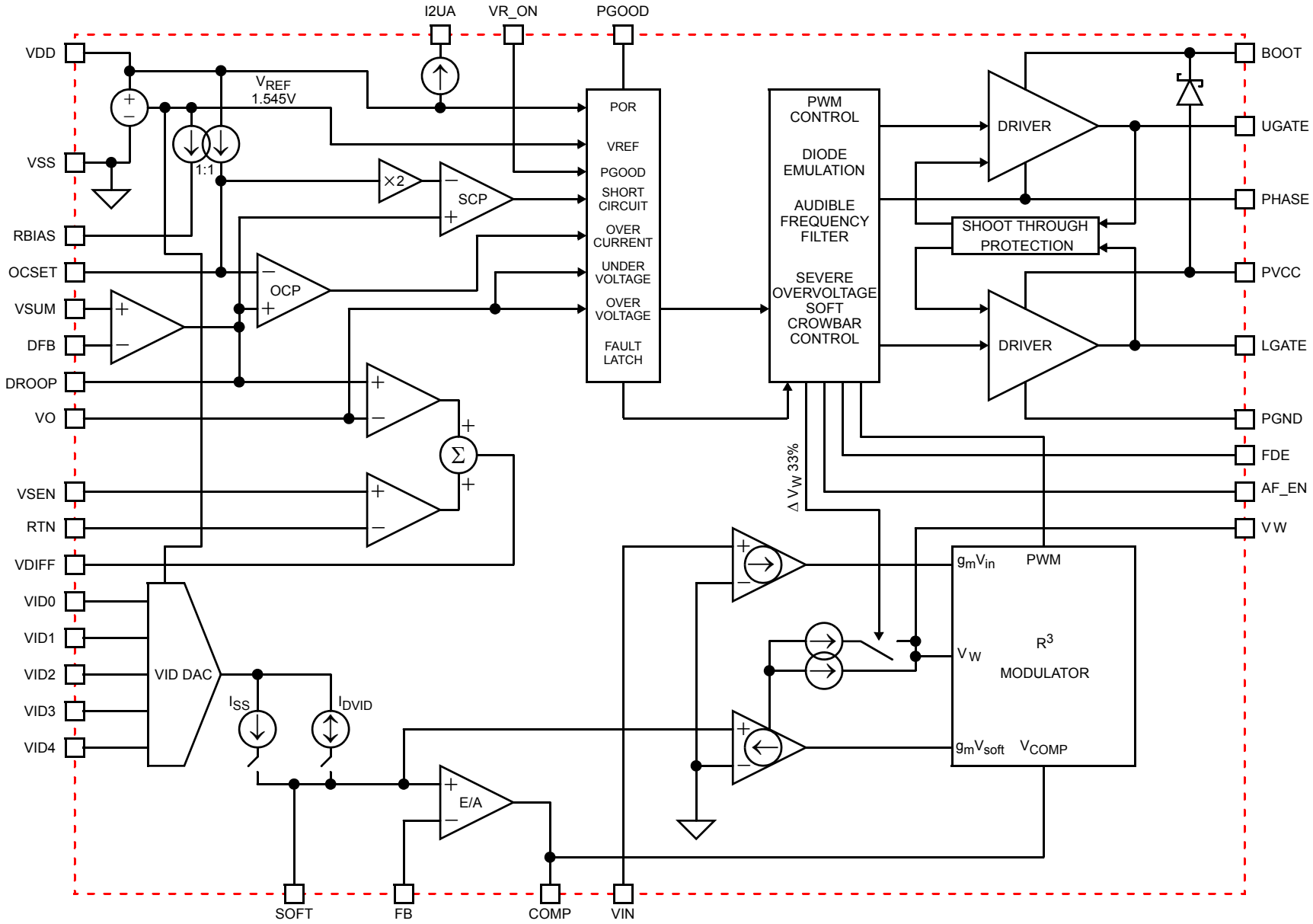


FIGURE 1. SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM OF THE ISL6263

Simplified Application Circuit for DCR Current Sensing

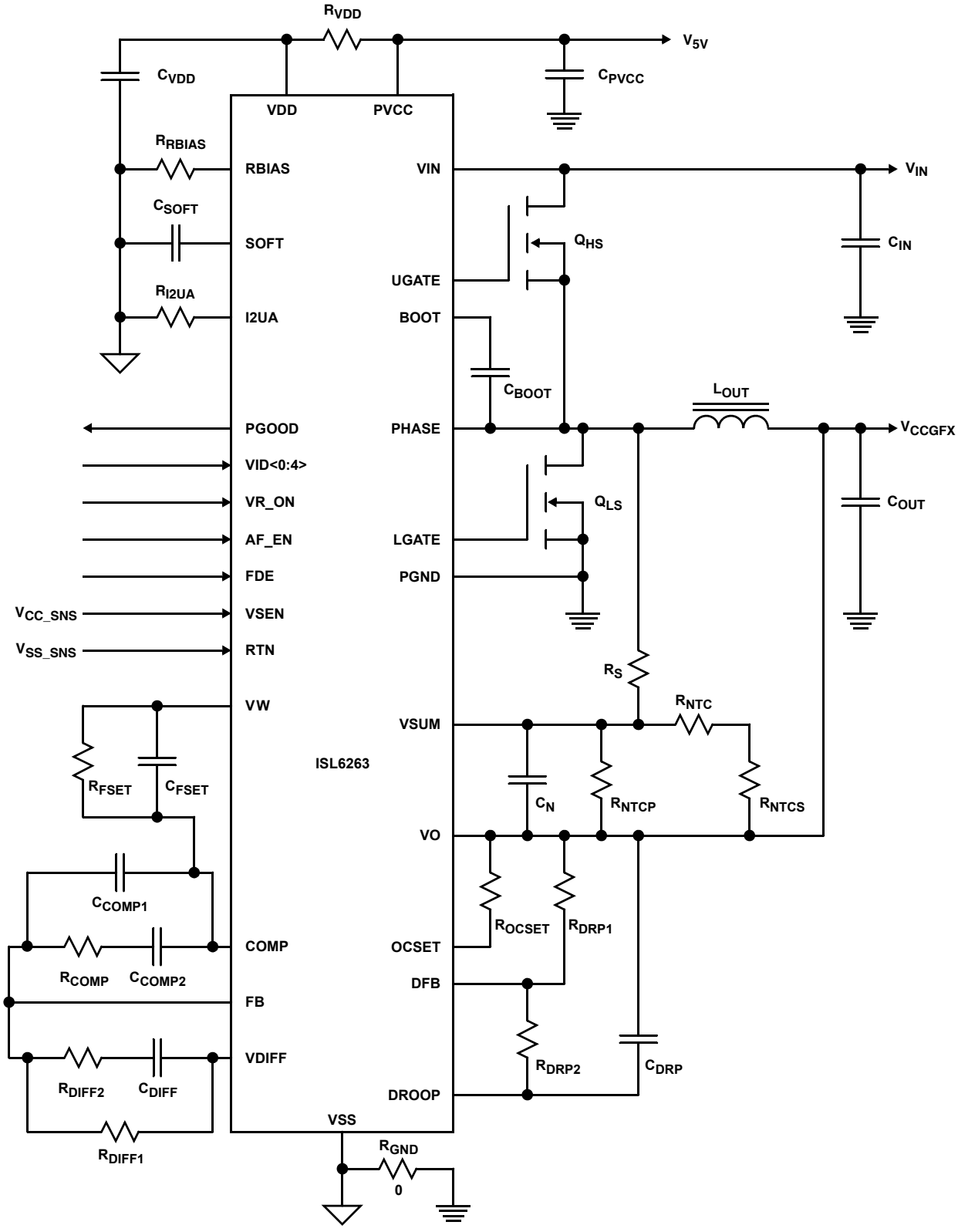


FIGURE 2. ISL6263 GPU RENDER-CORE VOLTAGE REGULATOR SOLUTION WITH DCR CURRENT SENSING

Simplified Application Circuit for Resistive Current Sensing

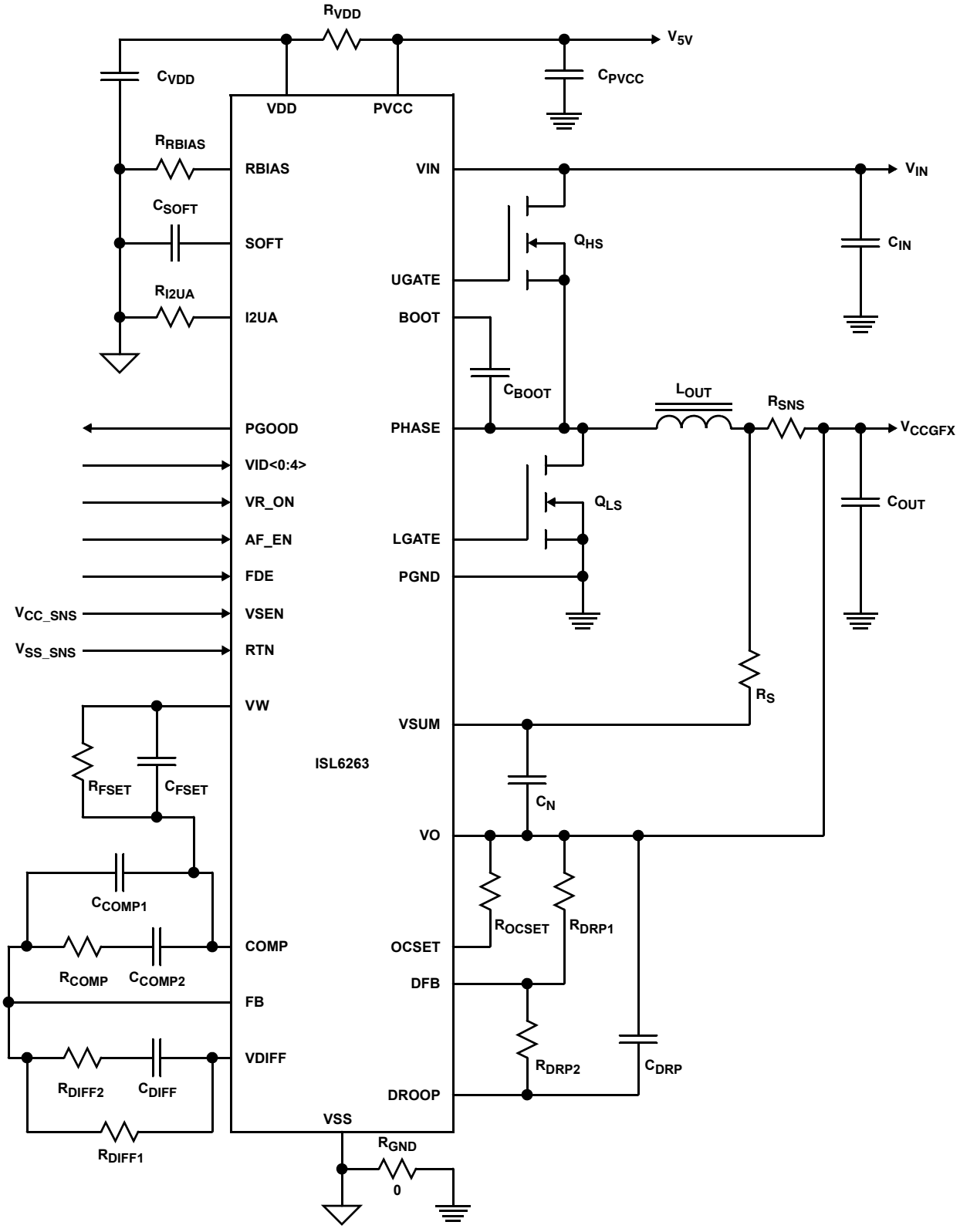


FIGURE 3. ISL6263 GPU RENDER-CORE VOLTAGE REGULATOR SOLUTION WITH RESISTIVE CURRENT SENSING

Absolute Voltage Ratings

VIN to VSS . . . . . -0.3V to +28V
VDD to VSS . . . . . -0.3V to +7.0V
PVCC to PGND . . . . . -0.3V to +7.0V
VSS to PGND . . . . . -0.3V to +0.3V
PHASE to VSS. . . . . (DC) -0.3V to +28V
(<100ns Pulse Width, 10µJ) -5.0V
BOOT to PHASE . . . . . -0.3V to +7.0V
BOOT to VSS or PGND . . . . . -0.3V to +33V
UGATE. . . . . (DC) -0.3V to PHASE, BOOT +0.3V
(<200ns Pulse Width, 20µJ) -4.0V
LGATE . . . . . (DC) -0.3V to PGND, PVCC +0.3V
(<100ns Pulse Width, 4µJ) -2.0V
ALL Other Pins. . . . . -0.3V to VSS, VDD +0.3V

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package.	35	6

Junction Temperature Range. . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range. . . . . -10°C to 100°C
VIN to VSS. . . . . +5V to +25V
VDD to VSS . . . . . +5V ±5%
PVCC to PGND . . . . . +5V ±5%
FDE to VSS . . . . . 0V to +3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VDD = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VIN						
VIN Input Resistance	R_{VIN}	VR_ON = 3.3V	-	1.0	-	MΩ
VIN Shutdown Current	I_{VIN_SHDN}	VR_ON = 0V, VIN = 25V	-	-	**1.0**	µA
VDD and PVCC						
VDD Input Bias Current	I_{VDD}	VR_ON = 3.3V	-	2.4	**3.0**	mA
VDD Shutdown Current	I_{VDD_SHDN}	VR_ON = 0V, VDD = 5.0V	-	-	**1.0**	µA
VDD POR THRESHOLD						
Rising VDD POR Threshold Voltage	V_{VDD_THR}		-	4.35	**4.50**	V
Falling VDD POR Threshold Voltage	V_{VDD_THF}		**3.85**	4.10	-	V
REGULATION						
Output Voltage Range	V_{GFX_MAX}	VID<4:0> = 00000	-	1.28750	-	V
	V_{GFX_MIN}	VID<4:0> = 11111	-	0.41200	-	V
VID Voltage Step		VID<4:0> = 00000 to 11110 (1.28750V to 0.51500V)	-	25.75	-	mV/step
		VID<4:0> = 11110 to 11111 (0.51500V to 0.41200V)	-	103	-	mV
System Accuracy		VID = 1.28750V to 0.74675V T_A = 0°C to +100°C	**-0.5**	-	**0.5**	%
		VID = 0.72100V to 0.51500V T_A = 0°C to +100°C	**-1.0**	-	**1.0**	%
		VID = 0.41200 T_A = 0°C to +100°C	**-2.0**	-	**2.0**	%
PWM						
Nominal Frequency	F_{SW}	R_{FSET} = 7kΩ, V_{COMP} = 2V	**318**	333	**348**	kHz

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VDD = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Frequency Range			**200**	-	**500**	kHz
AMPLIFIERS						
Error Amplifier DC Gain (Note 8)	A_{V0}		-	90	-	dB
Error Amplifier Gain-Bandwidth Product (Note 8)	GBW	C_L = 20pF	-	18	-	MHz
Error Amp Slew Rate (Note 8)	SR	C_L = 20pF	-	5	-	V/µs
FB Input Bias Current	I_{FB}	V_{FB} = 1.28750V	-	10	**150**	nA
Droop Amplifier Offset	V_{DROOP_OFS}		**-0.3**	-	**0.3**	mV
RBIAS Voltage	V_{RBIAS}	R_{RBIAS} = 150kΩ	**1.50**	1.52	**1.54**	V
I2UA Reference Current	I_{I2UA}	V_{I2UA} = 2.5V	**1.85**	2.00	**2.15**	µA
SOFT-START CURRENT						
Soft-Start Current	I_{SS}		**-46**	-41	**-36**	µA
Soft Dynamic VID Current	I_{DVID}	|SOFT - REF|>100mV	**±175**	±200	**±225**	µA
GATE DRIVER						
UGATE Source Resistance	R_{UGSRC}	500mA Source Current	-	1.0	**1.5**	Ω
UGATE Source Current (Note 7)	I_{UGSRC}	V_{UGATE_PHASE} = 2.5V	-	2.0	**-**	A
UGATE Sink Resistance	R_{UGSNK}	500mA Sink Current	-	1.0	**1.5**	Ω
UGATE Sink Current (Note 7)	I_{UGSNK}	V_{UGATE_PHASE} = 2.5V	-	2.0	**-**	A
LGATE Source Resistance	R_{LGSRC}	500mA Source Current	-	1.0	**1.5**	Ω
LGATE Source Current (Note 7)	I_{LGSRC}	V_{LGATE_PGND} = 2.5V	-	2.0	**-**	A
LGATE Sink Resistance	R_{LGSNK}	500mA Sink Current	-	0.5	**0.9**	Ω
LGATE Sink Current (Note 7)	I_{LGSNK}	V_{LGATE_PGND} = 2.5V	-	4.0	**-**	A
UGATE Pull-Down Resistor (Note 7)	R_{PD}		-	1.1	**-**	kΩ
UGATE Turn-On Propagation Delay	t_{PDRU}	PV_{CC} = 5V, UGATE open	**20**	30	**44**	ns
LGATE Turn-On Propagation Delay	t_{PDRL}	PV_{CC} = 5V, LGATE open	**7**	15	**30**	ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 10mA	**0.56**	0.69	**0.76**	V
Reverse Leakage	I_R	V_R = 16V	-	-	**5.0**	µA
POWER GOOD and PROTECTION MONITOR						
PGOOD Low Voltage	V_{PGOOD}	I_{PGOOD} = 4mA	-	0.11	0.40	V
PGOOD Leakage Current	I_{PGOOD}	V_{PGOOD} = 3.3V	**-1.0**	-	**1.0**	µA
Overvoltage Threshold (VO - VSOFT)	V_{OVP}	V_O rising above V_{SOFT} > 1ms	**160**	200	**240**	mV
Severe Overvoltage Threshold	V_{OVPS}	V_O rising above 1.55V reference > 0.5µs	**1.525**	1.550	**1.575**	V
OCSET Reference Current	I_{OCSET}	R_{RBIAS} = 150kΩ	**9.9**	10.1	**10.3**	µA
OCSET Voltage Threshold Offset	V_{OCSET_OFS}	V_{DROOP} rising above V_{OCSET} > 120µs	**-3**	-	**3**	mV
Undervoltage Threshold (VSOFT - VO)	V_{UVF}	V_O falling below V_{SOFT} for > 1ms	**-360**	-300	**-240**	mV
CONTROL INPUTS						
VR_ON Input Low	V_{VR_ONL}		-	-	**1**	V

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise stated. All typical specifications T_A = +25°C, VDD = 5V, PVCC = 5V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VR_ON Input High	V_{VR_ONH}		**2.3**	-	**-**	V
AF_EN Input Low	V_{AF_ENL}		**-**	-	**1**	V
AF_EN Input High	V_{AF_ENH}		**2.3**	-	**-**	V
VR_ON Leakage	I_{VR_ONL}	V_{VR_ON} = 0V	**-1.0**	0	**-**	µA
	I_{VR_ONH}	V_{VR_ON} = 3.3V	**-**	0	**1.0**	µA
AF_EN Leakage	I_{AF_ENL}	V_{AF_EN} = 0V	**-1.0**	0	**-**	µA
	I_{AF_ENH}	V_{AF_EN} = 3.3V	**-**	0.45	**1.0**	µA
VID<4:0> Input Low	V_{VIDL}		**-**	-	**0.3**	V
VID<4:0> Input High	V_{VIDH}		**0.7**	-	**-**	V
FDE Input Low	V_{FDEL}		**-**	-	**0.3**	V
FDE Input High	V_{FDEH}		**0.7**	-	**-**	V
VID<4:0> Leakage	I_{VIDL}	V_{VID} = 0V	**-1.0**	0	**-**	µA
	I_{VIDH}	V_{VID} = 1.0V	**-**	0.45	**1.0**	µA
FDE Leakage	I_{FDEL}	V_{FDE} = 0V	**-1.0**	0	**-**	µA
	I_{FDEH}	V_{FDE} = 1.0V	-	0.45	**1.0**	µA

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.
8. Limits should be considered typical and are not production tested.

Functional Pin Descriptions

RBIAS (Pin 1) - Sets the internal 10µA current reference. Connect a 150kΩ ±1% resistor from RBIAS to VSS.

SOFT (Pin 2) - Sets the output voltage slew-rate. Connect an X5R or X7R ceramic capacitor from SOFT to VSS. The SOFT pin is the non-inverting input of the error amplifier.

OCSET (Pin 3) - Sets the overcurrent threshold. Connect a resistor from OCSET to VO.

VW (Pin 4) - Sets the static PWM switching frequency in continuous conduction mode. Connect a resistor from VW to COMP.

COMP (Pin 5) - Connects to the output of the control loop error amplifier.

FB (Pin 6) - Connects to the inverting input of the control loop error amplifier.

VDIFF (Pin 7) - Connects to the output of the VDIFF differential-summing amplifier.

VSEN (Pin 8) - This is the V_{CC_SNS} input of the processor socket Kelvin connection. Connects internally to one of two non-inverting inputs of the VDIFF differential-summing amplifier.

RTN (Pin 9) - This is the V_{SS_SNS} input of the processor socket Kelvin connection. Connects internally to one of two inverting inputs of the VDIFF differential-summing amplifier.

DROOP (Pin 10) - Connects to the output of the droop differential amplifier and to one of two non-inverting inputs of the VDIFF differential-summing amplifier.

DFB (Pin 11) - This is the feedback of the droop amplifier. Connects internally to the inverting input of the droop differential amplifier.

VO (Pin 12) - Connects to one of two inverting inputs of the VDIFF differential-summing amplifier.

VSUM (Pin 13) - Connects to the non-inverting input of the droop differential amplifier.

VIN (Pin 14) - Connects to the R^3 PWM modulator providing input voltage feed-forward. For optimum input voltage transient response, connect near the drain of the high-side MOSFETs.

VSS (Pin 15) - Analog ground.

VDD (Pin 16) - Input power supply for the IC. Connect to +5VDC and decouple with at least a 1µF MLCC capacitor from the VDD pin to the VSS pin.

BOOT (Pin 17) - Input power supply for the high-side MOSFET gate driver. Connect an MLCC bootstrap capacitor from the BOOT pin to the PHASE pin.

UGATE (Pin 18) - High-side MOSFET gate driver output. Connect to the gate of the high-side MOSFET.

PHASE (Pin 19) - Current return path for the UGATE high-side MOSFET gate driver. Detects the polarity of the PHASE node voltage for diode emulation. Connect the PHASE pin to the drains of the low-side MOSFETs.

PGND (Pin 20) - Current return path for the LGATE low-side MOSFET gate driver. The PGND pin only conducts current when LGATE pulls down. Connect the PGND pin to the sources of the low-side MOSFETs.

LGATE (Pin 21) - Low-side MOSFET gate driver output. Connect to the gate of the low-side MOSFET.

PVCC (Pin 22) - Input power supply for the low-side MOSFET gate driver, and the high-side MOSFET gate driver, via the internal bootstrap diode connected between the PVCC and BOOT pins. Connect to +5VDC and decouple with at least 1µF of an MLCC capacitor from the PVCC pin to the PGND pin.

VID0:VID4 (Pin 23:Pin 27) - Voltage identification inputs. VID0 input is the least significant bit (LSB) and VID4 input is the most significant bit (MSB).

I2UA (Pin 28) - Output of an internal 2µA current source. Connect a 20kΩ resistor from the I2UA pin to the VSS pin.

VR_ON (Pin 29) - A high logic signal on this pin enables the converter and a low logic signal disables the converter.

AF_EN (Pin 30) - A high logic signal on this pin enables the audible frequency filter. A low logic signal on this pin disables the audible frequency filter and improves the converter efficiency.

PGOOD (Pin 31) - The PGOOD pin is an open-drain output that indicates when the converter is able to supply regulated voltage. Connect the PGOOD pin to a maximum of 5V through a pull-up resistor.

FDE (Pin 32) - A low logic state on this pin confines the availability of diode emulation mode to Render Suspend VID states only. A high logic state on this pin enables diode emulation for all VID states.

TABLE 1. FDE AND AF_EN STATE TABLE

RENDER MODE	FDE	AF_EN	PWM MODE	ΔV_W	AUDIO FILTER
PERFORMANCE	0	0	CCM	x	x
	1	0	CCM/DCM	x	x
	0	1	CCM	x	x
	1	1	CCM/DCM	x	x
SUSPEND	0	0	CCM/DCM	+33%	Off
	1	0	CCM/DCM	+33%	Off
	0	1	CCM/DCM	None	On
	1	1	CCM/DCM	None	Off

TABLE 2. VID TABLE FOR INTEL IMVP-6+ V_{CCGFX} CORE

	VID4	VID3	VID2	VID1	VID0	V_{CCGFX} (V)
RENDER PERFORMANCE STATES	x	x	x	x	x	0
	0	0	0	0	0	1.28750
	0	0	0	0	1	1.26175
	0	0	0	1	0	1.23600
	0	0	0	1	1	1.21025
	0	0	1	0	0	1.18450
	0	0	1	0	1	1.15875
	0	0	1	1	0	1.13300
	0	0	1	1	1	1.10725
	0	1	0	0	0	1.08150
	0	1	0	0	1	1.05575
	0	1	0	1	0	1.03000
	0	1	0	1	1	1.00425
	0	1	1	0	0	0.97850
	0	1	1	0	1	0.95275
	0	1	1	1	0	0.92700
	0	1	1	1	1	0.90125
	1	0	0	0	0	0.87550
	1	0	0	0	1	0.84975

TABLE 2. VID TABLE FOR INTEL IMVP-6+ V_{CCGFX} CORE (Continued)

	VID4	VID3	VID2	VID1	VID0	V_{CCGFX} (V)
RENDER SUSPEND STATES	1	0	0	1	0	0.82400V
	1	0	0	1	1	0.79825V
	1	0	1	0	0	0.77250V
	1	0	1	0	1	0.74675V
	1	0	1	1	0	0.72100V
	1	0	1	1	1	0.69525V
	1	1	0	0	0	0.66950V
	1	1	0	0	1	0.64375V
	1	1	0	1	0	0.61800V
	1	1	0	1	1	0.59225V
	1	1	1	0	0	0.56650V
	1	1	1	0	1	0.54075V
	1	1	1	1	0	0.51500V
	1	1	1	1	1	0.41200V

Theory of Operation

The R^3 Modulator

The heart of the ISL6263 is Intersil's Robust-Ripple-Regulator (R^3) Technology™. The R^3 modulator is a hybrid of fixed frequency PWM control, and variable frequency hysteretic control that will simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients.

The term "Ripple" in the name "Robust-Ripple-Regulator" refers to the synthesized voltage-ripple signal V_R that appears across the internal ripple-capacitor C_R. The V_R signal is a representation of the output inductor ripple current. Transconductance amplifiers measuring the input voltage of the converter and the output set-point voltage V_{SOFT}, together produce the voltage-ripple signal V_R.

A voltage window signal V_W is created across the VW and COMP pins by sourcing a current proportional to $g_m V_{soft}$ through a parallel network consisting of resistor R_{FSET} and capacitor C_{FSET}. The synthesized voltage-ripple signal V_R along with similar companion signals are converted into PWM pulses.

The PWM frequency is proportional to the difference in amplitude between V_W and V_{COMP}. Operating on these large-amplitude, low noise synthesized signals allows the ISL6263 to achieve lower output ripple and lower phase jitter than either conventional hysteretic or fixed frequency PWM controllers. Unlike conventional hysteretic converters, the ISL6263 has an error amplifier that allows the controller to maintain tight voltage regulation accuracy throughout the VID range from 0.41200V to 1.28750V.

Power-On Reset

The ISL6263 is disabled until the voltage at the VDD pin has increased above the rising VDD power-on reset (POR) V_{DD_THR} threshold voltage. The controller will become disabled when the voltage at the VDD pin decreases below the falling POR V_{DD_THF} threshold voltage.

Start-Up Timing

Figure 4 shows the ISL6263 start-up timing. Once VDD has ramped above V_{DD_THR}, the controller can be enabled by pulling the VR_ON pin voltage above the input-high threshold V_{VR_ONH}. Approximately 100µs later, the soft-start capacitor C_{SOFT} begins slewing to the designated VID set-point as it is charged by the soft-start current source I_{SS}. The V_{CCGFX} output voltage of the converter follows the V_{SOFT} voltage ramp to within 10% of the VID set-point then counts 6 switching cycles, then changes the open-drain output of the PGOOD pin to high impedance. During soft-start, the regulator always operates in continuous conduction mode (CCM).

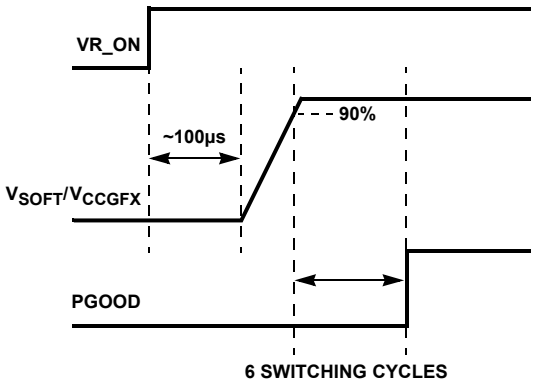


FIGURE 4. ISL6263 START-UP TIMING

Static Regulation

The V_{CCGFX} output voltage will be regulated to the value set by the VID inputs per Table 2. A true differential amplifier connected to the VSEN and RTN pins implements processor socket Kelvin sensing for precise core voltage regulation at the GPU voltage sense points.

As the load current increases from zero, the V_{CCGFX} output voltage will droop from the VID set-point by an amount proportional to the IMVP-6+ load line. The ISL6263 can accommodate DCR current sensing or discrete resistor current sensing. The DCR current sensing uses the intrinsic series resistance of the output inductor as shown in the application circuit of Figure 2. The discrete resistor current sensing uses a shunt connected in series with the output inductor as shown in the application circuit of Figure 3. In both cases the signal is fed to the non-inverting input of the DROOP amplifier at the VSUM pin, where it is measured differentially with respect to the output voltage of the converter at the VO pin and amplified. The voltage at the

DROOP pin minus the output voltage measured at the VO pin, is proportional to the total inductor current. This information is used exclusively to achieve the IMVP-6+ load line as well as the overcurrent protection. It is important to note that this current measurement should not be confused with the synthetic current ripple information created within the R^3 modulator.

When using inductor DCR current sensing, an NTC element is used to compensate the positive temperature coefficient of the copper winding thus maintaining the load-line accuracy.

Processor Socket Kelvin Voltage Sensing

The remote voltage sense input pins VSEN and RTN of the ISL6263 are to be terminated at the die of the GPU through connections that mate at the processor socket. (The signal names are Vcc_sense and Vss_sense respectively.) Kelvin sensing allows the voltage regulator to tightly control the processor voltage at the die, compensating for various resistive voltage drops in the power delivery path.

Since the voltage feedback is sensed at the processor die, removing the GPU will open the voltage feedback path of the regulator, causing the output voltage to rise towards VIN. The ISL6263 will shut down when the voltage between the VO and VSS pins exceeds the severe overvoltage protection threshold V_{OVPS} of 1.55V. To prevent this issue from occurring, it is recommended to install resistors Ropn1 and Ropn2 as shown in Figure 5. These resistors provide voltage feedback from the regulator local output in the absence of the GPU. These resistors should be in the range of 20Ω to 100Ω.

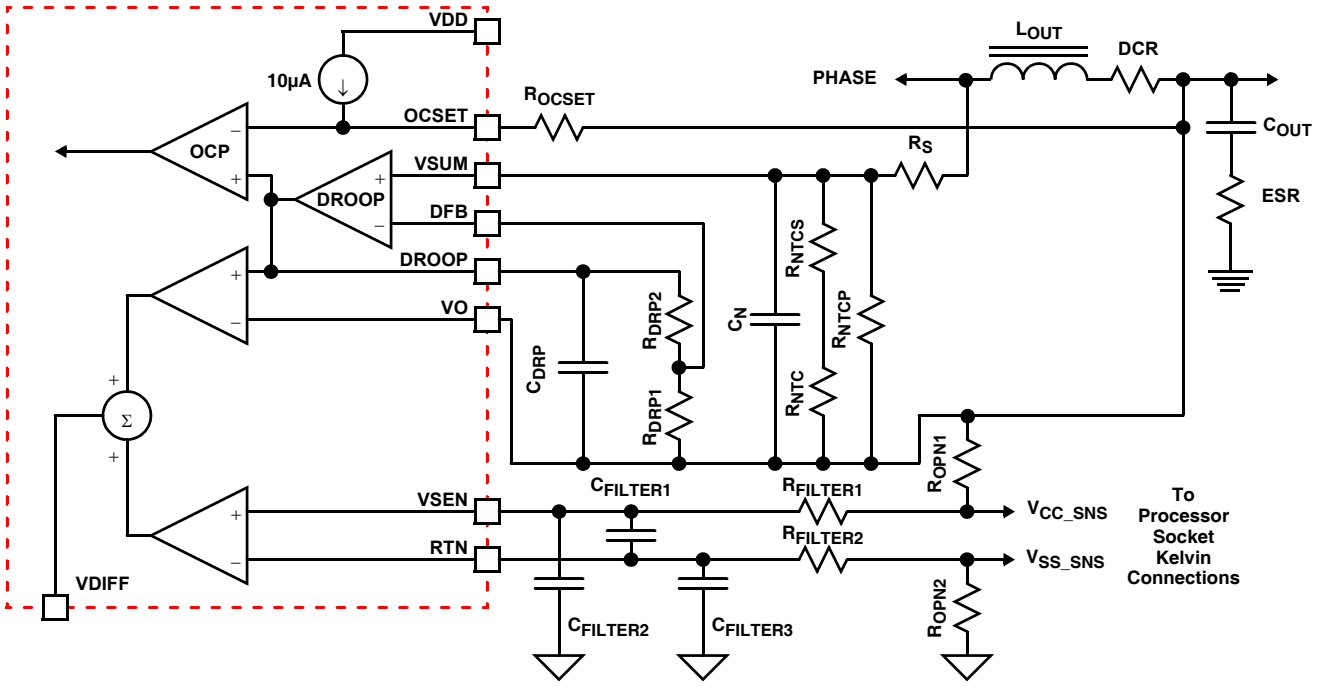


FIGURE 5. SIMPLIFIED VOLTAGE DROOP CIRCUIT WITH GPU SOCKET KELVIN SENSING AND INDUCTOR DCR CURRENT SENSING

High Efficiency Diode Emulation Mode

The ISL6263 operates in continuous-conduction-mode (CCM) during heavy load for minimum conduction loss by forcing the low-side MOSFET to operate as a synchronous rectifier. Depending upon the VID and FDE pin states, an improvement in light-load efficiency can be achieved by operating in discontinuous-conduction-mode (DCM) where the low-side MOSFET is operated in diode-emulation-mode (DEM), forcing the low-side MOSFET to block negative inductor current flow.

Positive-going inductor current flows from either the source of the high-side MOSFET, or the drain of the low-side MOSFET. Negative-going inductor current flows into the source of the high-side MOSFET, or the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the VSS pin. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the VSS pin. Negative inductor current occurs in CCM when the output load current is less than ½ the inductor ripple current. Sinking negative inductor through the low-side MOSFET lowers efficiency through unnecessary conduction losses. Upon entering DEM the PWM switching frequency is automatically shifted downward by an increase of the window voltage V_W of 33%. The PWM switching frequency will continue to decrease as the load continues to decrease. The reduction of PWM

frequency further improves efficiency by reducing switching losses. The converter will automatically enter DEM after eight consecutive PWM pulses where the PHASE pin has detected positive voltage shortly after the LGATE pin has gone high. The converter will return to CCM on the following cycle after the PHASE pin detects negative voltage shortly after the LGATE pin has gone high, indicating that the body diode of the low-side MOSFET is conducting positive inductor current. The converter inhibits the automatic 33% change of V_W whenever the audio filter is enabled.

Smooth mode transitions are facilitated by the R^3 modulator which correctly maintains the internally synthesized ripple current information throughout mode transitions.

Protection

The ISL6263 provides overcurrent protection (OCP), overvoltage protection (OVP), and undervoltage protection (UVP) as shown in Table 3.

Overcurrent protection is tied to the voltage droop, which is determined by the resistors selected in the Static Droop Design Using DCR Sensing section. After the load line is set, the OCSET resistor can be selected. The OCP threshold detector is checked every 15µs and will increment a counter if the OCP threshold is exceeded, conversely the counter will be decremented if the load current is below the OCP threshold. The counter will latch an OCP fault when the counter reaches eight. The fastest OCP response for overcurrent events occurring above the OCP threshold but below twice the OCP threshold is 120µs, which is eight counts at 15µs each. The ISL6263 will latch an OCP fault within 2µs for an overcurrent exceeding twice the OCP threshold to maximize protection against hard shorts. The value of R_{OCSET} is calculated as Equation 1:

$$R_{OCSET} = \frac{I_{OC} \cdot R_{droop}}{10\mu A} \quad \text{(EQ. 1)}$$

For example: The desired overcurrent trip level, I_{oc}, is 30A, R_{droop} load-line is 8mΩ, Equation 1 gives R_{OCSET} = 24kΩ.

Undervoltage protection is independent of the overcurrent protection. If the output voltage measured on the VO pin is less than +300mV below the voltage on the SOFT pin for longer than 1ms, the controller will latch a UVP fault. If the output voltage measured on the VO pin is greater than +200mV above the voltage on the SOFT pin for longer than 1ms, the controller will latch an OVP fault. Keep in mind that V_{SOFT} will equal the voltage level commanded by the VID states only after the soft-start capacitor C_{SOFT} has slewed to the VID DAC output voltage. The UVP and OVP detection circuits act on static and dynamic V_{SOFT} voltage.

When an OCP, OVP, or UVP fault has been latched, PGOOD becomes a low impedance and the gate driver outputs UGATE and LGATE are pulled low. The energy stored in the inductor is dissipated as current flows through the low-side MOSFET body diode. The controller will remain latched in the fault state until the VR_ON pin has been pulled below the falling VR_ON threshold voltage V_{VR_ONL} or until VDD has gone below the falling POR threshold voltage V_{VDD_THF}.

A severe-overvoltage protection fault occurs immediately after the voltage between the VO and VSS pins exceed the rising severe-overvoltage threshold V_{OVPS} which is 1.545V, the same reference voltage used by the VID DAC. The ISL6263 will latch UGATE and PGOOD low but unlike other protective faults, LGATE remains high until the voltage between VO and VSS falls below approximately 0.77V, at which time LGATE is pulled low. The LGATE pin will continue to switch high and low at 1.545V and 0.77V until VDD has gone below the falling POR threshold voltage V_{VDD_THF}. This provides maximum protection against a shorted high-side MOSFET while preventing the output voltage from ringing below ground. The severe-overvoltage fault circuit can be triggered after another fault has already been latched.

TABLE 3. FAULT PROTECTION SUMMARY OF ISL6263

FAULT TYPE	FAULT DURATION PRIOR TO PROTECTION	PROTECTION ACTIONS	FAULT RESET
Overcurrent	120µs	LGATE, UGATE, and PGOOD latched low	Cycle VR_ON or VDD
Short Circuit	<2µs	LGATE, UGATE, and PGOOD latched low	Cycle VR_ON or VDD
Overvoltage (+200mV) between VO pin and SOFT pin	1ms	LGATE, UGATE, and PGOOD latched low	Cycle VR_ON or VDD
Severe Overvoltage (+1.55V) between VO pin and VSS pin	Immediately	UGATE, and PGOOD latched low, LGATE toggles ON when VO>1.55V OFF when VO <0.77V until fault reset	Cycle VDD only
Undervoltage (-300mV) between VO pin and SOFT pin	1ms	LGATE, UGATE, and PGOOD latched low	Cycle VR_ON or VDD

Gate-Driver Outputs LGATE and UGATE

The ISL6263 has internal high-side and low-side N-Channel MOSFET gate-drivers. The LGATE driver is optimized for low duty-cycle applications where the low-side MOSFET conduction losses are dominant. The LGATE pull-down resistance is very low in order to clamp the gate-source voltage of the MOSFET below the $V_{GS(th)}$ at turnoff. The current transient through the low-side gate at turnoff can be considerable due to the characteristic large switching charge of a low $r_{DS(on)}$ MOSFET.

Adaptive shoot-through protection prevents the gate-driver outputs from going high until the opposite gate-driver output has fallen below approximately 1V. The UGATE turn-on propagation delay t_{PDRU} and LGATE turn-on propagation delay t_{PDRL} are found in the Electrical Specifications table. The power for the LGATE gate-driver is sourced directly from the PVCC pin. The power for the UGATE gate-driver is sourced from a boot-strap capacitor connected across the BOOT and PHASE pins. The boot capacitor is charged from PVCC through an internal boot-strap diode each time the low-side MOSFET turns on, pulling the PHASE pin low.

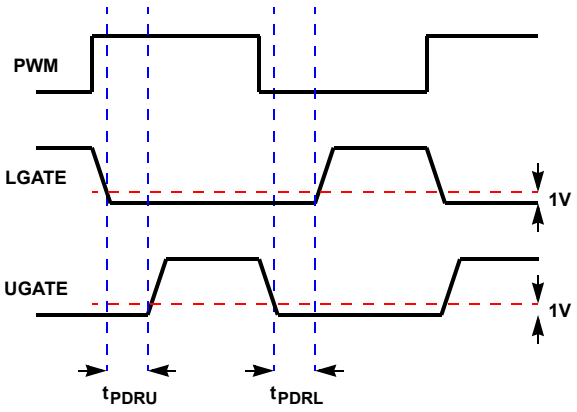


FIGURE 6. GATE DRIVER TIMING DIAGRAM

Internal Bootstrap Diode

The ISL6263 has an integrated boot-strap Schottky diode connected from the PVCC pin to the BOOT pin. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.

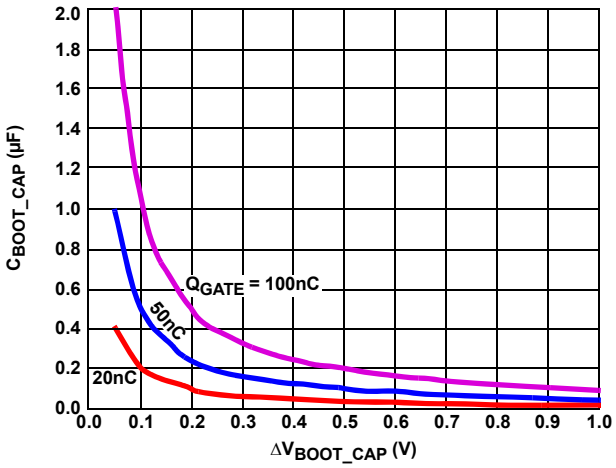


FIGURE 7. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

The minimum value of the bootstrap capacitor can be calculated from Equation 2:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 2)}$$

where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. The ΔV_{BOOT} term is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge, Q_{GATE}, of 25nC at 5V and also assume the droop in the drive voltage at the end of a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.15µF. A good quality ceramic capacitor is recommended.

Soft-Start and Soft Dynamic VID Slew Rates

The output voltage of the converter tracks V_{SOFT}, the voltage across the SOFT and VSS pins. Shown in Figure 1, the SOFT pin is connected to the output of the VID DAC through the unidirectional soft-start current source I_{SS} or the bidirectional soft-dynamic VID current source I_{DVID}, and the non-inverting input of the error amplifier. Current is sourced from the SOFT pin when I_{SS} is active. The SOFT pin can both source and sink current when I_{DVID} is active. The soft-start capacitor C_{SOFT} changes voltage at a rate proportional to I_{SS} or I_{DVID}. The ISL6263 automatically selects I_{SS} for the soft-start sequence so that the inrush current through the output capacitors is maintained below the OCP threshold. Once soft-start has completed, I_{DVID} is automatically selected for output voltage changes commanded by the VID inputs, charging C_{SOFT} when the output voltage is commanded to rise, and discharging C_{SOFT} when the output voltage is commanded to fall.

The IMVP-6+ Render Voltage Regulator specification requires a minimum of 10mV/µs for $SLEWRATE_{GFX}$. The value for C_{SOFT} must guarantee the minimum slew-rate of 10mV/µs when the soft-dynamic VID current source I_{DVID} is the minimum specified value in the Electrical Specifications table. The value of C_{SOFT}, can be calculated from Equation 3:

$$C_{SOFT} = \frac{I_{DVIDmin}}{\left(\frac{10mV}{\mu s}\right)} = \frac{175\mu A}{10K} = 0.0175\mu F \quad \text{(EQ. 3)}$$

Choosing the next lower standard component value of 0.015µF will guarantee 10mV/µs $SLEWRATE_{GFX}$. This choice of C_{SOFT} controls the startup slew-rate as well. One should expect the output voltage during soft-start to slew to the voltage commanded by the VID settings at a nominal rate given by Equation 4:

$$\frac{dV_{SOFT}}{dt} = \frac{I_{SS}}{C_{SOFT}} = \frac{41\mu A}{0.015\mu F} \approx \frac{2.8mV}{\mu s} \quad \text{(EQ. 4)}$$

Note that the slewrate is the average rate of change between the initial and final voltage values. The slewrate is moderated as V_{CCGFX} approaches the voltage commanded by the VID inputs.

RBIAS Current Reference

The RBIAS pin is internally connected to a 1.545V reference through a 3kΩ resistance. A bias current is established by connecting a ±1% tolerance, 150kΩ resistor between the RBIAS and VSS pins. This bias current is mirrored, creating the OCSET reference current I_{OCSET} that is sourced from the OCSET pin. Do not connect any other components to this pin, as they will have a negative impact on the performance of the IC.

I2UA Current Reference

The I2UA pin is connected to a 2µA current source I_{I2UA}. This current source is made available for implementing a voltage offset of the commanded VID states. A 20kΩ resistor R_{I2UA} should be connected across the I2UA and VSS pins if the I_{I2UA} current source is unused.

Setting the PWM Switching Frequency

The R^3 modulator scheme is not a fixed-frequency architecture, lacking a fixed-frequency clock signal to produce PWM. The switching frequency increases during the application of a load to improve transient performance. The static PWM frequency varies slightly depending on the input voltage, output voltage, and output current, but this variation is normally less than 10% in continuous conduction mode.

Refer to Figure 2, and find that resistor R_{FSET} is connected between the VW and COMP pins. A current is sourced from VW through R_{FSET} creating the synthetic ripple window voltage signal V_W which determines the PWM switching frequency. The relationship between the resistance of R_{FSET} and the switching frequency in CCM is approximately given by Equation 5:

$$R_{FSET} = \frac{1}{(T - 0.29\times10^{-6})\cdot 47} \quad \text{(EQ. 5)}$$

For example, the value of R_{FSET} for 300kHz operation is approximately:

$$7\times10^{3} = \frac{1}{(3.33\times10^{-6} - 0.29\times10^{-6})\cdot 47} \quad \text{(EQ. 6)}$$

This relationship only applies to operation in constant conduction mode because the PWM frequency naturally decreases as the load decreases while in diode emulation mode. Note that the Electrical Specifications table gives the nominal PWM frequency of 333kHz with R_{FSET} = 7kΩ, different from the result of equation Equation 6. This is because the IC is trimmed with V_{COMP} = 2V which is higher than the typical value encountered in a typical application.

Static Droop Design Using DCR Sensing

The ISL6263 has an internal differential amplifier to accurately regulate the voltage at the processor die.

For DCR sensing, the process to compensate the DCR resistance variation takes several iterative steps. Figure 2 shows the DCR sensing method. Figure 8 shows the simplified model of the droop circuitry. The inductor DC current generates a DC voltage drop on the inductor DCR. Equation 7 gives this relationship:

$$V_{DCR} = I_o \cdot DCR \quad \text{(EQ. 7)}$$

An R-C network senses the voltage across the inductor to get the inductor current information. R_{NTCEQ} represents the NTC network consisting of R_{NTC}, $R_{NTCS,\ and}$ R_{NTCP}. The choice of R_S will be discussed in the next section.

The first step in droop load line compensation is to adjust R_{NTCEQ}, and R_S such that the correct droop voltage appears even at light loads between the VSUM and VO pins. As a rule of thumb, the voltage drop V_N across the R_{NTCEQ} network, is set to be 0.5x to 0.8x V_{DCR}. This gain, defined as G_1, provides a reasonable amount of light load signal from which to derive the droop voltage.

The NTC network resistor value is dependent on temperature and is given by Equation 8:

$$R_N(T) = \frac{(R_{NTC} + R_{NTCS})\cdot R_{NTCP}}{R_{NTC} + R_{NTCS} + R_{NTCP}} \quad \text{(EQ. 8)}$$

G_1, the gain of V_N to V_{DCR}, is also dependent on the temperature of the NTC thermistor:

$$G_1(T) = \frac{R_N(T)}{R_N(T) + R_S} \quad \text{(EQ. 9)}$$

The inductor DCR is a function of temperature and is approximately given by Equation 10:

$$DCR(T) = DCR_{25°C}\cdot(1 + 0.00393\cdot(T - 25°C)) \quad \text{(EQ. 10)}$$

The droop amplifier output voltage divided by the total load current is given by Equation 11:

$$R_{droop} = G_1(T)\cdot DCR_{25°C}\cdot(1 + 0.00393\cdot(T - 25°C))\cdot k_{droopamp} \quad \text{(EQ. 11)}$$

R_{droop} is the actual load line slope, and 0.00393 is the temperature coefficient of the copper. To make R_{droop} independent of the inductor temperature, it is desired to have Equation 12:

$$G_1(T)\cdot(1 + 0.00393\cdot(T - 25°C)) \cong G_{1target} \quad \text{(EQ. 12)}$$

where $G_{1target}$ is the desired ratio of V_n / V_{DCR}. Therefore, the temperature characteristics G_1 is described by Equation 13:

$$G_1(T) = \frac{G_{1target}}{(1 + 0.00393\cdot(T - 25°C))} \quad \text{(EQ. 13)}$$

It is recommended to begin your droop design using the R_{NTC}, R_{NTCS}, and R_{NTCP} component values of the evaluation board available from Intersil.

The gain of the droop amplifier circuit is Equation 14:

$$k_{droopamp} = 1 + \frac{R_{DRP2}}{R_{DRP1}} \quad \text{(EQ. 14)}$$

After determining R_S and R_{NTCEQ} networks, use Equation 15 to calculate the droop resistances R_{DRP1} and R_{DRP2}.

$$R_{DRP2} = \left(\left(\frac{R_{droop}}{DCR \cdot G_{1(25°C)}}\right) - 1\right) \cdot R_{DRP1} \quad \text{(EQ. 15)}$$

R_{droop} is 8mΩ per Intel IMVP-6+ specification and R_{DRP1} is typically 1kΩ.

The effectiveness of the R_{NTCEQ} network is sensitive to the coupling coefficient between the NTC thermistor and the inductor. The NTC thermistor should be placed in the closet proximity of the inductor.

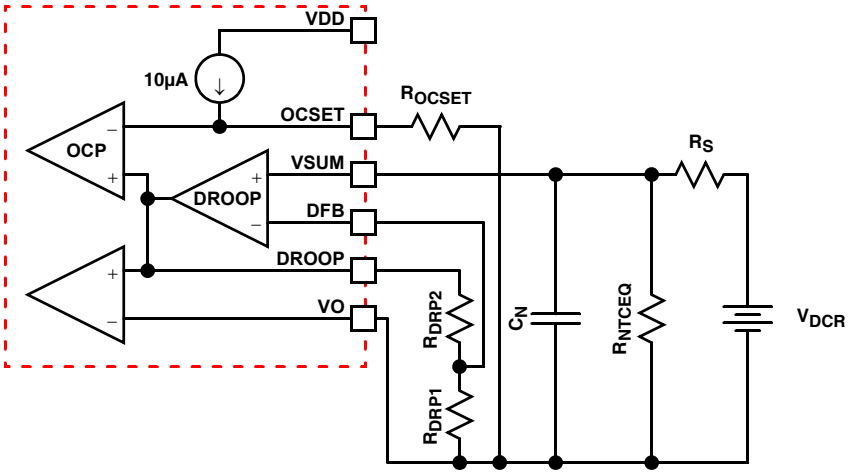


FIGURE 8. EQUIVALENT MODEL FOR DROOP CIRCUIT USING INDUCTOR DCR CURRENT SENSING

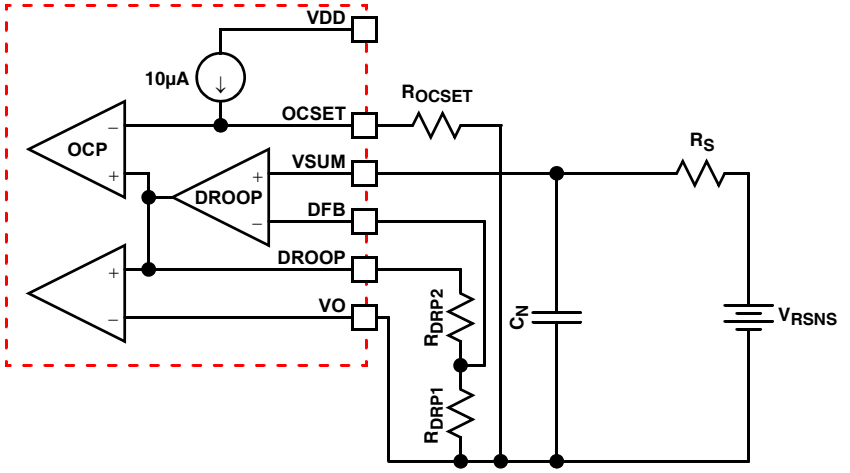


FIGURE 9. EQUIVALENT MODEL FOR DROOP CIRCUIT USING DISCRETE RESISTOR CURRENT SENSING

To see whether the NTC network successfully compensates the DCR change over temperature, one can apply full load current and wait for the thermal steady state and see how much the output voltage deviates from the initial voltage reading. A good compensation can limit the drift to less than 2mV. If the output voltage is decreasing when the temperature increases, that ratio between the NTC thermistor value and the rest of the resistor divider network has to be increased. Following the evaluation board value and layout of NTC placement will minimize the engineering time.

The current sensing traces should be routed directly to the inductor pads for accurate DCR voltage drop measurement. However, due to layout imperfection, the calculated R_{DRP2} may still need slight adjustment to achieve optimum load line slope. It is recommended to adjust R_{DRP2} after the system has achieved thermal equilibrium at full load. For example, if the maximum load current is 20A, one should apply a 20A load current and look for 160mV output voltage droop. If the voltage droop is 155mV, the new value of R_{DRP2} is calculated by Equation 16:

$$R_{DRP2new} = \frac{160mV}{155mV} \cdot (R_{DRP1} - R_{DPR2}) - R_{DRP1} \quad \text{(EQ. 16)}$$

For the best accuracy, the effective resistance on the DFB and VSUM pins should be identical so that the bias current of the droop amplifier does not cause an offset voltage.

Dynamic Droop Capacitor Design Using DCR Sensing

Figure 10 shows the desired waveforms during load transient response. V_{CCGFX} needs to follow the change in I_{core} as close as possible. The transient response of V_{CCGFX} is determined by several factors, namely the choice of output inductor, output capacitor, compensator design, and the design of droop capacitor C_N.

If C_N is designed correctly, the voltage V_{DROOP} -V_O will be an excellent representation of the inductor current. Given the correct C_N design, V_{CCGFX} has the best chance of tracking I_{CORE}, if not, its voltage will be distorted from the actual waveform of the inductor current and worsens the transient response. Figure 11 shows the transient response when C_N is too small allowing V_{CCGFX} to sag excessively during the load transient. Figure 12 shows the transient response when C_N is too large. V_{CCGFX} takes too long to droop to its final value.

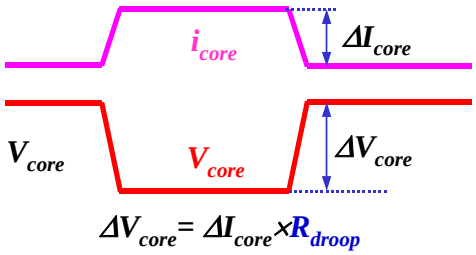


FIGURE 10. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

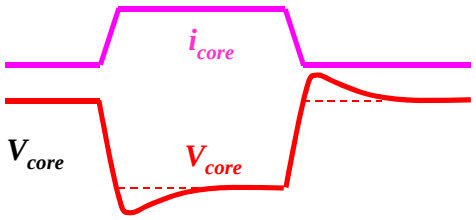


FIGURE 11. LOAD TRANSIENT RESPONSE WHEN C_N IS TOO SMALL

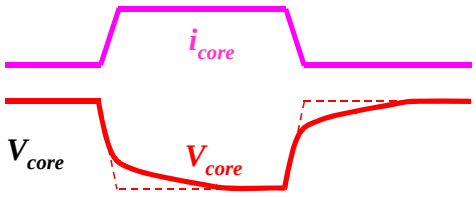


FIGURE 12. LOAD TRANSIENT RESPONSE WHEN C_N IS TOO LARGE

The current sensing network consists of R_{NTCEQ}, R_S, and C_N. The effective resistance is the parallel of R_{NTCEQ} and R_S. The RC time constant of the current sensing network needs to match the L/DCR time constant of the inductor to get the correct representation of the inductor current waveform. Equation 17 shows this relationship:

$$\frac{L}{DCR} = \left(\frac{R_{NTCEQ} \cdot R_S}{R_{NTCEQ} + R_S}\right) \cdot C_N \quad \text{(EQ. 17)}$$

Solution of C_N yields Equation 18:

$$C_N = \frac{\left(\frac{L}{DCR}\right)}{\left(\frac{R_{NTCEQ} \cdot R_S}{R_{NTCEQ} + R_S}\right)} \quad \text{(EQ. 18)}$$

For example: L = 0.45µH, DCR = 1.1mΩ, R_S = 7.68kΩ, and R_{NTCEQ} = 3.4kΩ:

$$C_N = \frac{\left(\frac{0.45\mu H}{1.1m\Omega}\right)}{\left(\frac{3.4k\Omega \cdot 7.68k\Omega}{3.4k\Omega + 7.68k\Omega}\right)} = 174nF \quad \text{(EQ. 19)}$$

Since the inductance and the DCR typically have 20% and 7% tolerance respectively, C_N needs to be fine tuned on the

actual board by examining the transient voltage. It is recommended to choose the minimum capacitance based on the maximum inductance. C_N also needs to be a high-grade capacitor such as NPO/COG or X7R with tight tolerance. The NPO/COG caps are only available in small capacitance values. In order to use such capacitors, the resistors and thermistors surrounding the droop voltage sensing and droop amplifier need to be scaled up 10x to reduce the capacitance by 10x.

Static and Dynamic Droop using Discrete Resistor Sensing

Figure 3 shows a detailed schematic using discrete resistor sensing of the inductor current. Figure 9 shows the equivalent circuit. Since the current sensing resistor voltage represents the actual inductor current information, R_S and C_N simply provide noise filtering. A low ESL sensing resistor is strongly recommended for R_{SNS} because this parameter is the most significant source of noise that affects discrete resistor sensing. It is recommended to start out using 100Ω for R_S and 47pF for C_N. Since the current sensing resistance changes very little with temperature, the NTC network is not needed for thermal compensation. Discrete resistor sensing droop design follows the same approach as DCR sensing. The voltage on the current sensing resistor is given by Equation 20:

$$V_{RSNS} = I_o \cdot R_{SNS} \quad \text{(EQ. 20)}$$

Equation 21 shows the droop amplifier gain. So the actual droop is given by:

$$R_{droop} = R_{SNS} \cdot \left(1 + \frac{R_{DRP2}}{R_{DRP1}}\right) \quad \text{(EQ. 21)}$$

Solution to R_{DRP2} yields Equation 22:

$$R_{DRP2} = R_{DRP1} \cdot \left(\frac{R_{droop}}{R_{SNS}} - 1\right) \quad \text{(EQ. 22)}$$

For example: R_{droop} = 8.0mΩ, R_{SNS} = 1.0mΩ, and R_{DRP1} = 1kΩ, R_{DRP2} then = 7kΩ.

The current sensing traces should be routed directly to the current sensing resistor pads for accurate measurement. However, due to layout imperfection, the calculated R_{DRP2} may still need slight adjustment to achieve optimum load line slope. It is recommended to adjust R_{DRP2} after the system has achieved thermal equilibrium at full load.

Dynamic Mode of Operation - Compensation Parameters

The voltage regulator is equivalent to a voltage source in series with the output impedance. The voltage source is the VID state and the output impedance is 8.0mΩ in order to achieve the 8.0mV/A load line. It is highly recommended to design the compensation such that the regulator output impedance is 8.0mΩ. Intersil provides a spreadsheet to calculate the compensator parameters. Caution needs to be used in choosing the input resistor to the FB pin. Excessively high resistance will cause an error to the output voltage regulation due to the bias current flowing through the FB pin. It is recommended to keep this resistor below 3kΩ.

Layout Considerations

As a general rule, power should be on the bottom layer of the PCB and weak analog or logic signals are on the top layer of the PCB. The ground-plane layer should be adjacent to the top layer to provide shielding.

Inductor Current Sensing and the NTC Placement

It is crucial that the inductor current be sensed directly at the PCB pads of the sense element, be it DCR sensed or discrete resistor sensed. The effect of the NTC on the inductor DCR thermal drift is directly proportional to its thermal coupling with the inductor and thus, the physical proximity to it.

Signal Ground and Power Ground

The ground plane layer should have a single point connection to the analog ground at the VSS pin. The VSS island should be located under the IC package along with the weak analog traces and components. The paddle on the bottom of the ISL6263 QFN package is not electrically connected to the IC however, it is recommended to make a good thermal connection to the VSS island using several vias. Connect the input capacitors, the output capacitors, and the source of the lower MOSFETs to the power ground plane.

LGATE, PVCC, and PGND

PGND is the return path for the pull-down of the LGATE low-side MOSFET gate driver. Ideally, PGND should be connected to the source of the low-side MOSFET with a low-resistance, low-inductance path. The LGATE trace should be routed in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces because of the high peak current and extremely fast dv/dt. PVCC should be decoupled to PGND with a ceramic capacitor physically located as close as practical to the IC pins.

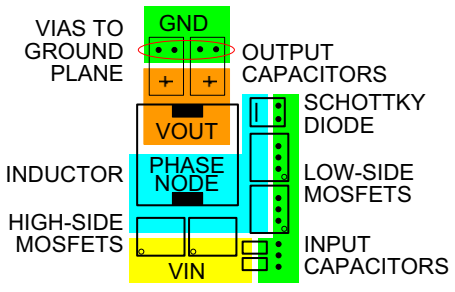


FIGURE 13. TYPICAL POWER COMPONENT PLACEMENT

UGATE, BOOT, and PHASE

PHASE is the return path for the entire UGATE high-side MOSFET gate driver. The layout for these signals require similar treatment, but to a greater extent, than those for LGATE, PVCC, and PGND. These signals swing from approximately VIN to VSS and are more likely to couple into other signals.

VSEN and RTN

These traces should be laid out as noise sensitive. For optimum load line regulation performance, the traces connecting these two pins to the Kelvin sense leads of the processor should be laid out away from rapidly rising voltage nodes, (switching nodes) and other noisy traces. The filter capacitors $C_{FILTER1}$, $C_{FILTER2}$, and $C_{FILTER3}$ used in conjunction with filter resistors $R_{FILTER1}$ and $R_{FILTER2}$ form common mode and differential mode filters as shown in Figure 8. The noise environment of the application and actual board layout conditions will drive the extent of filter complexity. The maximum recommended resistance for $R_{FILTER1}$ and $R_{FILTER2}$ is approximately 10Ω to avoid interaction with the 50kΩ input resistance of the remote sense differential amplifier. The physical location of these resistors is not as critical as the filter capacitors. Typical capacitance values for $C_{FILTER1}$, $C_{FILTER2}$, and $C_{FILTER3}$ range between 330pF to 1000pF and should be placed near the IC.

RBIAS and I2UA

The resistors R_{RBIAS} and R_{I2UA} should be placed in close proximity to the ISL6263 using a noise-free current return path to the VSS pin.

SOFT, OCSET, VW, COMP, FB, VDIFF, DROOP, DFB, VO, and VSUM

The traces and components associated with these pins require close proximity to the IC as well as close proximity to each other. This section of the converter circuit needs to be located above the island of analog ground with the single-point connection to the VSS pin.

Resistor R_S

Resistor R_S is preferably located near the boundary between the power ground and the island of analog ground connected to the VSS pin.

VID<0:4>, AF_EN, PGOOD, and VR_ON

These are logic signals that do not require special attention.

FDE

This logic signal should be treated as noise sensitive and should be routed away from rapidly rising voltage nodes, (switching nodes) and other noisy traces.

VIN

The VIN signal should be connected near the drain of the high-side MOSFET.

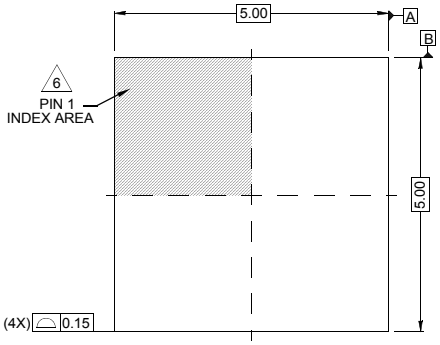
Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the high-side MOSFET and the source of the low-side MOSFET to suppress turn-off voltage spikes.

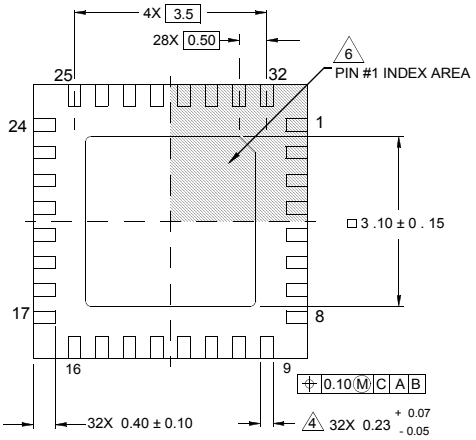
Package Outline Drawing

L32.5x5

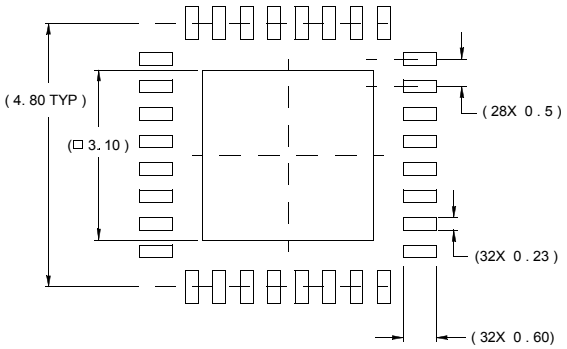
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 4/10



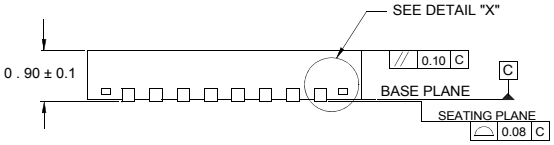
TOP VIEW



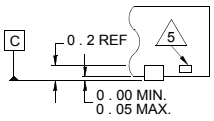
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.