ISL6423B

Single Output LNB Supply and Control Voltage Regulator with I2C Interface for Advanced Satellite Set-Top Box Designs

FN6412
Rev 1.00
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The ISL6423B is a highly integrated voltage regulator and interface IC, specifically designed for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNBs) of singe antenna ports. The device consists of a current-mode boost PWM and a low-noise linear regulator along with the circuitry required for 22kHz tone generation, modulation and I^2C device interface. The device makes the total LNB supply design simple, efficient and compact with low external component count.

The current-mode boost converters provides the linear regulator with input voltage that is set to the final output voltages, plus typically 0.8V to insure minimum power dissipation across each linear regulator. This maintains constant voltage drop across the linear pass element while permitting adequate voltage range for tone injection.

The final regulated output voltage is available at output terminals to support the operation of an antenna port for single tuners. The outputs for each PWM can be controlled in two ways, full control from I^2C using the VTOP and VBOT bits or set the I^2C to the lower range i.e., 13V/14V, and switch to higher range i.e., 18V/19V, with the SELVTOP pin. All the functions on this IC are controlled via the I^2C bus by writing 8 bits words onto the System Registers (SR). The same register can be read back, and five I^2C bits will report the diagnostic status. Separate enable command sent on the I^2C bus provides for standby mode control for the PWM and linear combination, disabling the output and forcing a shutdown mode. The output channel is capable of providing 750mA of continuous current. The overcurrent limit can be digitally programmed to four levels.

The External modulation input EXTM can accept a modulated Diseqc command and transfer it symmetrically to the output. Alternatively the EXTM pin can be used to modulate the continuos internal tone.

The $\overline{FLT}$ pin serves as an interrupt for the processor when any condition turns OFF the LNB controller (Over Temperature, Overcurrent, Disabled). The nature of the Disable can be read of the I^2C registers.

Features

- Single Chip Power solution
  - Operation for 1-Tuner/1-Dish Applications
  - Integrated DC/DC Converter and I^2C Interface
- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWMs with >92% Efficiency
  - Selectable 13.3V or 18.3V Outputs
  - Digital Cable Length Compensation (1V)
  - I^2C and Pin Controllable Output
- Output Back Bias Capability of 28V
- I^2C Compatible Interface for Remote Device Control
- Registered Slave Address 0001 00XX
- 2.5V, 3.3V, 5V Logic Compatible
- External Pin to Toggle Between V and H Polarization
- Built-In Tone Oscillator Factory Trimmed to 22kHz
  - Facilitates DiSEqC (EUTELSAT) Encoding
  - External Modulation Input
- Internal Over-Temperature Protection and Diagnostics
- Internal OV, UV, Overload and Overtemp Flags (Visible on I^2C)
- $\overline{FLT}$ signal
- LNB Short-Circuit Protection and Diagnostics
- QFN, EPTSSOP Packages
- Pb-Free Available (RoHS Compliant)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

Ordering Information

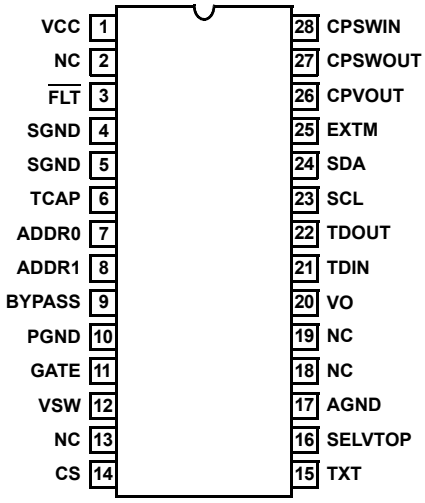
PART NUMBER*	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6423BERZ (Note)	6423BERZ	-20 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4D
ISL6423BEVEZ (Note)	ISL6423BEVEZ	-20 to +85	28 Ld EPTSSOP (Pb-free)	M28.173B

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

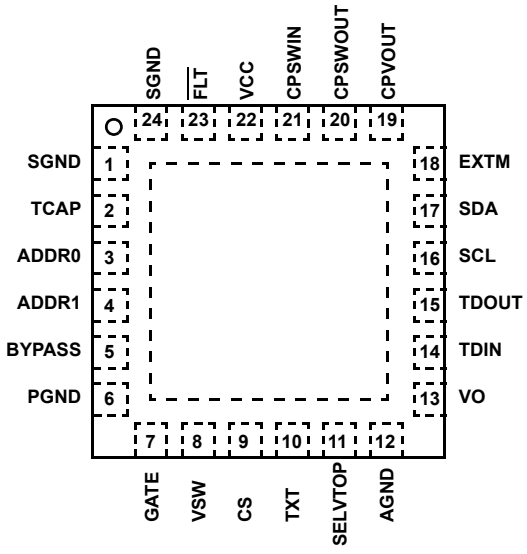
Add “-T” suffix for tape and reel.

Pinouts

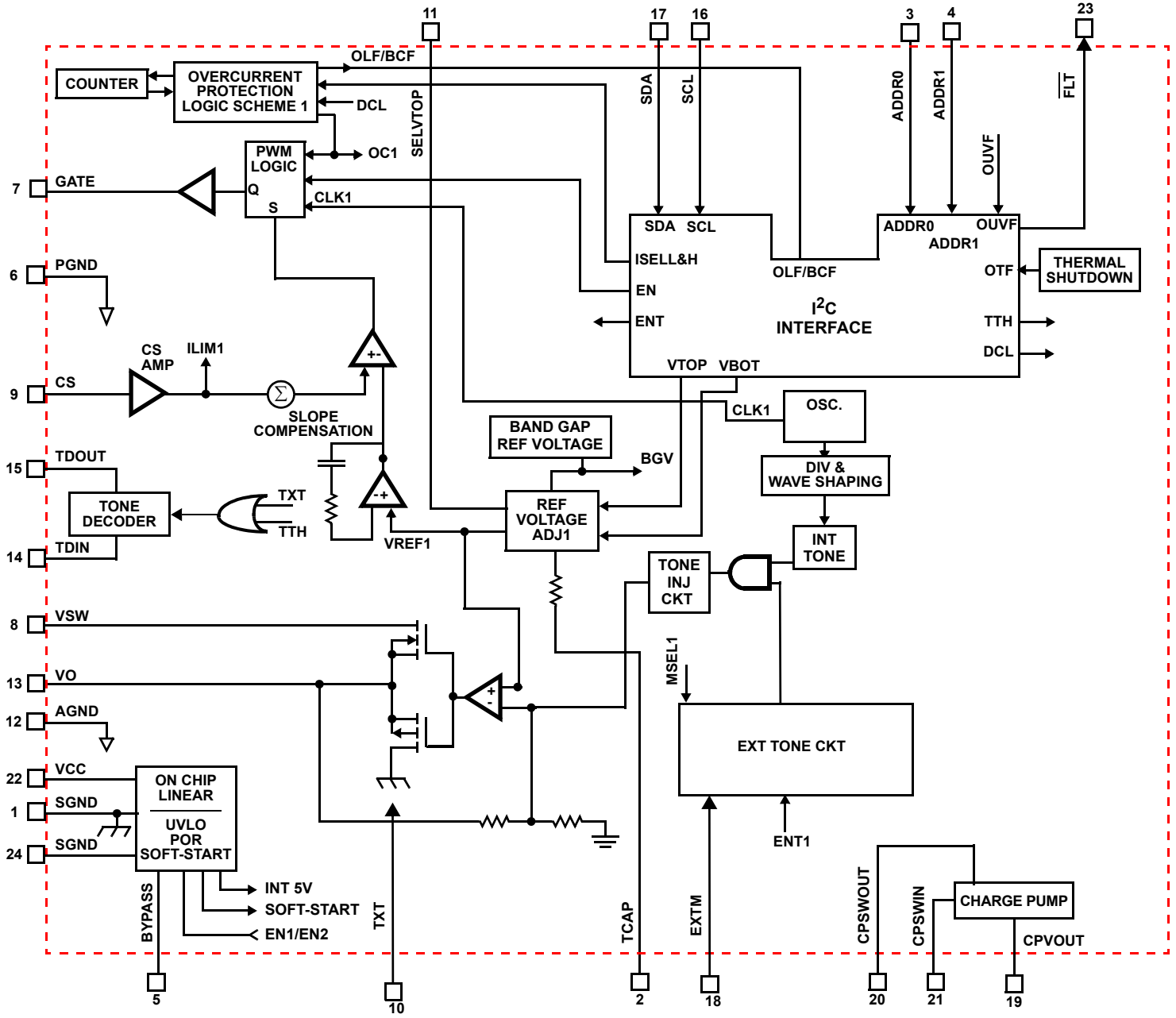
ISL6423B
(28 LD EPTSSOP)
TOP VIEW



ISL6423B
(24 LD QFN)
TOP VIEW



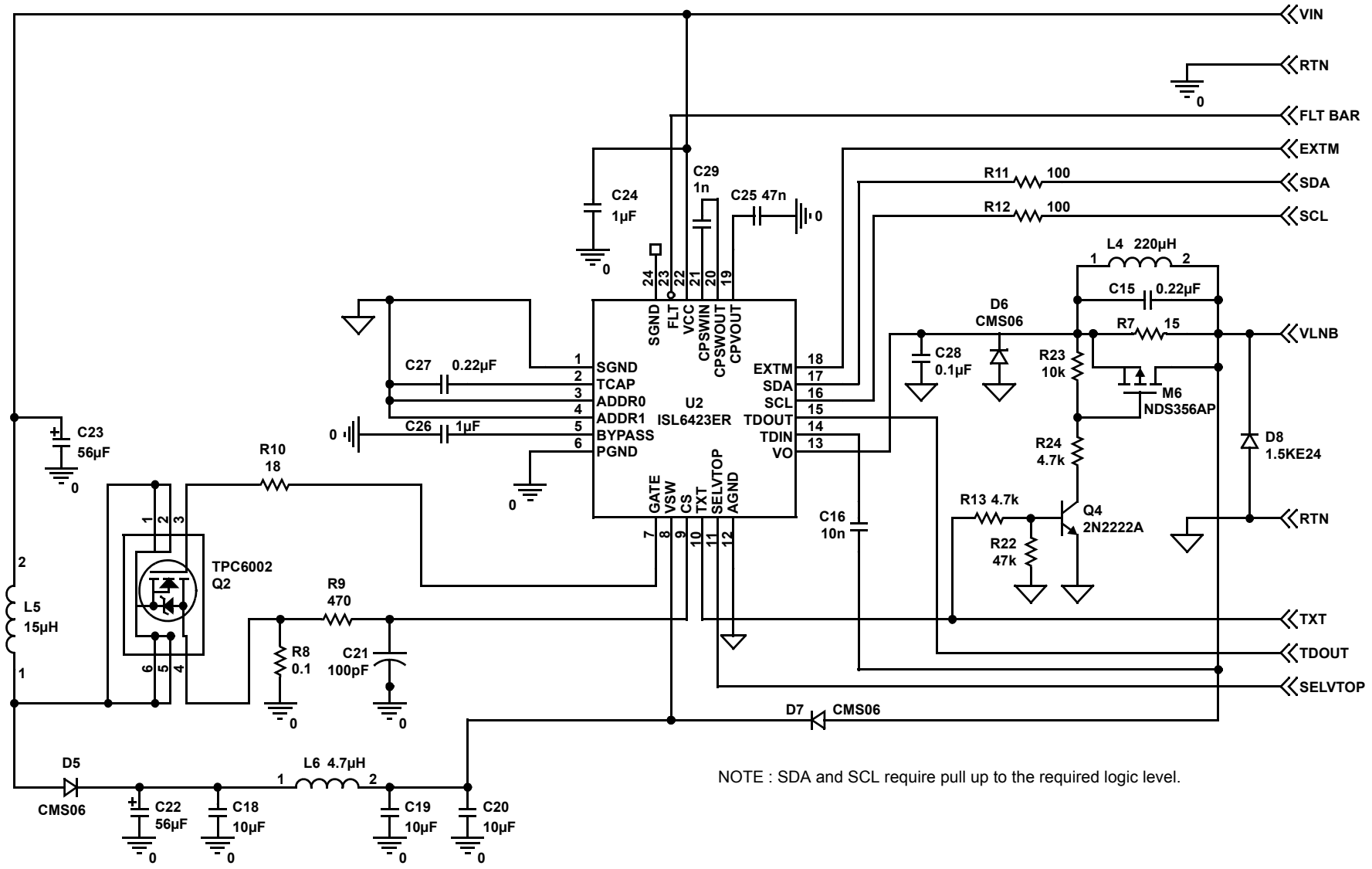
Block Diagram



NOTE:

1. Pinouts shown are for the QFN package.

Typical Application Schematic QFN



NOTE : SDA and SCL require pull up to the required logic level.

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . 8.0V to 18.0V
Logic Input Voltage Range
(SDA, SCL, ENT, DSQIN 1 and 2, SEL18V 1 and 2) . -0.5V to 7V

Thermal Information

Thermal Resistance (Typical, Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 2, 3)	38	4.5
EPTSSOP Package (Notes 2, 3)	35	2.5

Maximum Junction Temperature (Note 4) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -40°C to +150°C
Operating Temperature Range . . . . . -20°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
4. +150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Operation close to +150°C junction may trigger the shutdown of the device even before +150°C, since this number is specified as typical.

Electrical Specifications

V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN = H, VTOP VBOT = L, ENT = L, DCL = L, I_{OUT} = 12mA, unless otherwise noted. See software description section for I^2C access to the system.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			8	12	14	V
Standby Supply Current		EN = L	-	1.5	3.0	mA
Supply Current	I_{IN}	EN = VTOP = VBOT = ENT = H, No Load	-	4.0	8.0	mA
UNDERVOLTAGE LOCKOUT						
Start Threshold			7.5	-	7.95	V
Stop Threshold			7.0	-	7.55	V
Start to Stop Hysteresis			350	400	500	mV
SOFT-START						
COMP Rise Time (Note 5)		(Note 5)	-	8196	-	Cycles
Output Voltage (Note 5)	V_{O1}	(Refer to Table 1)	13.04	13.3	13.56	V
	V_{O1}	(Refer to Table 1)	14.02	14.3	14.58	V
	V_{O1}	(Refer to Table 1)	17.94	18.3	18.66	V
	V_{O1}	(Refer to Table 1)	19.00	19.3	19.68	V
Line Regulation	DV_{O1}, DV_{O2}	V_{IN} = 8V to 14V; V_O = 13.3V	-	4.0	40.0	mV
		V_{IN} = 8V to 14V; V_O = 18.3V	-	4.0	60.0	mV
Load Regulation	DV_{O1}, DV_{O2}	I_O = 0mA to 350mA	-	50	80	mV
		I_O = 0mA to 750mA	-	100	200	mV
Dynamic Output Current Limiting	I_{MAX}	DCL = 0, ISEL H = 0, ISEL L = 0 (Note 8)	275	305	345	mA
		DCL = 0, ISEL H = 0, ISEL L = 1 (Note 8)	515	570	630	mA
		DCL = 0, ISEL H = 1, ISEL L = 0 (Note 8)	635	705	775	mA
		DCL = 0, ISEL H = 1, ISEL L = 1 (Note 8)	800	890	980	mA
Dynamic Overload Protection Off Time	TOFF	DCL = 0, Output Shorted (Note 8)	-	900	-	ms
Dynamic Overload Protection On Time	TON		-	51	-	ms
Static Output Current Limiting	I_{MAX}	DCL = 1 (Note 8)	-	1000	-	mA
Cable Fault CABF Threshold	I_{CAB}	EN = 1, V_O = 19V, No Tone.	2	10	20	mA

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN = H, VTOP VBOT = L, ENT = L, DCL = L, I_{OUT} = 12mA, unless otherwise noted. See software description section for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TONE OSCILLATOR						
Tone Frequency	f_{tone}	ENT = H	20.0	22.0	24.0	kHz
Tone Amplitude	V_{tone}	ENT = H, I_O = 5mA	500	680	800	mV
Tone Duty Cycle	dc_{tone}	ENT = H,	40	50	60	%
Tone Rise or Fall Time	T_r, T_f	ENT = H,	5	10	14	µs
TONE DECODER						
Input Amplitude	Vtdin		200	-	1000	mV
Frequency Capture Range	Ftdin		17.5	-	26.5	kHz
Input Impedance	Zdet		-	8.6	-	kΩ
Detector Output Voltage	Vtdout_L	Tone Present, I_{LOAD} = 3mA	-	-	0.4	V
Detector Output Leakage	Itdout_H	Tone absent, V_O = 6V	-	-	10	µA
Tone Decoder Rx Threshold	V_{RXth}	TXT = L and TTH = 0 (Note 9)	100	150	200	mV
Tone Decoder Tx Threshold	V_{TXth}	TXT = H and TTH = 0 (Note 9)	400	450	500	mV
LINEAR REGULATOR						
Drop-out Voltage		I_{OUT} = 750mA	-	0.8	1.05	V
Output Backward Leakage Current	I_{BKLK}	EN = 0; V_{OBK} = 27V	-	2.0	3.0	mA
Output Backward Leakage Current	I_{BKLK}	EN = 0; V_{OBK} = 28V	-	3.0	17	mA
Output Backward Current Threshold	I_{BKTH}	EN = 1; V_{OFAULT} = 19V (Note 7)	-	140	-	mA
Output Backward Current Limit	I_{BKLM}	EN = 1; V_{OFAULT} = 19V (Note 7)	-	350	-	mA
Output Backward Voltage	V_{OBK}	EN = 0	-	-	27	V
Output Under Voltage (Asserted high during soft-start)		OUVF bit is asserted high, Measured from the typ. output set value	-6	-	-2	%
Output Over Voltage (Asserted high during soft-start)		OUVF bit is asserted high, Measured from the typ. output set value	+2	-	+6	%
TXT, EXTM, SELVTOP AND ADDR 0/1 INPUT PINs (Note 8)						
Asserted LOW			-	-	0.8	V
Asserted HIGH			1.7	-	-	V
Input Current			-	25	-	µA
CURRENT SENSE (CS pin)						
Input Bias Current	I_{BIAS}		-	700	-	nA
Overcurrent Threshold	V_{CS}	Static current mode, DCL = H	325	450	500	mV
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{OL}		-	93	-	dB
Gain Bandwidth Product	GBP		-	14	-	MHz
PWM						
Maximum Duty Cycle			90	93	-	%
Minimum Pulse Width			-	20	-	ns

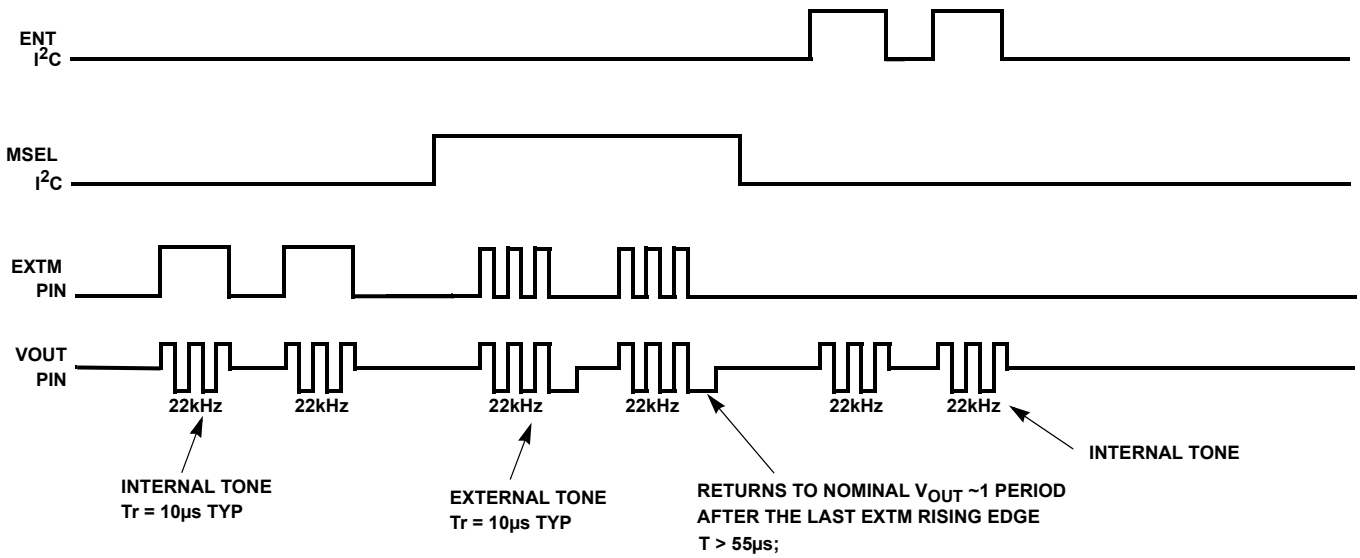
Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN = H, VTOP VBOT = L, ENT = L, DCL = L, I_{OUT} = 12mA, unless otherwise noted. See software description section for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Oscillator Frequency	f_o	Fixed at (20)(f_{tone})	396	440	484	kHz
Thermal Shutdown						
Temperature Shutdown Threshold			-	150	-	°C
Temperature Shutdown Hysteresis			-	20	-	°C
OTFI						
$\overline{FLT}$ (released)		V_O = 6V	-	-	10	µA
$\overline{FLT}$ (asserted)		I_{SINK} = 3.2mA	-	-	0.4	V

NOTES:

5. Internal digital soft-start
6. EXTM, TXT and SELVTOP and addr 0/1 pins have 200k internal pulldown resistors.
7. On exceeding this backward current limit threshold for a period of 2ms, the device enters the Backward dynamic current limit mode (350mA typ) and the BCF I^2C bit is set. The dynamic current limit duty ratio during a back current fault is ON = 2ms/OFF = 50ms. The output will remain clamped to the fault output voltage till released. On removal of the fault condition the device returns to normal operation
8. In the Dynamic current limit mode the output is ON for 51ms and OFF for 900ms. But remains continuously ON in the Static mode. When tone is ON the minimum current limit is 50mA lower the values indicated in the table.

Tone Waveform



NOTES:

9. The signal pin TXT changes the decoder threshold during tone transmit and receive. TTH allows threshold control through I^2C.
10. The tone rise and fall times are not shown due to resolution of graphics. It is 10µs typ for 22kHz.
11. The EXTM pins have input thresholds of Vil(max) = 0.8V and Vih(min) = 1.7V

FIGURE 1. TONE WAVEFORM

Typical Performance Curves

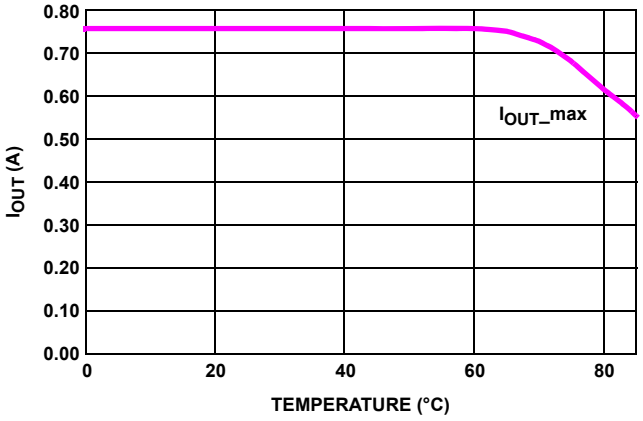


FIGURE 2. OUTPUT CURRENT DERATING (EPTSSOP)

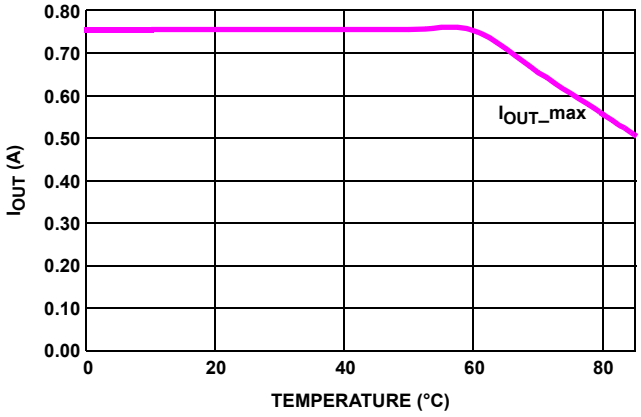


FIGURE 3. OUTPUT CURRENT DERATING (4x4 QFN)

Functional Pin Description

SYMBOL	FUNCTION
SDA	Bidirectional data from/to I^2C bus.
SCL	Clock from I^2C bus.
VSW	Input of the linear post-regulator.
PGND	Dedicated ground for the output gate driver of respective PWM.
CS	Current sense input; connect the sense resistor Rsc at this pin for desired peak overcurrent value for the boost FET. The set peak limit is effective in the static mode current limit only i.e., DCL = HIGH.
SGND	Small signal ground for the IC.
TCAP	Capacitor for setting rise and fall time of the output voltage. Typical value is 0.1µF.
BYPASS	Bypass capacitor for internal 5V.
TXT	TXT is the Tone Transmit signal input used to change the Tone Decoder Threshold from TXT = 0, 200mV max during Receive to TXT = 1, 400mV min during Transmit.
VCC	Main power supply to the chip.
GATE	This output drives the boost FET gate. The output is held low when V_{CC} is below the UVLO threshold.
VO	Output voltage for the LNB is available at VO pin.
ADDR0 & ADDR1	Logic combination at the ADDR0 & 1 can select four different chip select addresses.
EXTM	This pin can be used in two ways: 1) As an input for externally modulated Diseqc tone signal which is transferred to the symmetrically onto V_{OUT} 2) Alternatively apply a Diseqc modulation envelope which modulates an internal tone and then transfers it symmetrically onto V_{OUT}
$\overline{FLT}$	This is an Open Drain output from the controller. When the $\overline{FLT}$ goes low it indicates that an Over Temperature, Over load fault, UVLO, or an I^2C reset condition has occurred. The processor should then look at the I^2C register to get the actual cause of the error. A high on the $\overline{FLT}$ indicates that the device is functioning normally.
CPVOUT, CPSWIN CPSWOUT	A 47n charge pump decoupling capacitor is to be connected to CPVOUT. Connect a 1.5n capacitor between CPSWIN and CPSWOUT
SELVTOP	When this pin is low the V_{OUT} is in the 13V, 14V range selected by the I^2C bit VBOT. When this pin is high the 18V, 19V range selected by the I^2C bit VTOP. The Voltage select pin enable VSPEN I^2C bit must be set low for the SELVTOP pins to be active. Setting VSPEN high disables this pins and voltage selection will be done using the I^2C bits VBOT and VTOP only.
TDIN, TDOUT	TDIN is the tone decoder input and TDOUT is the tone detector output. TDOUT is an open drain output

Functional Description

The ISL6423B single output voltage regulator makes an ideal choice for advanced satellite set-top box and personal video recorder applications. The device utilizes built-in DC/DC step up converters that, operates from a single supply source ranging from 8V to 14V, and generates the voltage needed to enable the linear post-regulator to work with a minimum of dissipated power. An undervoltage lockout circuit disables the device when VCC drops below a fixed threshold (7.5V typ).

DiSEqC Encoding

The internal oscillator is factory-trimmed to provide a tone of 22kHz in accordance with DiSEqC (EUTELSAT) standards. No further adjustment is required. The tone oscillator can be controlled either by the I^2C interface (ENT bit) or by a dedicated pin (EXTM) that allows immediate DiSEqC data encoding separately for each LNB. All the functions of this IC are controlled via the I^2C bus by writing to the system registers. The same registers can be read back, and four bits will report the diagnostic status. The internal oscillator operates the converters at twenty times the 22k tone frequency. The device offers full I^2C compatibility, and supports 2.5V, 3.3V or 5V logic, up to an operational speed of 400kHz.

If the Tone Enable (ENT) bit is set LOW and the MSEL bits set LOW through I^2C, then the EXTM terminal activates the internal tone signal, modulating the DC output with a $680mV_{PP}$ typical symmetrical tone waveform. The presence of this signal usually provides the LNB with information about the band to be received.

Burst coding of the tone can be accomplished due to the fast response of the EXTM input and rapid tone response. This allows implementation of the DiSEqC (EUTELSAT) protocols.

When the ENT bit is set HIGH, a continuous 22kHz tone is generated regardless of the EXTM pin logic status for the regulator channel LNB-A. The ENT bit must be set LOW when the EXTM pin is used for DiSEqC encoding.

The EXTM accepts an externally modulated tone command when the MSEL I^2C bit is set HIGH and ENT is set LOW.

DiSEqC Decoder

TDIN is the input to the tone decoder. It accepts and the tone signal derived from the V_{OUT} thru the 10nF decoupling capacitor. The detector threshold can be set to 200mV max in the Receive mode and to 400mV min in the Transmit mode by means of the logic presented to the TXT pin. If tone is detected the open drain pin TDOUT is asserted low. This enables the tone diagnostics to be performed, apart from the normal tone detection function.

Linear Regulator

The output linear regulator will sink and source current. This feature allows full modulation capability into capacitive loads as high as 0.75µF. In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at minimum dropout.

When the device is put in the shutdown mode (EN = LOW), the PWM power block is disabled. When the regulator blocks are active (EN = HIGH and VSPEN = LOW), the output can be controlled via I^2C logic to be 13V/14V or 18V/19V (typical) by means of the VTOP and VBOT bits (Voltage Select) for remote controlling of non-DiSEqC LNBs.

When the regulator blocks are active (EN = HIGH and VSPEN = HIGH), the VBOT and SELVTOP pin will control the output between 13V and 14V and the VTOP and SELVTOP pin will control the output between 18V and 19V.

Output Timing

The output voltage rise and fall times can be set by an the external capacitor on the TCAP pin. The output rise and fall times is given by the equation:

$$C = \frac{327.6T}{\Delta V} \quad \text{(EQ. 1)}$$

Where C is the TCAP value in nF, T is the required transition time in ms and ΔV is the differential transition voltage from low output voltage range to the high output range in Volts.

The maximum recommended value for TCAP is 0.15µF. Too large a value of TCAP prevents the output from rising to the nominal value, within the soft-start time when the error amplifier is released. Too small a value of the TCAP can cause high peak currents in the boost circuit. For example, a 10V/ms slew on a 80µF VSW capacitor with an inductor of 15µH can cause a peak inductor current of approximately 2.3A.

Current Limiting

Dynamic current limiting block has four thresholds that can be selected by the ISEL H and ISEL L bits of the SR. Refer to Table 8 and Table 9 for threshold selection using these bits. The DCL bit has to be set to low for this mode of operation. In the dynamic overcurrent mode a fault exceeding the selected overcurrent threshold for a period greater than 51ms, will shutdown the output for 900ms, during which the I^2C bit OLF is set high. At the end of 900ms the OLF bit is returned to the low state, a soft-start cycle (~20ms long) is initiated to ramp VSW and V_{OUT} back up. If the fault is still present the overcurrent will be reached early in the soft-start cycle and the 51ms shutdown timer will be started again. If the fault is still present at the end of the 51ms, the OLF bit is again set high and the device once again enters the 900ms OFF time. This dynamic operation greatly reduces the power dissipation in a short circuit condition, while still ensuring excellent power-on start-up in most conditions.

However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is selected. This can be solved by initiating any power start-up in static mode (DCL = HIGH) and then switching to the dynamic mode (DCL = LOW) after a predetermined interval. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW at the end of initial power-on soft-start. In the Static mode the output current through the linears is limited to a 990mA typ.

When a 19.3V line is connected onto a VOUT1 or 2 that has been set to 13.3V the linear will then enter a back current limited state. When a back current of greater than 140mA typical is sensed at the lower FET of the linear for a period greater that 2ms the output is disabled for a period of 50ms and the BCF bit is set. If the 19.3V remains connected, the output will cycle through the ON = 2ms/OFF = 50ms. The output will return to the setpoint when the fault is removed. BCF bit is set high during the 50ms OFF period.

Thermal Protection

This IC is protected against overheating. When the junction temperature exceeds +150°C (typical), the step-up converter and the linear regulator are shut off and the OTF bit of the SR is set HIGH. When the junction is cooled down to +130°C (typical), normal operation is resumed and the OTF bit is reset LOW. If a part is repeatedly driven to the overtemp shutdown temperature the chip is latched off after the fourth occurrence and the I^2C OTF bit is latched high and FLT_bar low. This OTF counter and FLT_bar can be reset and the chip restarted by either a power down/up and reload the I^2C or power can be left on and the reset accomplished by toggling the I^2C bit EN low then back high.

External Output Voltage Selection

When the I^2C bit VSPEN is set high the output voltage can be selected by the I^2C bus. Additionally, the package offers the pin SELVTOP for independent 13 thru 19V output voltage selection., when the VSPEN bit is set low. A summary of the voltage control is given in Table 1. For further details refer to the individual registers SR1 and SR3

TABLE 1.

VSPEN	VTOP	VBOT	SELVTOP	VOUT
0	x	0	0	13.3V
0	x	1	0	14.3V
0	0	x	1	18.3V
0	1	x	1	19.3V
1	0	0	x	13.3V
1	0	1	x	14.3V
1	1	0	x	18.3V
1	1	1	x	19.3V

I^2C Bus Interface for ISL6423B

(Refer to Philips I^2C Specification, Rev. 2.1)

Data transmission from main microprocessor to the ISL6423B and vice versa takes place through the two wire I^2C bus interface, consisting of the two lines SDA and SCL. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor. (Pull up resistors to positive supply voltage must be externally connected). When the bus is free, both lines are HIGH. The output stages of ISL6423B will have an open drain/open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred up to 100Kbps in the standard-mode or up to 400Kbps in the fast-mode. The level of logic “0” and logic “1” is dependent of associated value of V_{DD} as per electrical specification table. One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 4.

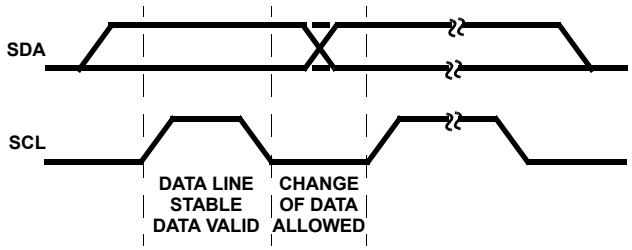


FIGURE 4. DATA VALIDITY

START and STOP Conditions

As shown in Figure 5, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

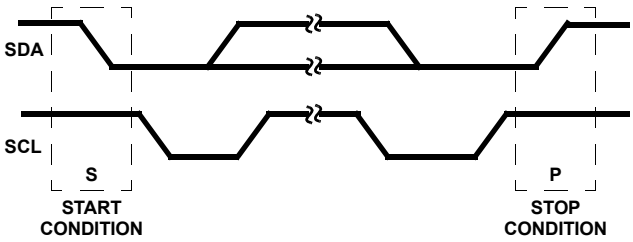


FIGURE 5. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (Figure 6). The peripheral that acknowledges has to pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Of course, set-up and hold times must also be taken into account.)

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer. The ISL6423B will not generate the acknowledge if the POWER OK signal from the UVLO is LOW.

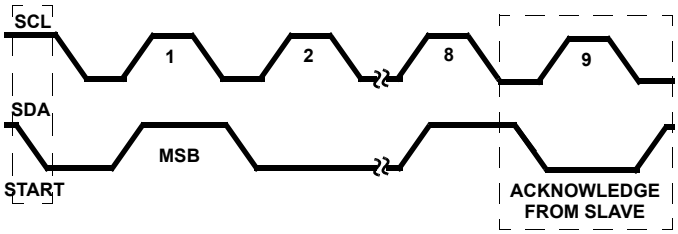


FIGURE 6. ACKNOWLEDGE ON THE I^{2}C BUS

Transmission Without Acknowledge

Avoiding detection of the acknowledgement, the microprocessor can use a simpler transmission; it waits one clock without checking the slave acknowledging, and sends the new data.

This approach, though, is less protected from error and decreases the noise immunity.

ISL6423B Software Description

Interface Protocol

The interface protocol is comprised of the following, as shown below in Table 2:

- A start condition (S)
- A chip address byte (MSB on left; the LSB bit determines read (1) or write (0) transmission) (the assigned I^{2}C slave address for the ISL6423B is 0001 0**XX**X)
- A sequence of data (1 byte + Acknowledge)
- A stop condition (P)

TABLE 2. INTERFACE PROTOCOL

S	0	0	0	1	0	A1	A0	R/W	ACK	Data (8 bits)	ACK	P

System Register Format

- R, W = Read and Write bit
- R = Read-only bit

All bits reset to 0 at Power-On

TABLE 3. STATUS REGISTER (SR1)

R, W	R, W	R, W	R	R	R	R	R
SR1H	SR1M	SR1L	OTF	CABF	OUVF	OLF	BCF

TABLE 4. TONE REGISTER (SR2)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR2H	SR2M	SR2L	ENT	MSEL	TTH	X	X

TABLE 5. COMMAND REGISTER (SR3)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR3H	SR3M	SR3L	DCL	VSPEN	X	ISELH	ISELL

TABLE 6. CONTROL REGISTER (SR4)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR4H	SR4M	SR4L	EN			VTOP	VBOT

Transmitted Data (I^{2}C bus WRITE mode)

When the R/W bit in the chip is set to 0, the main microprocessor can write on the system registers (SR2 thru SR4) of the ISL6423B via I^{2}C bus. These will be written by the microprocessor as shown below. The spare bits of registers can be used for other functions.

TABLE 7. STATUS REGISTER SR1 CONFIGURATION

SR1H	SR1M	SR1L	OTF	CABF	OUVF	OLF	BCF	FUNCTION
0	0	0	X	X	X	X	X	SR1 is selected
0	0	0	X	X	X	0	X	$I_{OUT} \leq$ set limit, Normal Operation
0	0	0	X	X	X	1	X	I_{OUT} > Static/Dynamic Limiting Mode/Power blocks disabled
0	0	0	X	X	X	X	0	Iobck ≤ set limit, Normal Operation
0	0	0	X	X	X	X	1	Iobck > Dynamic Limiting Mode / Power blocks disabled
0	0	0	X	X	0	X	X	V_{IN}/V_{OUT} within specified range
0	0	0	X	X	1	X	X	V_{IN}/V_{OUT} is not within specified range
0	0	0	X	0	X	X	X	Cable is connected, Io is >20mA
0	0	0	X	1	X	X	X	Cable is open, Io <2mA
0	0	0	0	X	X	X	X	$T_J \leq$130°C, Normal operation
0	0	0	1	X	X	X	X	T_J >150°C, Power blocks disabled

TABLE 8. TONE REGISTER SR2 CONFIGURATION

SR2H	SR2M	SR2L	ENT	MSEL	TTH	X	X	FUNCTION
0	0	1	X	X	X	X	X	SR2 is selected
0	0	1	0	0	X	X	X	Int Tone = 22kHz, modulated by EXTM, T_r, T_f = 10µs typ
0	0	1	0	1	X	X	X	Ext 22k modulated input, T_r, T_f = 10µs typ
0	0	1	1	0	X	X	X	Int Tone = 22kHz, modulated by ENT bit, T_r, T_f = 10µs typ
0	0	1	X	X	0	X	X	TXT = 0; Decoder Rx threshold is set at 200mV max
0	0	1	X	X	1	X	X	TXT = 0; Decoder Tx threshold is set at 400mV min

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode.

TABLE 9. COMMAND REGISTER SR3 CONFIGURATION

SR3H	SR3M	SR3L	DCL	VSPEN	X	ISELH	ISELL	FUNCTION
0	1	0	X	X	X	X	X	SR3 is selected
0	1	0	0	X	X	0	0	I_{OUT} limit threshold = 305mA typ.
0	1	0	0	X	X	0	1	I_{OUT} limit threshold = 570mA typ.
0	1	0	0	X	X	1	0	I_{OUT} limit threshold = 705mA typ.
0	1	0	0	X	X	1	1	I_{OUT} limit threshold = 890mA typ.
0	1	0	1	X	X	X	X	Dynamic current limit NOT selected
0	1	0	0	X	X	X		Dynamic current limit selected
0	1	0	X	0	X	X	X	SELVTOP H/W pin Enabled
0	1	0	X	1	X	X	X	SELVTOP H/W pin Disabled

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode.

TABLE 10. CONTROL REGISTER SR4 CONFIGURATION

SR4H	SR4M	SR4L	EN	X	X	VTOP	VBOT	FUNCTION
0	1	1	1	X	X	0	0	SR4 is selected
0	1	1	1	X	X	0	0	VSPEN = SELVTOP = 0, V_{OUT} = 13V, V_{BOOST} = 13V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN = SELVTOP = 0, V_{OUT} = 14V, V_{BOOST} = 14V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN = SELVTOP = 0, V_{OUT} = 13V, V_{BOOST} = 13V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN = SELVTOP = 0, V_{OUT} = 14V, V_{BOOST} = 14V + V_{DROP}
0	1	1	1	X	X	0	0	VSPEN = 0,SELVTOP = 1, V_{OUT} = 18V, V_{BOOST} = 18V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN = 0,SELVTOP = 1, V_{OUT} = 18V, V_{BOOST} = 18V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN = 0,SELVTOP = 1, V_{OUT} = 19V, V_{BOOST} = 19V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN = 0,SELVTOP = 1, V_{OUT} = 19V, V_{BOOST} = 19V + V_{DROP}
0	1	1	1	X	X	0	0	VSPEN = 1,SELVTOP = X V_{OUT} = 13V, V_{BOOST} = 13V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN = 1,SELVTOP = X V_{OUT} = 14V, V_{BOOST} = 14V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN = 1,SELVTOP = X V_{OUT} = 18V, V_{BOOST} = 18V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN = 1,SELVTOP = X V_{OUT} = 19V, V_{BOOST} = 19V + V_{DROP}
0	1	1	0	X	X	X	X	PWM and Linear for channel 1 disabled

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode.

Received Data (I²C bus READ MODE)

The ISL6423B can provide to the master a copy of the system register information via the I²C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following Master generated clock bits, the ISL6423B issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the ISL6423B.
- Not acknowledge, stopping the read mode communication.

The read only bits of the register SR1 convey diagnostic information about the ISL6423B, as indicated in the Table 7.

Power–On I²C Interface Reset

The I²C interface built into the ISL6423B is automatically reset at power-on. The I²C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I²C commands and the system register SR1 thru SR4 are all initialized to all zero, thus keeping the power blocks disabled. Once the V_{CC} rises above UVLO, the POWER OK signal to the I²C is asserted high, and the I²C interface becomes operative and the SR’s can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the Power-On reset circuit. (I²C comes up with EN = 0; EN goes HIGH at the same time as (or later than) all other I²C data for that PWM becomes valid).

ADDR0 and ADDR1 Pins

Connecting these pin to GND the chip I²C interface address is 0001000, but, it is possible to choose between four different addresses by setting these pins to the logic levels indicated in Table 11.

TABLE 11. ADDRESS PIN CHARACTERISTICS

V_{ADDR}	ADDR1	ADDR0
V_{ADDR}-1 “0001000”	0	0
V_{ADDR}-2 “0001001”	0	1
V_{ADDR}-3 “0001010”	1	0
V_{ADDR}-4 “0001011”	1	1

I^2C Bit Description

BIT NAME	DESCRIPTION
EN	ENable Output for channels 1 and 2
VTOP	Voltage TOP select i.e. 18V, 19V for channels 1 and 2
VBOT	Voltage BOTtom select i.e. 13V, 14V for channels 1 and 2
ENT	ENable Tone
MSEL	Modulation SELect
DCL	Dynamic Current Limit select
VSPEN	Voltage Select Pin ENable
ISELH and ISELL	Current limit “I” SELect High and Low bit
OTF	Over Temperature Fault bit
CABF	CABle Fault or open status bit
OUVF	Over and Under Voltage Fault status bit
OLF	Over Load Fault status bit
BCF	Backward Current Fault bit
TTH	Tone THreshold is the OR of the signal pin TXT

I^2C Electrical Characteristics

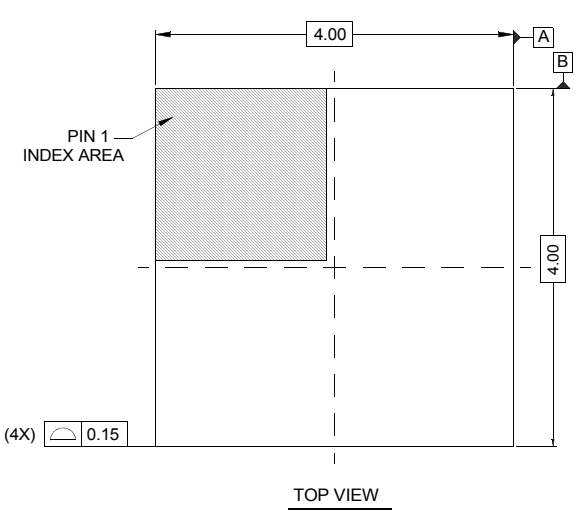
TABLE 12.

PARAMETER	TEST CONDITION	MIN	TYP	MAX
Input Logic High, VIH	SDA, SCL	2.0V		
Input Logic Low, VIL	SDA, SCL			0.8V
Input Logic Current, IIL	SDA, SCL; $0.4V < V_{DD} < 3.3V$			10µA
Input Logic Current IOL	VOL = 0.4V	3mA		
Input Hysteresis	SDA, SCL	165mV	200mV	235mV
SCL Clock Frequency		0	100kHz	400kHz
Input Filter Spike reject			50ns	

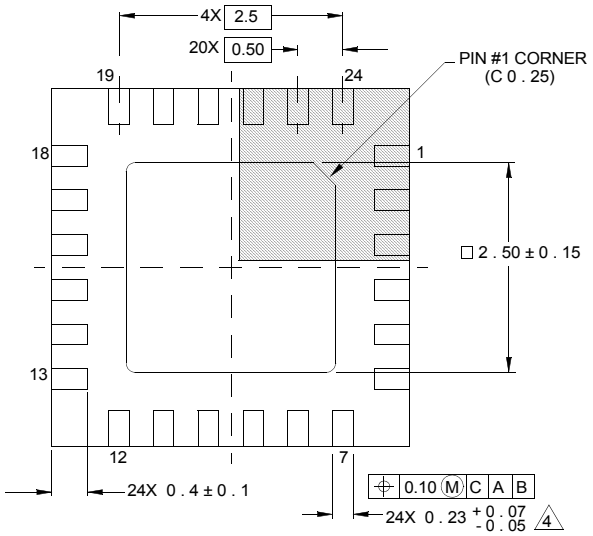
Package Outline Drawing

L24.4x4D

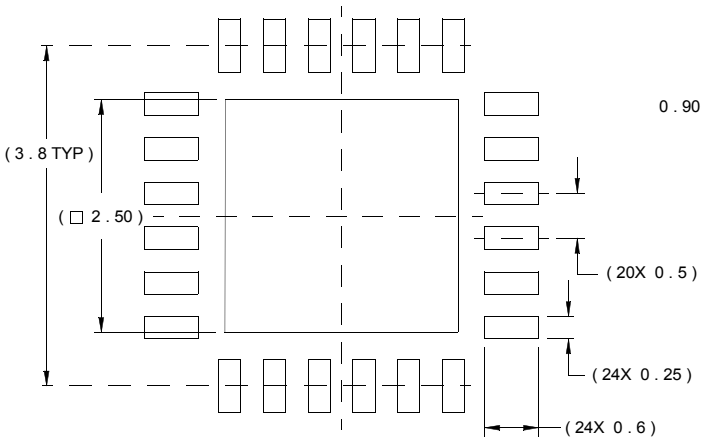
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



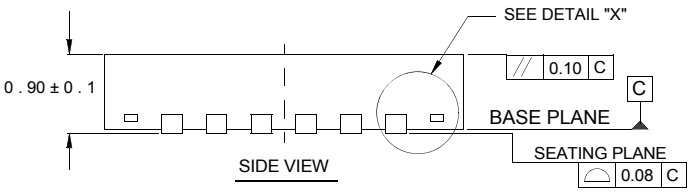
TOP VIEW



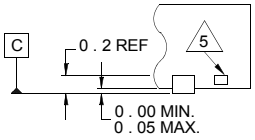
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

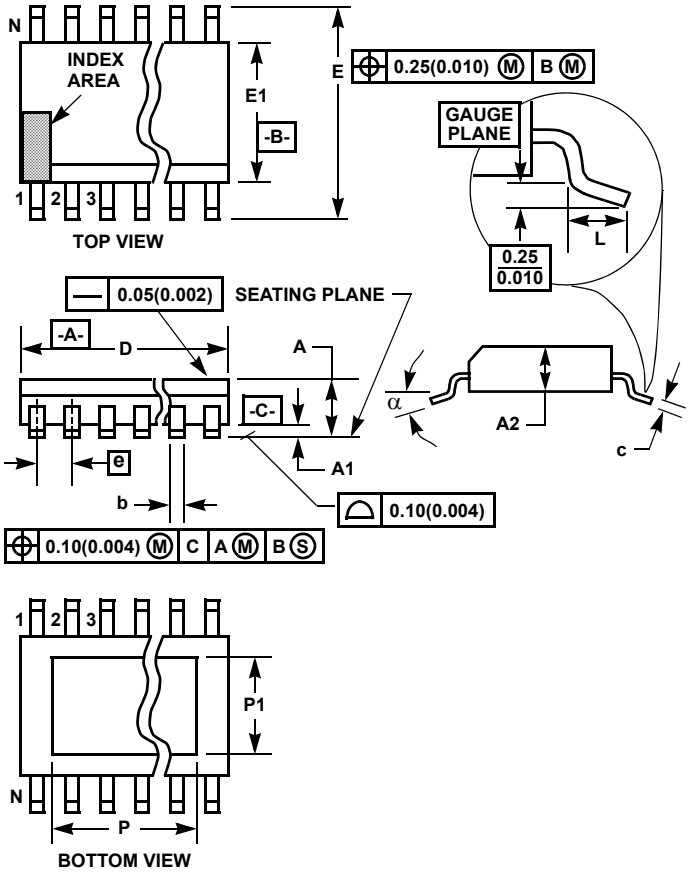


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Thin Shrink Small Outline Exposed Pad Plastic Packages (EPTSSOP)



M28.173B

28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	28		28		7
α	0°	8°	0°	8°	-
P	-	0.138	-	5.50	11
P1	-	0.118	-	3.0	11

Rev. 0 6/05

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AET, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.