Data Sheet | October 2001 | File Number 9041

Advanced PWM and Triple Linear Power Controller for Gateway Applications

The ISL6440A provides the power control and protection for four output voltages required by microprocessors used in high-performance, graphics-intensive gateway applications. The IC integrates a voltage-mode PWM controller and three linear controllers, as well as the monitoring and protection functions into a 28 lead SOIC package.

The synchronous rectified buck converter includes an Intel®-compatible, TTL five-input, digital-to-analog converter (DAC) that adjusts the core PWM output voltage from $1.3V_{DC}$ to $2.05V_{DC}$ in 0.05V steps and from $2.1V_{DC}$ to $3.5V_{DC}$ in 0.1V increments. The precision reference and voltage-mode control provide ±1% static regulation. A TTL-compatible signal applied to the SELECT pin dictates which method of control is used for the AGP bus power. A low state results in linear control of the AGP bus to 1.5V, while a high state transitions the output through a linearly controlled soft-start to 3.3V, followed by full enhancement of the external MOSFET to pass the input voltage. The other two linear regulators provide fixed output voltages of 1.5V GTL bus power and 1.8V power for the north/south bridge core and/or cache memory. These levels are user-adjustable by means of an external resistor divider and pulling the FIX pin low. All linear controllers can employ either N-Channel MOSFETs or bipolar NPNs for the pass transistor.

The ISL6440A monitors all the output voltages. A single power good signal is issued when the core is within ±10% of the DAC setting and all other outputs are above their under-voltage levels. Additional built-in overvoltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controller's overcurrent function monitors the output current by using the voltage drop across the upper MOSFET's $r_{DS(ON)}$.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ISL6440ACB	0 to 70	28 Ld SOIC	M28.3

Features

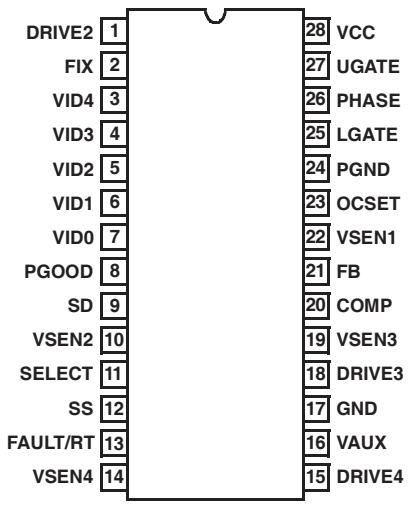
- Provides four regulated voltages
  - Microprocessor core, AGP bus, memory, and GTL bus power
- Drives N-Channel MOSFETs
- Linear regulator drives compatible with both MOSFET and bipolar series pass transistors
- Fixed or externally resistor-adjustable linear outputs
- Simple single-loop control design
  - Voltage-mode PWM control
- Fast PWM converter transient response
  - High-bandwidth error amplifier
  - Full 0–100% duty ratio
- Excellent output voltage regulation
  - Core PWM output: ±1% over temperature
  - Other outputs: ±3% over temperature
- TTL-compatible 5-bit DAC core output voltage selection
  - Shutdown feature removed when all inputs high
  - Wide range $1.3V_{DC}$ to $3.5V_{DC}$
- Power-good output voltage monitor
- Overvoltage and overcurrent fault monitors
  - Switching regulator does not require extra current Sensing element, uses upper MOSFET's $r_{DS(ON)}$
- Small converter size
  - Constant frequency operation
  - 200kHz free-running oscillator; programmable from 50kHz to over 1MHz
  - Small external component count

Applications

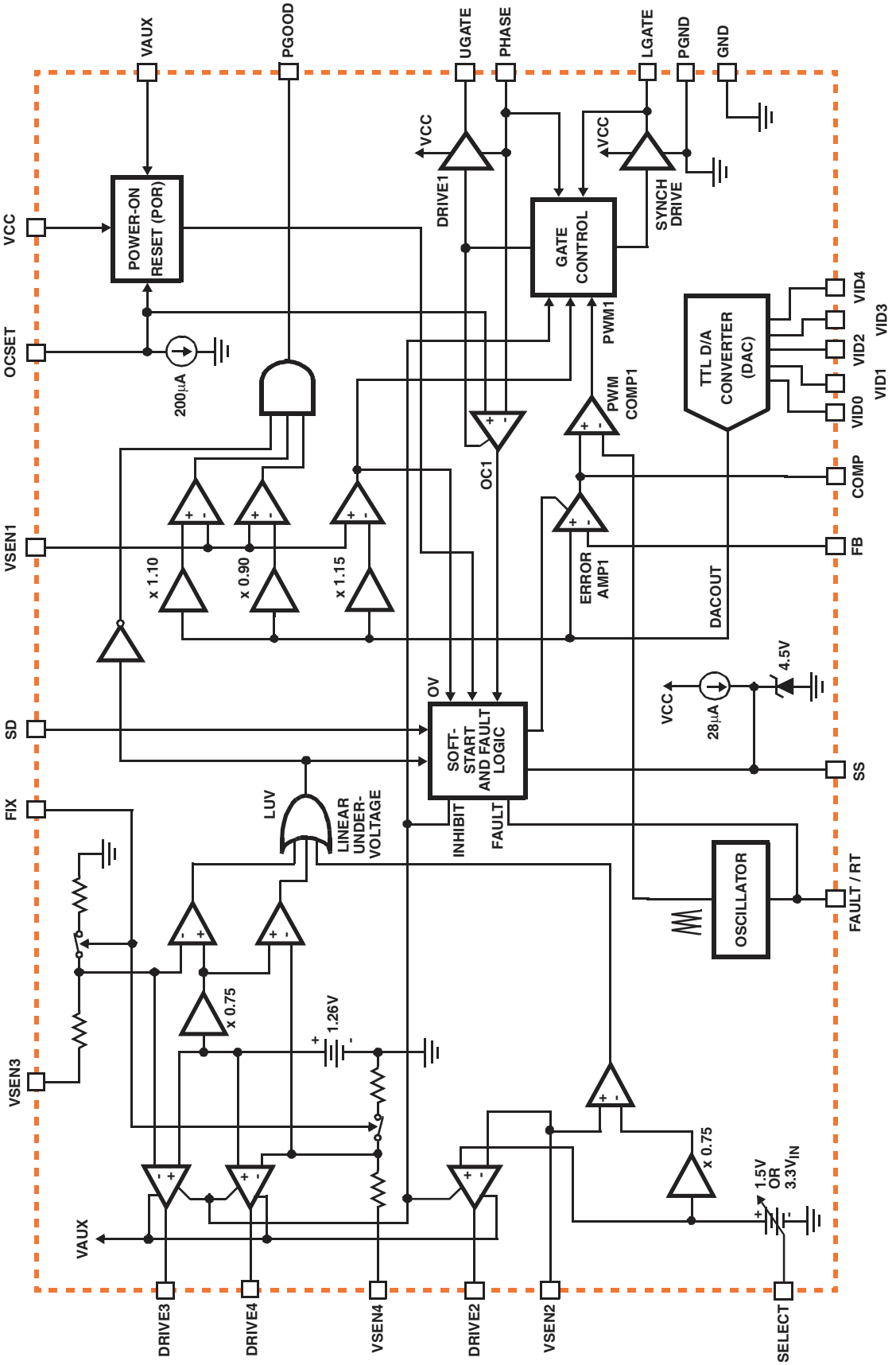
- Power regulation for gateway processors

Pinout

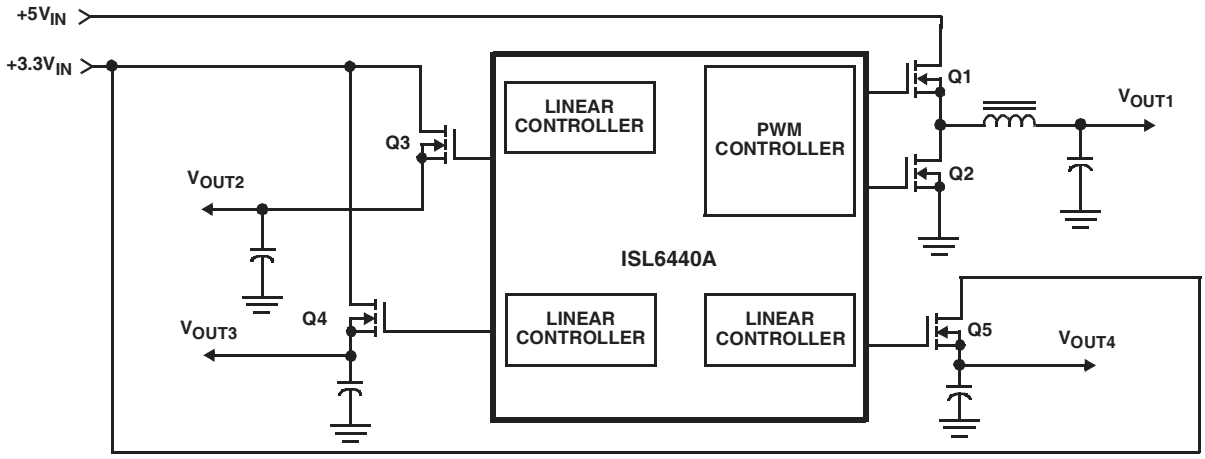
ISL6440A (SOIC)
TOP VIEW



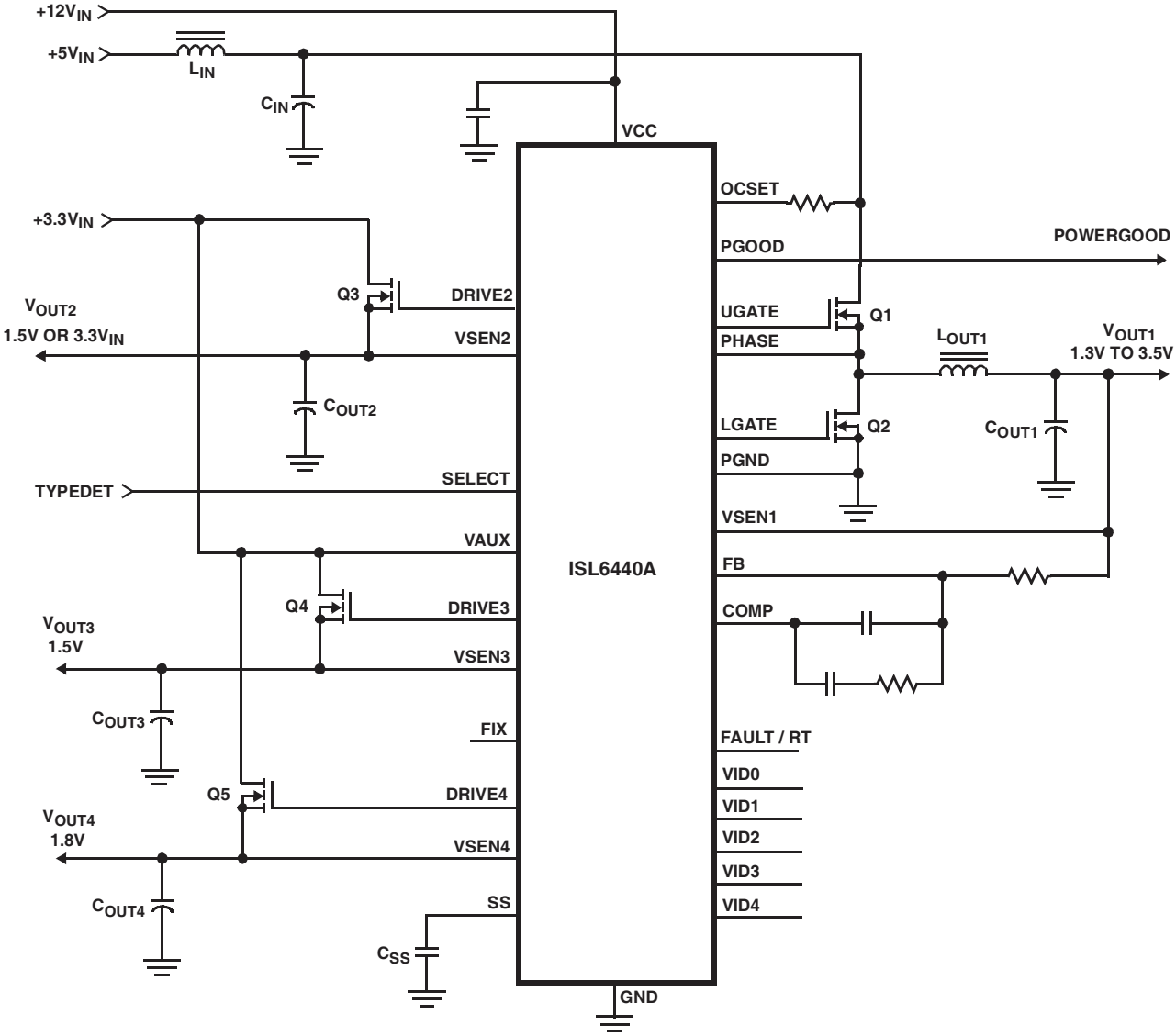
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
PGOOD, RT/FAULT, DRIVE, PHASE,
and GATE Voltage . . . . . GND -0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . GND -0.3V to 7V
ESD Classification . . . . . Class 1

Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOIC Package 45
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications — Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE, LGATE, DRIVE2, DRIVE3, and DRIVE4 Open	-	9	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	-	-	10.4	V
Falling VCC Threshold		V_{OCSET} = 4.5V	8.2	-	-	V
Rising VAUX Threshold		V_{OCSET} = 4.5V	-	2.5	-	V
VAUX Threshold Hysteresis		V_{OCSET} = 4.5V	-	0.5	-	V
Rising V_{OCSET} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency	F_{OSC}	RT = OPEN	185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	V_{P-P}
DAC AND BANDGAP REFERENCE						
DAC(VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC(VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
Bandgap Reference Voltage	V_{BG}		-	1.265	-	V
Bandgap Reference Tolerance			-2.5	-	+2.5	%
LINEAR REGULATORS (OUT2, OUT3, AND OUT4)						
Regulation (All Linears)		Except OUT2 when SELECT > 2.0V	-	3	-	%
VSEN2 Regulation Voltage	$VREG_2$	SELECT < 0.8V	-	1.5	-	V
VSEN3 Regulation Voltage	$VREG_3$		-	1.5	-	V
VSEN4 Regulation Voltage	$VREG_4$		-	1.8	-	V
Undervoltage Level (VSEN/VREG)	$VSEN_{UV}$	VSEN Rising	-	75	-	%
Undervoltage Hysteresis (VSEN/VREG)		VSEN Falling	-	7	-	%
Output Drive Current (All Linears)		VAUX-V_{DRIVE} > 0.6V	20	40	-	mA
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC Gain			-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR	COMP = 10pF	-	6	-	V/μs
PWM CONTROLLER GATE DRIVER						
UGATE Source	I_{UGATE}	VCC = 12V, V_{UGATE} = 6V	-	1	-	A
UGATE Sink	R_{UGATE}	$V_{GATE-PHASE}$ = 1V	-	1.7	3.5	Ω
LGATE Source	I_{LGATE}	VCC = 12V, V_{LGATE} = 1V	-	1	-	A
LGATE Sink	R_{LGATE}	V_{LGATE} = 1V	-	1.4	3.0	Ω
PROTECTION						
VSEN1 Overvoltage (VSEN1/DACOUT)		VSEN1 Rising	-	115	120	%
FAULT Sourcing Current	I_{OVP}	$V_{FAULT/RT}$ = 2.0V	-	8.5	-	mA
OCSET1 Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	μA
Soft-Start Current	I_{SS}		-	28	-	μA
POWER GOOD						
VSEN1 Upper Threshold (VSEN1/DACOUT)		VSEN1 Rising	108	-	110	%
VSEN1 Undervoltage (VSEN1/DACOUT)		VSEN1 Rising	92	-	94	%
VSEN1 Hysteresis (VSEN1/DACOUT)		Upper/Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.8	V

Typical Performance Curve

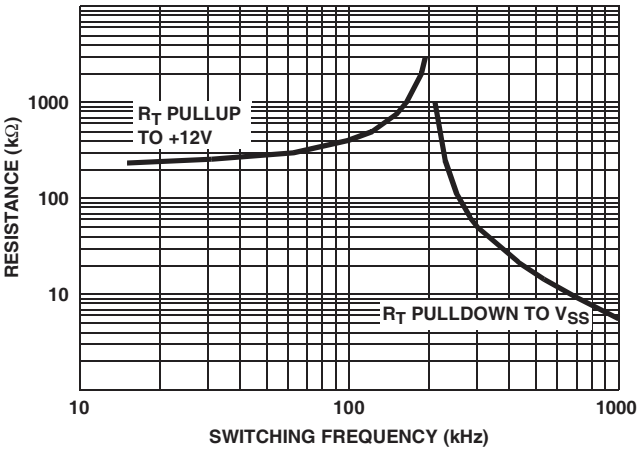


FIGURE 1. R_T RESISTANCE vs FREQUENCY

Functional Pin Descriptions

VCC (Pin 28)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for power-on reset (POR) purposes.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

VAUX (Pin 16)

This pin provides boost current for the linear regulators' output drives in the event bipolar NPN transistors (instead of N-Channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for POR purposes.

SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28µA current source, sets the soft-start interval of the converter.

FAULT / RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \times 10^6}{R_T(k\Omega)} \qquad (R_T \text{ to GND})$$

Conversely, connecting a resistor from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \times 10^7}{R_T(k\Omega)} \qquad (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V. In the event of an overvoltage or overcurrent condition, this pin is internally pulled to VCC.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage or when any of the other outputs are below their undervoltage thresholds.

The PGOOD output is open for '11111' VID code.

SD (Pin 9)

This pin shuts down all the outputs. A TTL-compatible, logic level high signal applied at this pin immediately discharges the soft-start capacitor, disabling all the outputs. Dedicated internal circuitry insures the core output voltage does not go negative during this process. When re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

FIX (Pin 2)

Grounding this pin bypasses the internal resistor dividers that set the output voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.26V up to the input voltage (+3.3V or +5V) by way of an external resistor divider connected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where R_{OUT} is the resistor connected from VSEN to the output of the regulator, and R_{GND} is the resistor connected from VSEN to ground. Left open, the FIX pin is pulled high, enabling fixed output voltage operation.

VID0, VID1, VID2, VID3, VID4 (Pins 7, 6, 5, 4 and 3)

VID0-4 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds.

OCSET (Pin 23)

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200µA current source, and the upper MOSFET's on-resistance set the converter overcurrent trip point. An overcurrent trip cycles the soft-start function.

The voltage at this pin is monitored for POR purposes and pulling this pin low with an open drain device will shutdown the IC.

PHASE (Pin 26)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

UGATE (Pin 27)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

LGATE (Pin 25)

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

COMP and FB (Pin 20 and 21)

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the

error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 22)

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for overvoltage protection.

DRIVE2 (Pin 1)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the AGP regulator's pass transistor.

VSEN2 (Pin 10)

Connect this pin to the output of the AGP linear regulator. The voltage at this pin is regulated to the level predetermined by the logic-level status of the SELECT pin. This pin is also monitored for undervoltage events.

SELECT (Pin 11)

This pin determines the output voltage of the AGP bus linear regulator. A low TTL input sets the output voltage to 1.5V and the linear controller regulates this voltage to within ±3%.

A TTL high input turns Q3 on continuously, providing a DC current path from the input ($+3.3V_{IN}$) to the output (V_{OUT2}) of the AGP controller.

DRIVE3 (Pin 18)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.5V regulator's pass transistor.

VSEN3 (Pin 19)

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for undervoltage events.

DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.8V regulator's pass transistor.

VSEN4 (Pin 14)

Connect this pin to the output of the linear 1.8V regulator. This pin is monitored for under voltage events.

Description

Operation

The ISL6440A monitors and precisely controls 4 output voltage levels (Refer to *Block* and *Simplified Power System Diagrams*, and *Typical Application Schematic*). It is designed for microprocessor computer applications with 3.3V, 5V, and 12V bias input from an ATX power supply. The microprocessor core voltage (V_{OUT1}) is controlled in a synchronous rectified buck converter configuration. The PWM controller regulates the microprocessor core voltage to a level programmed by the 5-bit digital-to-analog converter (DAC).

The AGP bus voltage (VOUT2) is set using the SELECT pin to either a 1.5V linear regulated output or to the $3.3V_{IN}$ through a pass device. Selection of either output voltage is set depending on the logic level of the SELECT pin.

The two remaining linear controllers supply the 1.5V GTL bus power (V_{OUT3}) and the 1.8V memory power (V_{OUT4}). These output voltages are user adjustable. All linear controllers are designed to employ an external pass transistor.

Initialization

The ISL6440A automatically initializes upon receipt of input power. Special sequencing of the input supplies is not necessary. The POR function continually monitors the input supply voltages. The POR monitors the bias voltage ($+12V_{IN}$) at the VCC pin, the 5V input voltage ($+5V_{IN}$) on the OCSET pin, and the 3.3V input voltage ($+3.3V_{IN}$) at the VAUX pin. The normal level on OCSET is equal to $+5V_{IN}$ less a fixed voltage drop (see overcurrent protection). The POR function initiates soft-start operation after all supply voltages exceed their POR thresholds.

Soft-Start

The POR function initiates the soft-start sequence. Initially, the voltage on the SS pin rapidly increases to approximately 1V (this minimizes the soft-start interval). Then an internal 28µA current source charges an external capacitor (C_{SS}) on the SS pin to 4.5V. The PWM error amplifier reference input (+ terminal) and output (COMP pin) are clamped to a level proportional to the SS pin voltage. As the SS pin voltage slews from 1V to 4V, the output clamp allows generation of PHASE pulses of increasing width that charge the output capacitor(s). After the output voltage increases to approximately 70% of the set value, the reference input clamp slows the output voltage rate-of-rise and provides a smooth transition to the final set voltage. Additionally, all linear regulators' reference inputs are clamped to a voltage proportional to the SS pin voltage. This method provides a rapid and controlled output voltage rise.

Figure 2 shows the soft-start sequence for the typical application. At t0 the SS voltage rapidly increases to approximately 1V. At t1, the SS pin and error amplifier output voltage reach the valley of the oscillator's triangle wave. The oscillator's triangular waveform is compared to the clamped error amplifier output voltage. As the SS pin voltage increases, the pulse width on the PHASE pin increases. The interval of increasing pulse width continues until each output reaches sufficient voltage to transfer control to the input reference clamp. If we consider the 2.5V core output (V_{OUT1}) in Figure 2, this time occurs at t2. During the interval between t2 and t3, the error amplifier reference ramps to the final value and the converter regulates the output a voltage proportional to the SS pin voltage. At t3 the input clamp voltage exceeds the reference voltage and the output voltage is in regulation.

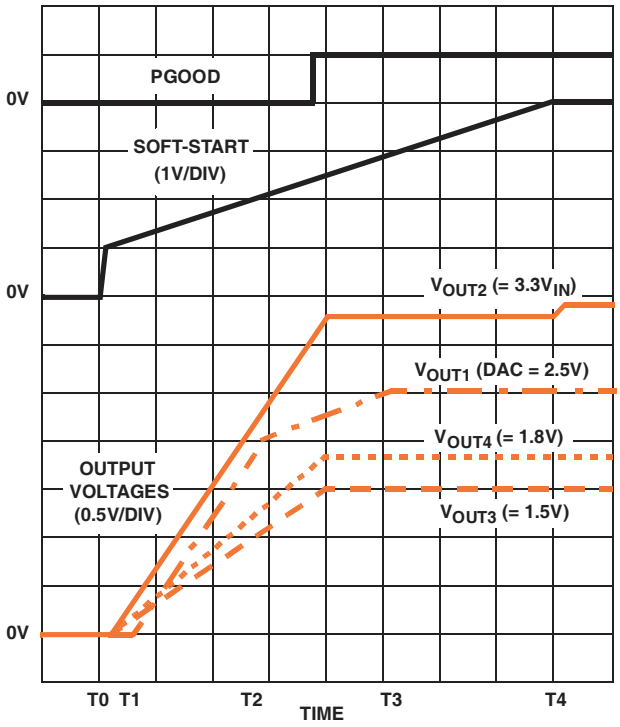


FIGURE 2. SOFT-START INTERVAL

The remaining outputs are also programmed to follow the SS pin voltage. The PGOOD signal toggles 'high' when all output voltage levels have exceeded their undervoltage levels. The waveform for V_{OUT2} represents the case where SELECT is held 'high'. The AGP bus voltage is controlled in the same manner as the other linear regulators during the soft-start sequence. Once the soft-start sequence is complete (t4), the gate of the external pass device is fully enhanced and V_{OUT2} tracks the $3.3V_{IN}$ voltage. See the *Soft-Start Interval* section under *Applications Guidelines* for a procedure to determine the soft-start interval.

Fault Protection

All four outputs are monitored and protected against extreme overload. A sustained overload on any output or an overvoltage on V_{OUT1} output (VSEN1) disables all outputs and drives the FAULT/RT pin to VCC.

Figure 3 shows a simplified schematic of the fault logic. An overvoltage detected on VSEN1 immediately sets the fault latch. A sequence of three overcurrent fault signals also sets the fault latch. The overcurrent latch is set dependent upon the states of the overcurrent (OC), linear undervoltage (LUV) and the soft-start signals. A window comparator monitors the SS pin and indicates when C_{SS} is fully charged to 4V (UP signal). An undervoltage on either linear output (VSEN2, VSEN3, or VSEN4) is ignored until after the soft-start interval (t4 in Figure 2). This allows V_{OUT2}, V_{OUT3}, and V_{OUT4} to increase without fault at start-up. Cycling the bias input voltage (+12V_{IN} on the VCC pin off, then on) resets the counter and the fault latch.

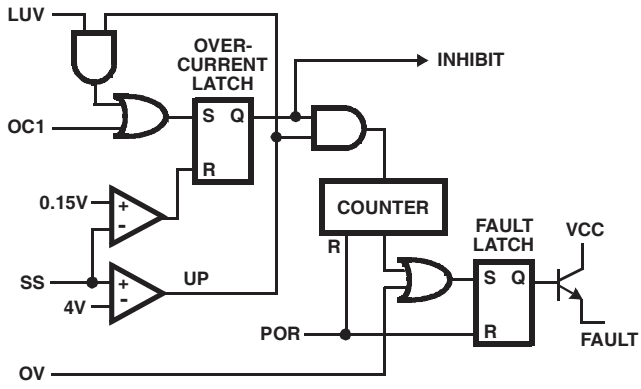


FIGURE 3. FAULT LOGIC - SIMPLIFIED SCHEMATIC

Overvoltage Protection

During operation, a short on the upper MOSFET of the PWM regulator (Q1) causes V_{OUT1} to increase. When the output exceeds the overvoltage threshold of 115% of DACOUT, the overvoltage comparator trips to set the fault latch and turns Q2 on. This blows the input fuse and reduces V_{OUT1}. The fault latch raises the FAULT/RT pin to VCC.

A separate overvoltage circuit provides protection during the initial application of power. For voltages on the VCC pin below the POR (and above ~4V), the output level is monitored for voltages above 1.3V. Should VSEN1 exceed this level, the lower MOSFET, Q2 is driven on.

Overcurrent Protection

All outputs are protected against excessive overcurrents. The PWM controller uses the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current for protection against shorted output. All linear controllers monitor their respective VSEN pins for undervoltage events to protect against excessive currents.

Figure 4 illustrates the overcurrent protection with an overload on OUT1. The overload is applied at T0 and the current increases through the inductor (L_{OUT1}). At time t1, the OVERCURRENT comparator trips when the voltage across Q1 ($i_D \bullet r_{DS(ON)}$) exceeds the level programmed by ROCSET. This inhibits all outputs, discharges the soft-start capacitor (C_{SS}) with a 10mA current sink, and increments the counter. C_{SS} recharges at t2 and initiates a soft-start cycle with the error amplifiers clamped by soft-start. With OUT1 still overloaded, the inductor current increases to trip the overcurrent comparator. Again, this inhibits all outputs, but the soft-start voltage continues increasing to 4V before discharging. The counter increments to 2. The soft-start cycle repeats at t3 and trips the overcurrent comparator. The SS pin voltage increases to 4V at t4 and the counter increments to 3. This sets the fault latch to disable the converter. The fault is reported on the FAULT/RT pin.

The linear controllers operate in the same way as the PWM in response to overcurrent faults. The differentiating factor

for the linear controllers is that they monitor the VSEN pins for undervoltage events. Should excessive currents cause the voltage at the VSEN pins to fall below the linear undervoltage threshold, the LUV signal sets the overcurrent latch if C_{SS} is fully charged. Blanking the LUV signal during the C_{SS} charge interval allows the linear outputs to build above the undervoltage threshold during normal operation. Cycling the bias input power off then on resets the counter and the fault latch.

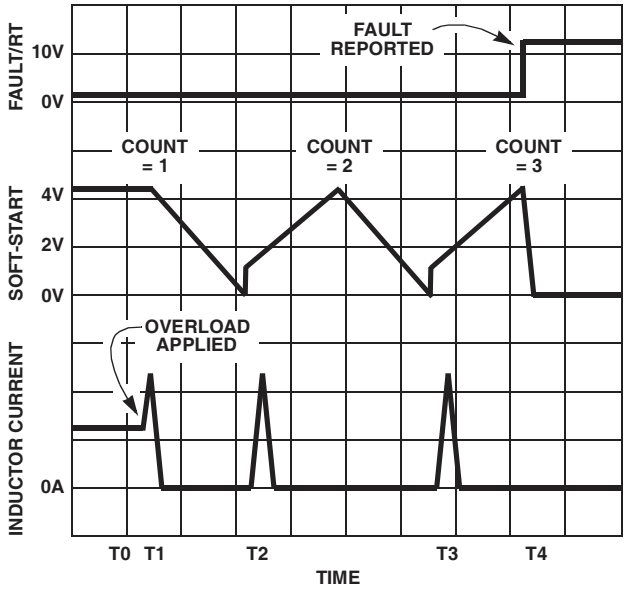


FIGURE 4. OVERCURRENT OPERATION

A resistor (R_{OCSET}) programs the overcurrent trip level for the PWM converter. As shown in Figure 5, the internal 200µA current sink, I_{OCSET} develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the overcurrent comparator (OVER-CURRENT). When the voltage across the upper MOSFET (V_{DS}) exceeds V_{SET}, the overcurrent comparator trips to set the overcurrent latch. Both V_{SET} and V_{DS} are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

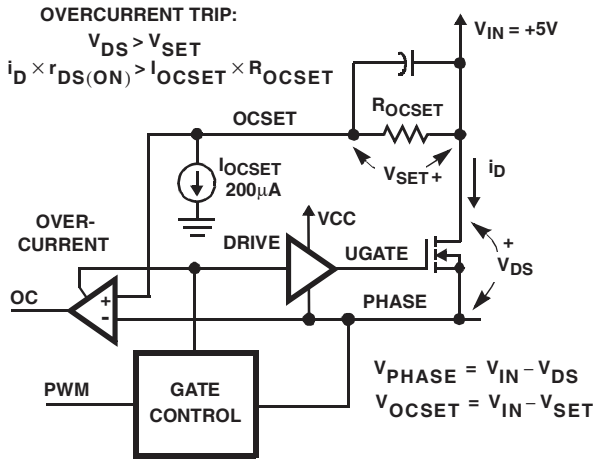


FIGURE 5. OVERCURRENT DETECTION

The OC trip point varies with MOSFET's $r_{DS(ON)}$ temperature variations. To avoid overcurrent tripping in the normal operating load range, determine the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled *PWM Output Inductor Selection*.

OUT1 Voltage Program

The output voltage of the PWM converter is programmed to discrete levels between $1.3V_{DC}$ and $3.5V_{DC}$. This output (OUT1) is designed to supply the core voltage of Intel's advanced microprocessors. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible 5-bit digital-to-analog converter. The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, because they are internally pulled up to an internal voltage of about 5V by a 10µA current source. Changing the VID inputs during operation is not recommended and could toggle the PGOOD signal and exercise the overvoltage protection.

TABLE 1. OUT1 VOLTAGE PROGRAM

PIN NAME					NOMINAL DACOUT VOLTAGE
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	2.00
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

NOTE: 0 = connected to GND, 1 = open or connected to 5V through pull-up resistors.

OUT2 Voltage Selection

The AGP output voltage is internally set to one of two levels, based on the status of the SELECT pin. Grounding the SELECT pin enables the internal 1.5V regulator control circuitry. Left open, the SELECT pin is internally pulled 'high' and the AGP voltage is regulated to 3.3V during the soft-start sequence. Once complete, the gate drive is increased and the regulator becomes a simple pass circuit for the 3.3V input voltage.

OUT3 and OUT4 Voltage Adjustability

The GTL bus voltage (1.5V, OUT3) and the chip set and/or cache memory voltage (1.8V, OUT4) are internally set for simple, low-cost implementation in typical Intel motherboard architectures. However, if different voltage settings are desired for these two outputs, the FIX pin provides the necessary adaptability. Left open (NC), this pin sets the fixed output voltages described above. Grounding this pin allows both output voltages to be set by means of external resistor dividers as shown in Figure 6.

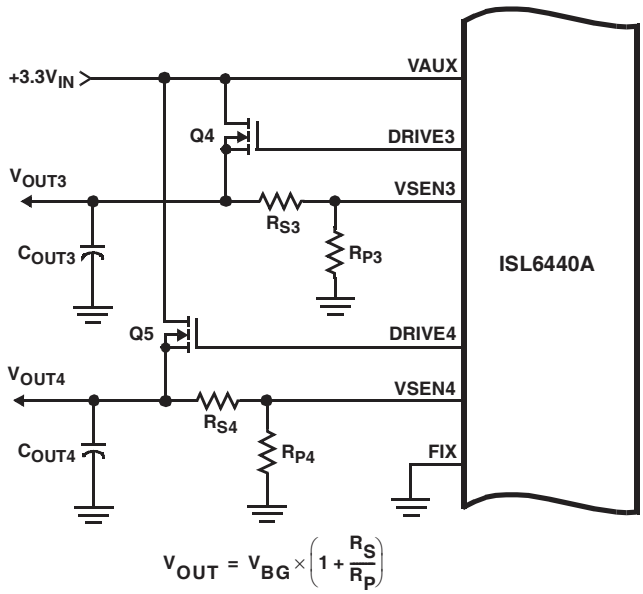


FIGURE 6. ADJUSTING THE OUTPUT VOLTAGE OF OUTPUTS 3 AND 4

Application Guidelines

Soft-Start Interval

Initially, the soft-start function clamps the error amplifier's output of the PWM converter. This generates PHASE pulses of increasing width that charge the output capacitor(s). After the output voltage increases to approximately 70% of the set value, the reference input of the error amplifier is clamped to a voltage proportional to the SS pin voltage. The resulting output voltages start-up as shown in Figure 2.

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. The soft-start interval and the surge current are programmed by the soft-start capacitor, C_{SS}. Programming a faster soft-start interval increases the peak surge current. The peak surge current occurs during the initial output voltage rise to 70% of the set value.

Shutdown

The ISL6440A features a dedicated shutdown pin (SD). A TTL-compatible, logic high signal applied to this pin shuts down (disables) all four outputs and discharges the soft-start capacitor. Following a shutdown, a logic low signal re-enables the outputs through initiation of a new soft-start cycle. Left open this pin will asses a logic low state, due to its internal pull-down resistor, thus enabling normal operation of all outputs.

The PWM output does not switch until the soft-start voltage (V_{SS}) exceeds the oscillator's valley voltage. The references on each linear's error amplifier are clamped to the soft-start voltage. Holding the SS pin low (with an open drain or collector signal) turns off all four regulators.

The '11111' VID code also shuts down the IC.

Layout Considerations

MOSFETs switch quickly and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper PWM MOSFET. Prior to turn-off, the upper MOSFET was carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes. See *Application Note AN9836* for evaluation board drawings of the component placement and the printed circuit board layout of a typical application.

There are two sets of critical components in a DC-DC converter using a ISL6440A controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the soft-start capacitor, C_{SS}. Locate these components close to their connecting pins on the control IC. Minimize any leakage current paths from SS node, since the internal current source is only 28µA.

A multi-layer printed circuit board is recommended. Figure 7 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE nodes, but do not unnecessarily oversize these particular islands. Since the PHASE nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

PWM Controller Feedback Compensation

The PWM controller uses voltage-mode control for output regulation. This section highlights the design consideration for a PWM voltage-mode controller. Apply the methods and considerations only to the PWM controller.

Figure 8 highlights the voltage-mode control loop for a synchronous rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The reference voltage level is the DAC output voltage (DACOUT). The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC gain, given by V_{IN}/V_{OSC}, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the ISL6440A) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2,

R3, C1, C2, and C3) in Figure 7. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick gain (R2/R1) for desired converter bandwidth
2. Place first zero below filter's double pole (~75% F_{LC})
3. Place second zero at filter's double pole
4. Place first pole at the ESR zero
5. Place second pole at half the switching frequency
6. Check gain against error amplifier's open-loop gain
7. Estimate phase margin - repeat if necessary

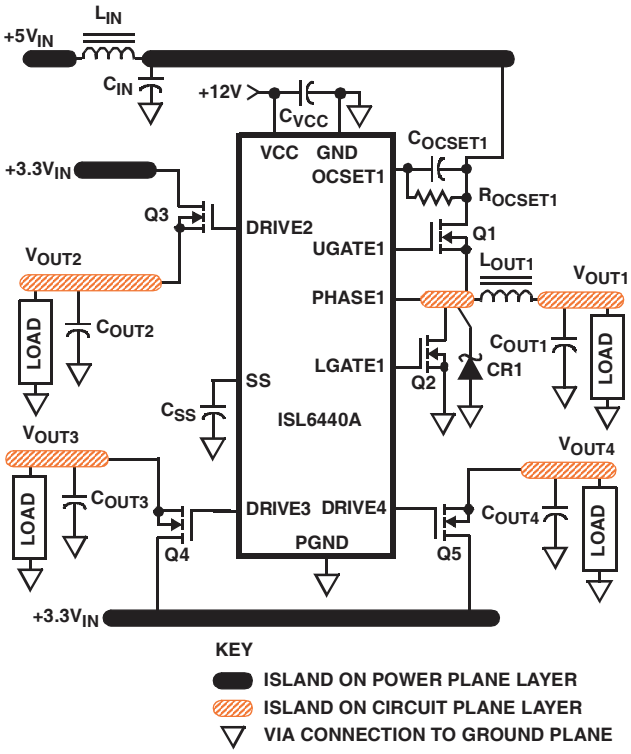


FIGURE 7. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Figure 9 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual modulator gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown in Figure 8. Using the above guidelines should yield a compensation gain similar to the curve plotted. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed loop gain is constructed on the log-log graph of Figure 9 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst-case component variations when determining phase margin.

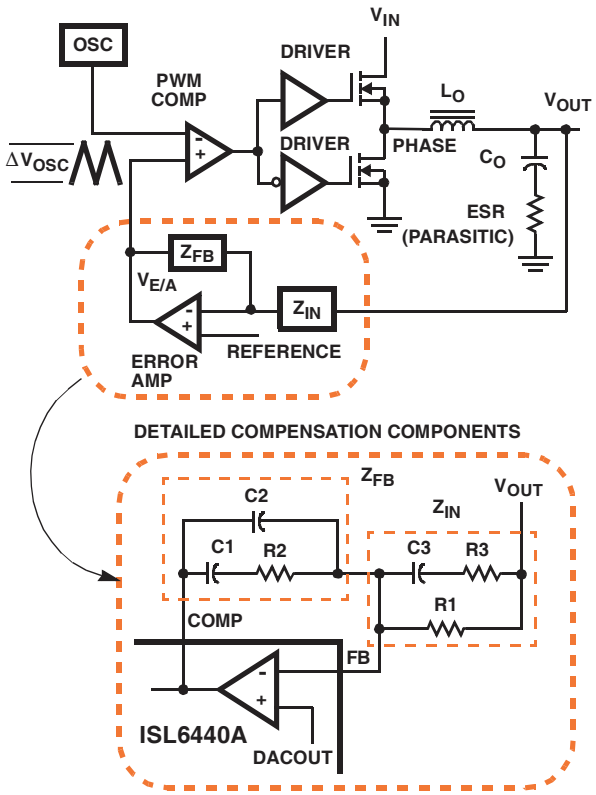


FIGURE 8. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \qquad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

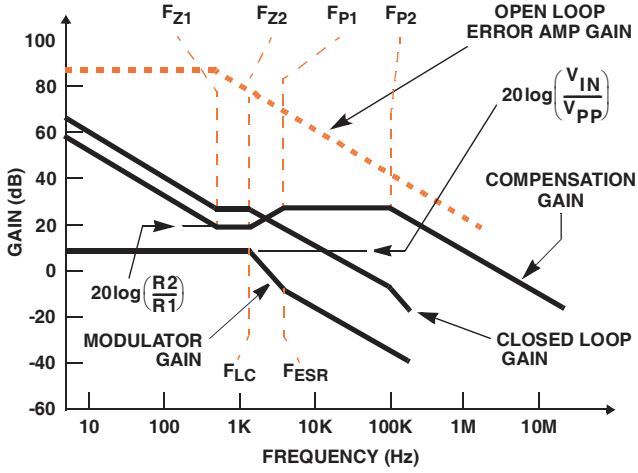


FIGURE 9. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitors

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements. Additionally, the PWM converters require an output capacitor to filter the current ripple. The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Linear Output Capacitors

The output capacitors for the linear regulators provide dynamic load current. The linear controllers use dominant pole compensation integrated into the error amplifier and are insensitive to output capacitor selection. Output capacitors should be selected for transient load regulation.

PWM Output Inductor

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values increase the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6440A will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitors

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately ½ the summation of the DC load current.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Considerations

The ISL6440A requires five external transistors. Two N-Channel MOSFETs are used in the synchronous rectified buck topology of PWM1 converter. It is recommended that the AGP linear regulator pass element be a N-Channel MOSFET as well. The GTL and memory linear controllers can also each drive a MOSFET or a NPN bipolar as a pass transistor. All these transistors should be selected based upon $r_{DS(ON)}$, current gain, saturation voltages, gate supply requirements, and thermal management considerations.

PWM MOSFETs

In high-current PWM applications, the MOSFET power dissipation, package selection and heat sink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see the equations below). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

The equations below assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6440A and do not heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heat sink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The $r_{DS(ON)}$ is different for the two equations above even if the same device is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Figure 10 shows the gate drive where the upper MOSFET's gate-to-source voltage is approximately VCC less the input supply. For +5V main power and +12VDC for the bias, the gate-to-source voltage of Q1 is 7V. The lower gate drive voltage is +12VDC. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to VCC.

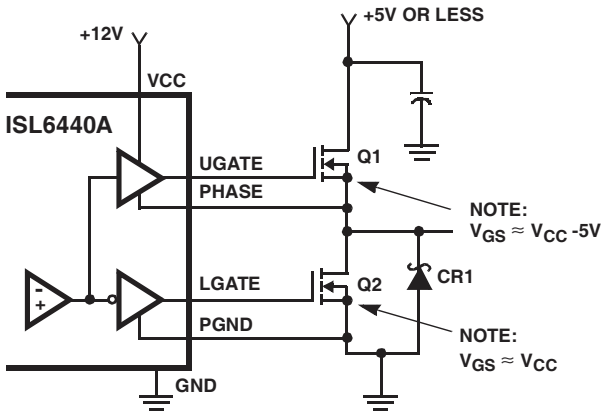


FIGURE 10. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE OPTION

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. The diode must be a Schottky type to prevent the lossy parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but efficiency could drop one or two percent as a result. The diode's rated reverse breakdown voltage must be greater than the maximum input voltage.

Linear Controller Transistors

The main criteria for selection of transistors for the linear regulators is package selection for efficient removal of heat. The power dissipated in a linear regulator is:

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heat sink that maintains the junction temperature below the rating with a the maximum expected ambient temperature.

When selecting bipolar NPN transistors for use with the linear controllers, insure the current gain at the given operating VCE is sufficiently large to provide the desired output load current when the base is fed with the minimum driver output current.

ISL6440A DC-DC Converter Application Circuit

Figure 11 shows an application circuit of a power supply for a microprocessor computer system. The power supply provides the microprocessor core voltage (VOUT1), the AGP bus voltage (VOUT2), the GTL bus voltage (VOUT3), and the memory voltage (VOUT4) from +3.3V, +5VDC, and +12VDC.

For detailed information on the circuit, including a bill of materials and circuit board description, see *Application Note AN9836*. Also see Intersil's web page (http://www.intersil.com) for the latest information.

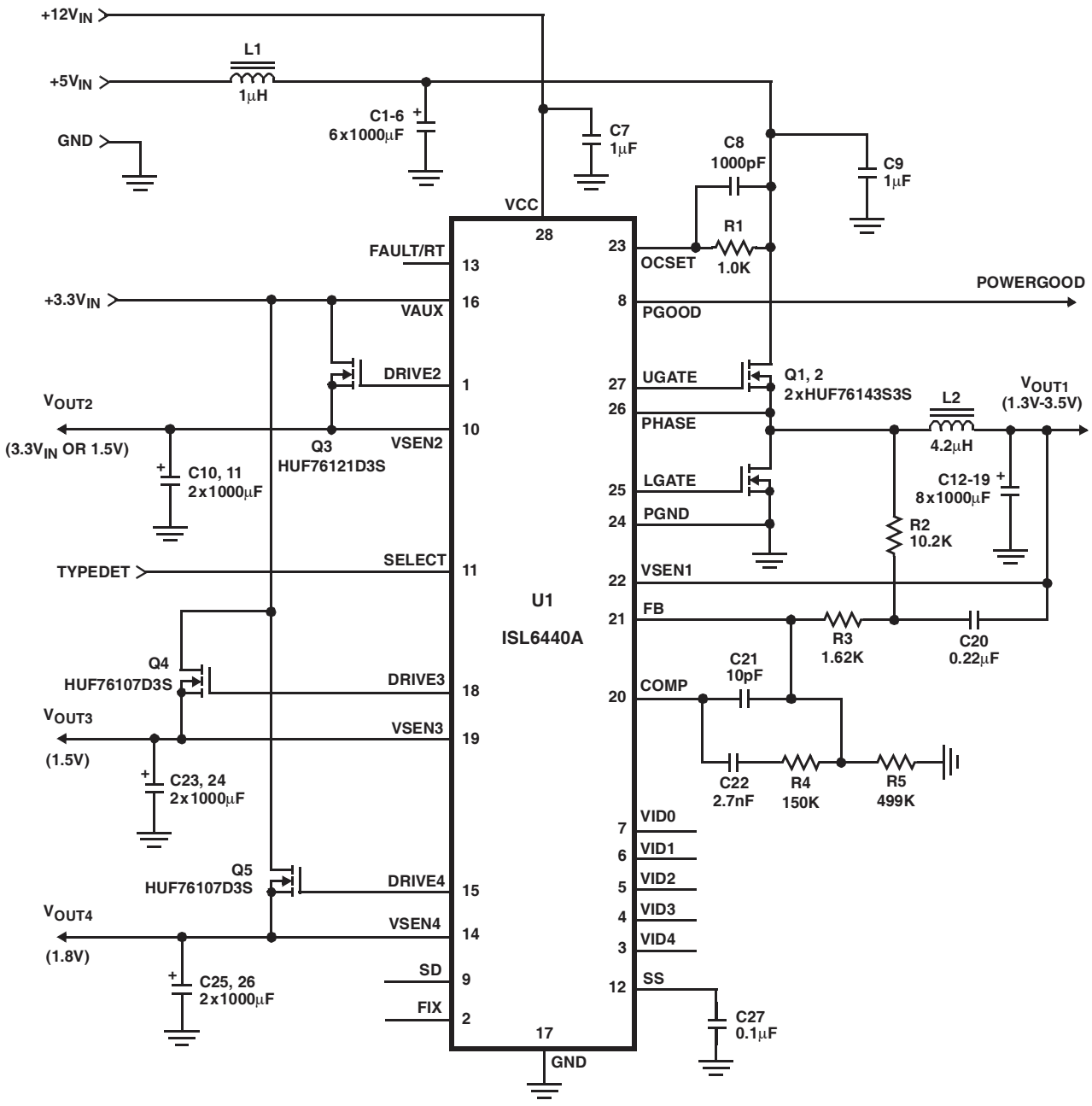
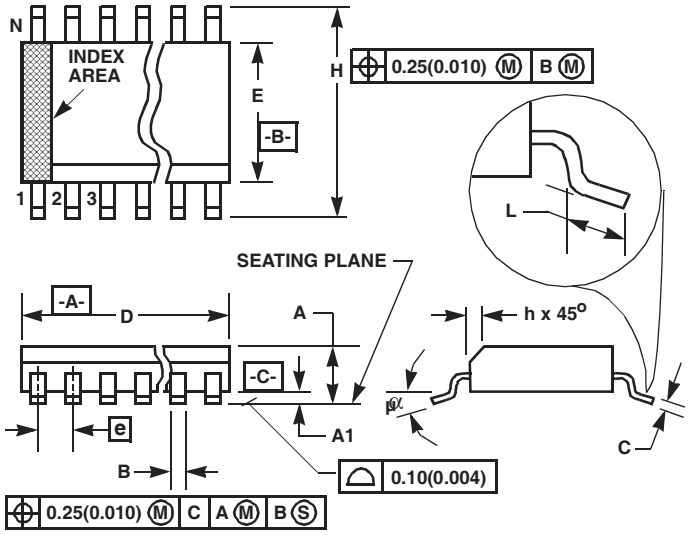


FIGURE 11. POWER SUPPLY APPLICATION CIRCUIT FOR A MICROPROCESSOR COMPUTER SYSTEM

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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