ISL6562

Microprocessor CORE Voltage Regulator Two-Phase Buck PWM Controller

FN9012
Rev 0.00
Mar 23, 2001

The ISL6562 two-phase current mode, PWM control IC together with companion gate drivers, the HIP6601A, HIP6602A, HIP6603A or HIP6604 and MOSFETs provides a precision voltage regulation system for advanced microprocessors. Two-phase power conversion is a marked departure from earlier single phase converter configurations previously employed to satisfy the ever increasing current demands of modern microprocessors. Multi-phase converters, by distributing the power and load current results in smaller and lower cost transistors with fewer input and output capacitors. These reductions accrue from the higher effective conversion frequency with higher frequency ripple current due to the phase interleaving process of this topology. For example, a two phase converter operating at 350kHz per phase will have a ripple frequency of 700kHz. Moreover, greater converter bandwidth of this design results in faster response to load transients.

Outstanding features of this controller IC include programmable VID codes from the microprocessor that range from 1.050V to 1.825V with an accuracy of ±0.8%. Pull up currents on these VID pins eliminates the need for external pull up resistors.

Another feature of this controller IC is the PWRGD monitor circuit which is held low until the CORE voltage increases, to within 18% of the programmed voltage. Over-voltage, 24% above programmed CORE voltage, results in the PWRGD output going low to indicate that the CORE is above the specified limit. Under voltage is also detected and results in PWRGD going low if the CORE voltage falls 18% below the programmed level. Over-current protection folds back the output voltage to 95mV, reducing the regulator dissipation. These features provide monitoring and protection for the microprocessor and power system.

Ordering Information

PART NUMBER	TEMP. (^{o}C)	PACKAGE	PKG. NO.
ISL6562CB	0 to 70	16 Ld SOIC	M16.15
ISL6562CB-T	16 Ld SOIC Tape and Reel		
ISL6560/62EVAL1	Evaluation Platform		

Features

- Two-Phase Power Conversion
- Precision Channel Current Sharing
- Precision CORE Voltage Regulation
  - ±0.8% Accuracy
- Microprocessor Voltage Identification Input
  - 5-Bit VID Input
  - 1.050V to 1.825V in 25mV Steps
  - Programmable “Droop” Voltage
- Fast Transient Recovery Time
- Over Current Protection
- High Ripple Frequency, (Channel Frequency Times Number of Channels). . . . . 100kHz to 2MHz

Applications

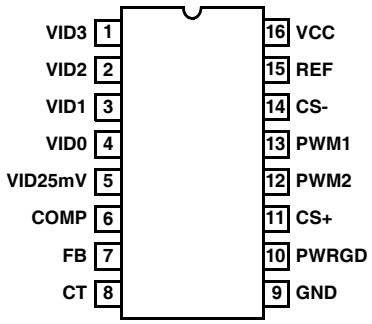
- VRM8.5 Modules
- Intel® Tualatin Processor Voltage Regulator
- Low Output Voltage, High Current DC/DC Converters

Related Literature

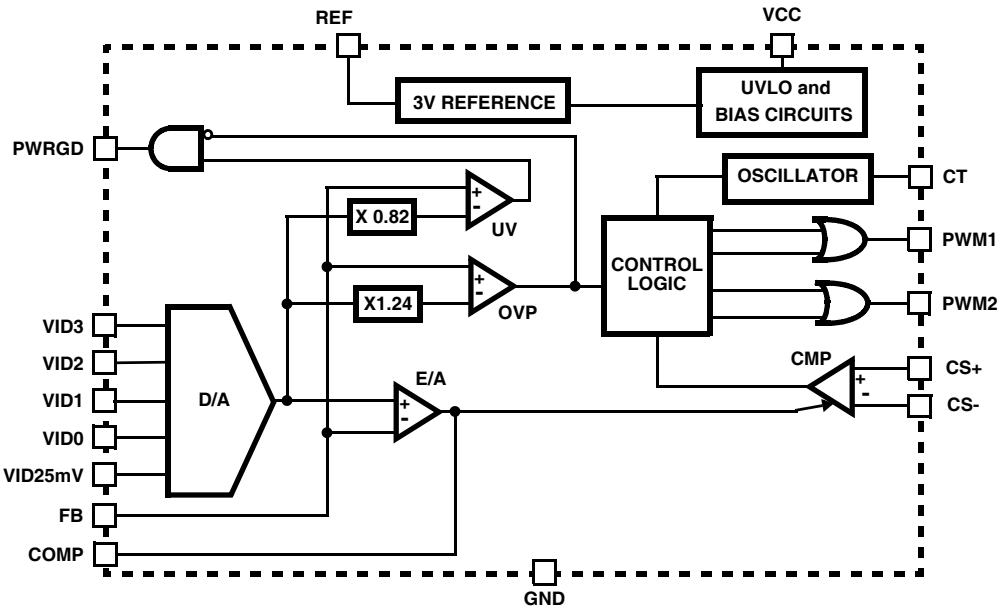
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

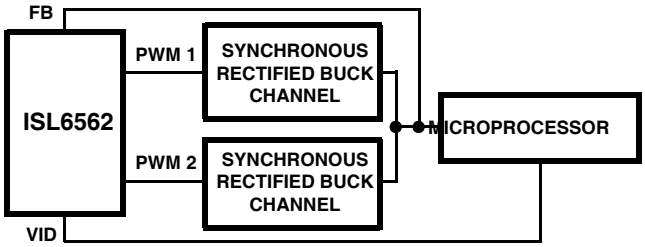
ISL6562 (SOIC)
TOP VIEW



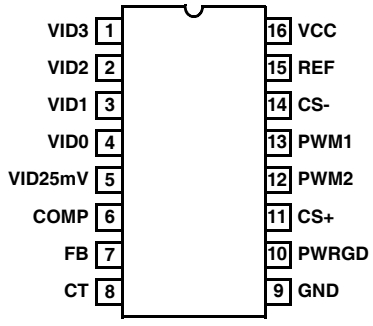
Block Diagram



Simplified Power System Diagram



Functional Pin Description



VID3 (Pin 1), VID2 (Pin 2), VID1 (Pin 3), VID0 (Pin 4) and VID25mV (Pin 5)

Voltage Identification inputs from microprocessor. These pins respond to TTL and 3.3V logic signals. The ISL6562 decodes VID bits to establish the output voltage. See Table 1.

COMP (Pin 6)

Output of the internal transconductance error amplifier. Voltage at this terminal sets the output current level of the Current Sense Comparator. Pulling this pin to ground disables the oscillator and drives both PWM outputs low.

FB (Pin 7)

Inverting input of the internal transconductance error amplifier.

CT (Pin 8)

A capacitor on this terminal sets the frequency of the internal oscillator.

GND (Pin 9)

Bias and reference ground. All signals are referenced to this pin.

PWRGD (Pin 10)

Open drain connection. A high voltage level at this pin with a resistor connected to this terminal and VCC indicates that CORE voltage is at the proper level,

CS+ (Pin 11) and CS- (Pin 14) These inputs monitor the supply current to the converter positive input voltage. CS+ is connected directly to the decoupled supply voltage and current sampling resistor. CS- is connected to the other end of the current sampling resistor and the upper drains of the series transistors.

PWM2 (Pin 12) and PWM1 (Pin 13)

PWM outputs connected to the gate driver ICs.

REF (Pin 15)

Three volt supply used to bias the output of the transconductance amplifier.

VCC (Pin 16)

Bias supply. Connect this pin to a 12V supply.

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 15V
CS+. CS- . . . . . -0.3V to VCC + 0.3V
PWRGD . . . . . -0.3V to VCC
All Other Inputs and Outputs . . . . . -0.3V to 5V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . . TBD
Machine Model (Per EIAJ ED-4701 Method C-111) . . . . . TBD

Thermal Information

Thermal Resistance (Note 1) θ_{JA} (^{o}C/W)
SOIC Package 106
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Ambient Temperature Range. . . . . 0^{o}C to 70^{o}C
Maximum Operating Junction Temperature. . . . . 125^{o}C
Supply Voltage, VCC . . . . . 12V ±10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Input Supply Current	I_{CC}	VCC = 12V	-	5.8	9.0	mA
Input Supply Current, UVLO Mode	$I_{CC(UVLO)}$	VCC ≤ V_{UVLO}, VCC Rising	-	5.7	8.9	mA
Undervoltage Lock Out Voltage	V_{UVLO}		5.4	6.4	6.9	V
Undervoltage Lock Out Hysteresis			0.1	0.4	0.8	V
DAC and REFERENCE VOLTAGES						
Minimum DAC Programed Voltage	V_{FB}	DAC Programmed to 1.050V	1.042	1.050	1.058	V
Middle DAC Programed Voltage	V_{FB}	DAC Programmed to 1.500V	1.488	1.500	1.512	V
Maximum DAC Programed Voltage	V_{FB}	DAC Programmed to 1.825V	1.811	1.825	1.839	V
Line Regulation	ΔV_{FB}	VCC = 10V to 14V	-	0.05	-	%
Crowbar Trip Point at FB Input	$V_{CROWBAR}$	Percent of Nominal DAC Voltage	114	124	134	%
Crowbar Reset Point at FB Input	$V_{CROWBAR}$	Percent of Nominal DAC Voltage	50	60	70	%
Crowbar Response Time	$I_{CROWBAR}$	Overvoltage to PWM Going Low	-	300	-	ns
Reference Voltage	V_{REF}	0mA ≤ I_{REF} ≤ 1mA	2.952	3.000	3.048	V
Output Current	I_{REF}		300	-	-	µA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$		-	-	0.6	V
Input High Voltage	$V_{IH(VID)}$		2.2	-	-	V
VID Pull-Up	I_{VID}	VIDx = 0V or VIDx = 3V	10	20	40	µA
Internal Pull-Up Voltage			4.5	5.0	5.5	V
OSCILLATOR						
Maximum Frequency	$f_{CT(MAX)}$		2.0	-	-	MHz
Frequency Variation	Δf_{CT}	T_A = 25^{o}C, CT = 91pF	430	500	570	kHz
CT Charging Current	I_{CT}	T_A = 25^{o}C, V_{FB} in Regulation	130	150	170	µA
CT Charging Current	I_{CT}	T_A = 25^{o}C, V_{FB} = 0V	26	36	46	µA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$		-	200	-	kΩ
Transconductance	$g_{m(ERR)}$		2.0	2.2	2.4	mS

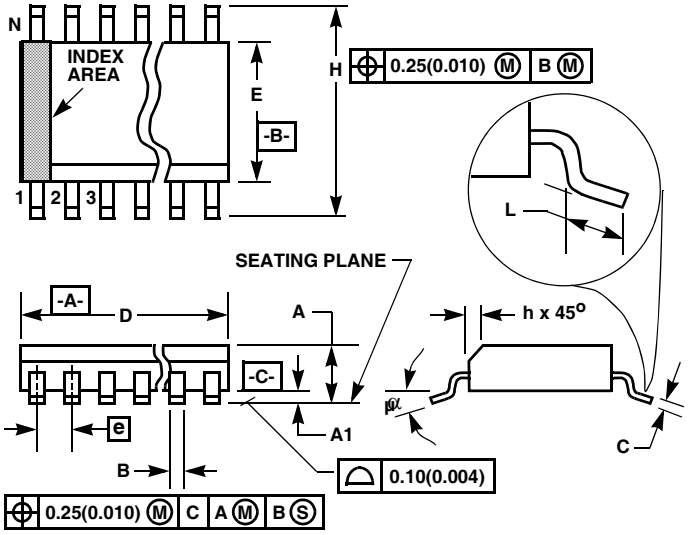
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Current	$I_{O(ERR)}$	FB Forced to V_{OUT} - 3%	-	1	-	mA
Input Bias Current	I_{FB}		-	5	100	nA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} - 3%	-	3.0	-	V
Output Disable Threshold	$V_{COMP(OFF)}$		560	720	800	mV
FB Low Foldback Threshold	$V_{FB(LOW)}$		375	425	500	mV
-3dB Bandwidth	BW_{ERR}	COMP = Open	-	500	-	kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	CS+ = VCC, FB Forced to V_{OUT} - 3%	69	79	89	mV
		$0.8 \le COMP \le 1V$	-	0	15	mV
Current Limit Foldback Voltage	$V_{CS(FOLD)}$	$FB \le 375mV$	37	47	58	mV
$\Delta V_{COMP}/\Delta V_{CS}$	n_i	$1\ V \le V_{COMP} \le 3V$	-	25	-	V/V
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS- = VCC	-	0.5	5.0	µA
Response Time	t_{CS}	CS+ - (CS-) ≥ 89mV to PWM Going Low	-	50	-	ns
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Percent of Nominal Output	76	82	88	%
Overvoltage Threshold	$V_{PWRGD(OV)}$	Percent of Nominal Output	114	124	134	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 100µA	-	30	200	mV
Response Time			-	200	-	ns
PWM OUTPUTS						
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA	-	100	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400µA	4.5	5.0	5.5	V
Output Current	I_{PWM}		0.4	1	-	mA
Duty Cycle Limit, by Design	D_{MAX}	Per Phase, Relative to f_{CT}	-	-	50	%

VOLTAGE IDENTIFICATION CODE AT PROCESSOR PINS					V_{CC}CORE (VDC)
VID25mV	VID3	VID2	VID1	VID0	
0	0	1	0	0	1.050
1	0	1	0	0	1.075
0	0	0	1	1	1.100
1	0	0	1	1	1.125
0	0	0	1	0	1.150
1	0	0	1	0	1.175
0	0	0	0	1	1.200
1	0	0	0	1	1.225
0	0	0	0	0	1.250
1	0	0	0	0	1.275
0	1	1	1	1	1.300
1	1	1	1	1	1.325
0	1	1	1	0	1.350
1	1	1	1	0	1.375
0	1	1	0	1	1.400
1	1	1	0	1	1.425

VOLTAGE IDENTIFICATION CODE AT PROCESSOR PINS					V_{CC}CORE (VDC)
VID25mV	VID3	VID2	VID1	VID0	
0	1	1	0	0	1.450
1	1	1	0	0	1.475
0	1	0	1	1	1.500
1	1	0	1	1	1.525
0	1	0	1	0	1.550
1	1	0	1	0	1.575
0	1	0	0	1	1.600
1	1	0	0	1	1.625
0	1	0	0	0	1.650
1	1	0	0	0	1.675
0	0	1	1	1	1.700
1	0	1	1	1	1.725
0	0	1	1	0	1.750
1	0	1	1	0	1.775
0	0	1	0	1	1.800
1	0	1	0	1	1.825

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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