ISL68301

Scalable Single Output Digital PWM Controller with PMBus

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The ISL68301 is a PMBus compliant, single-phase digital DC/DC controller for use with SPS and DrMOS power stages.

The ISL68301 implements the Renesas fully digital ChargeMode™ control modulation scheme, allowing it to achieve both industry leading performance and ease of use. ChargeMode control provides an inherently stable control loop that can respond to load transients in a single switching cycle, significantly decreasing output capacitor requirements.

A dedicated current share bus allows for paralleling up to eight devices in a current share configuration, allowing support for a wide range of load currents.

In conjunction with many other Renesas digital controllers, the ISL68301 is capable of complex sequencing and fault spreading. The Digital-DC™ (DDC) bus is a single-wire serial bus which provides high performance inter-device communication without the need for external sequencers, reducing overall system costs.

The PMBus interface facilitates device configuration, provides supply telemetry and detailed fault reporting including a parametric capture tool (SnapShot). All of these features are conveniently accessible through the PowerNavigator™ software tool. Additionally, a wide array of common configuration options are independently configurable through use of pin-strap resistors.

The ISL68301 supports a comprehensive fault management system, with dedicated hardware support for cycle-by-cycle overcurrent, overvoltage, undervoltage, and temperature faults. The configurable fault response system is capable of latching off or restarting the output on a fault-by-fault basis. Integrated LDOs for device and gate driver bias allow for single supply operation.

The ISL68301 drives a PWM output designed to be paired with the Renesas family of Smart Power power stages.

A companion device, the ISL68300, has built-in MOSFET driver circuitry which supports use with discrete output MOSFETs.

Related Literature

For a full list of related documents, visit our website

- ISL68301 product page

Features

- Unique compensation-free design, which is always stable
- Output voltage range: 0.45V to 5.5V
- Input voltage range: 4.75V to 16V or 4.5V to 5.5V
- 0.5% output voltage accuracy over line, load, and temperature
- ChargeMode control achieves fast transient response, requires minimal output capacitance, and provides output stability without compensation
- Single-channel output, can be paralleled with up to eight devices in a single droop-less current sharing output
- Switching frequency range of 200kHz to 1.0MHz
- Proprietary single-wire DDC serial bus enables voltage sequencing and fault spreading with other Renesas digital power ICs
- Cycle-by-cycle inductor peak current protection
- Configurable fault protection for output voltage UV/OV, input voltage UV/OV, internal and SPS temperature
- Cycle-by-cycle output current measurement with adjustable gain settings for sensing with SPS current monitor or low DCR inductors
- Dedicated telemetry ADC monitors input voltage, input current, output voltage, internal temperature, and power stage temperature
- Nonvolatile memory (NVRAM) stores operating parameters and fault events across POR cycles
- PMBus compliant. Supports 113 PMBus commands
- Compatible with Smart Power Stage (SPS) devices

Applications

- Servers and storage equipment
- Telecom and datacom equipment
- Power supplies (FPGA, ASIC, DSP, memory)

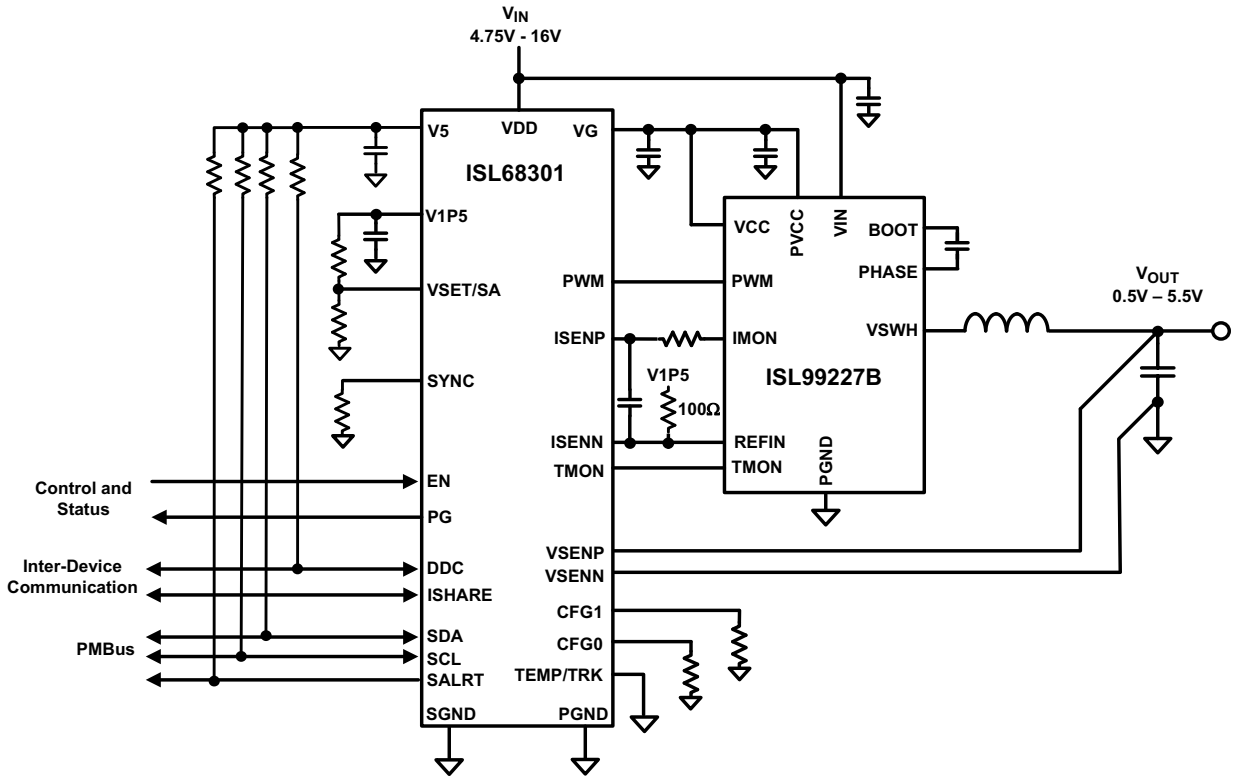


Figure 1. Wide Range Input and Output Applications

Contents

1. Overview

1.1 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL68301IRAZ	68301 IRAZ	-40 to +85	-	24 Ld 4x4 QFN	L24.4x4H
ISL68301IRAZ-T	68301 IRAZ	-40 to +85	4k	24 Ld 4x4 QFN	L24.4x4H
ISL68301IRAZ-T7A	68301 IRAZ	-40 to +85	250	24 Ld 4x4 QFN	L24.4x4H
ISL68301IRAZ-TK	68301 IRAZ	-40 to +85	1k	24 Ld 4x4 QFN	L24.4x4H

Notes:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pbfree peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL68301 product information page.For more information about MSL, see TB363.

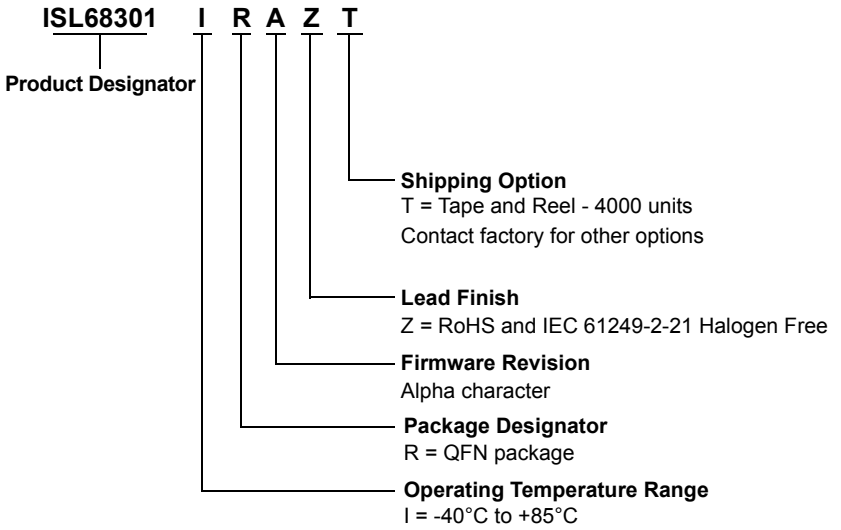
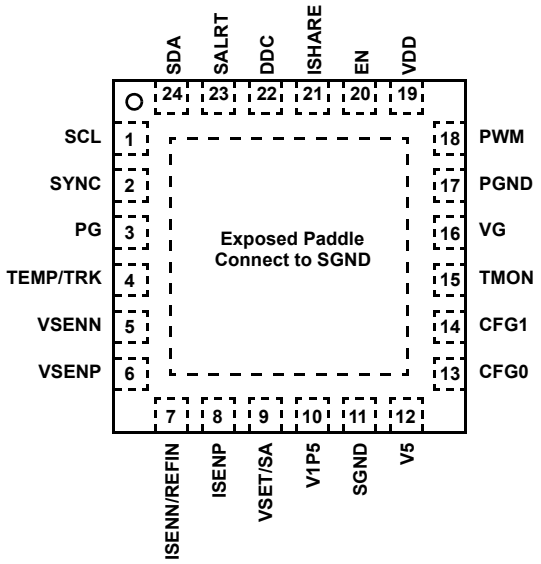


Table 1. Key Differences between Family of Parts

Part Number	Internal MOSFET Driver	SPS Support	Recommended Power Stage
ISL68301	No	Yes	ISL99227B
ISL68300	Yes	No	Discrete or Dual Device MOSFETs

1.2 Pin Configuration

24 Ld 4x4 QFN
Top View



1.3 Pin Descriptions

Pin	Label	Type (Note 4)	Description
1	SCL	I/O	Serial clock. Connect to an external host and/or other PMBus devices. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended.
2	SYNC	M/I/O	Clock synchronization input. Sets the frequency of the internal clock to synchronize to an external clock or an output internal clock. When used as part of a SYNC bus for phase spreading or current sharing, at most, one of the devices may be configured to use this pin as and output. In such applications, do not attach pull-up or pull-down resistors to the bus.
3	PG	O	Power-good output. Can be configured as open-drain or push-pull using the PMBus interface. The default setting is open-drain.
4	TEMP/TRK	I	External temperature sensor or tracking input. When using as an external temperature sensor, connect to an external 2N3904 base-emitter junction with collector shorted to base. When configured for tracking, connect to a tracking voltage input. If not used, connect to SGND.
5	VSENN	I	Differential voltage sense feedback. Connect to a negative output regulation point.
6	VSENP	I	Differential voltage sense feedback. Connect to a positive output regulation point.
7	ISENN/REFIN	I	Negative differential voltage input for current sensing should be routed as a pair with ISENP. Supports DCR current sensing and SPS current monitor pin. See “Inductor Current Sensing” on page 24 for details.
8	ISENP	I	Positive differential voltage input for current sensing should be routed as a pair with ISENN. Supports DCR current sensing and SPS current monitor pin. See “Inductor Current Sensing” on page 24 for details.
9	VSET/SA	M	Used to assign unique PMBus address for each device and to set output voltage set-point. See PMBus address and output voltage options. Connect one resistor to SGND and a second resistor to V1P5 (Pin 10). Default V_{OUT} maximum is 115% of V_{OUT} setting, but this can be overridden with VOUT_MAX command using the PMBus interface.
10	V1P5	PWR	Bypass for internal 1.5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X5R 6V or better ceramic capacitor placed close to this pin.

Pin	Label	Type (Note 4)	Description
11	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND. All pin-strap resistors should be connected to SGND. SGND must be connected to PGND for minimum voltage differential between SGND and PGND. Use of a contiguous ground plane is recommended.
12	V5	PWR	Bypass for internal 5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X5R 6V or better ceramic capacitor placed close to this pin.
13	CFG0	I	Pin-strap resistor reading configuration pin used to set device operating settings. See Table 3 on page 16 for details. Leave floating if not used.
14	CFG1	I	Pin-strap resistor reading configuration pin used to set device operating settings. See Table 3 on page 16 for details. Leave floating if not used.
15	TMON	I	SPS temperature monitoring pin. Connect to SGND if not used. A voltage above 2.5V on this pin always triggers an over-temperature fault.
16	VG	PWR	5V nominal supply for gate drive circuitry. Decouple with a high quality 4.7µF X5R 6V or better ceramic capacitor placed close to this pin. Additional decoupling capacitance may be needed depending on the gate drive current needed to drive the SPS power stage. Limited to 40mA maximum.
17	PGND	PWR	Power ground. Must connect to SGND using a contiguous ground plane. VDD and VG bypass capacitors must connect to this pin by the shortest possible path.
18	PWM	O	Tri-state PWM signal.
19	VDD	PWR	Supply voltage. Decouple with a high quality 1µF X5R 16V or better ceramic capacitor placed close to this pin.
20	EN	I	Enable input. Active signal enables device. Recommended to be tied low during device configuration. The EN signal must be “de-bounced” to achieve specified delay timing. Positive or negative pulse widths shorter than 10µs are ignored.
21	ISHARE	I/O	Current sharing communication bus. Connect to ISHARE pins of other ISL68301 devices within a current sharing group. Leave disconnected in single phase applications.
22	DDC	I/O	Single-wire DDC bus (inter-device communication). Requires a pull-up resistor to a 3.3V or 5.5V source. A V5 source recommended. Pull-up voltage must be present when the device is powered.
23	SALRT	O	Serial alert. Connect to an external host if desired. Requires a pull-up resistor to a 3.3V or 5.5V source. V5 source recommended. Leave this pin floating if not used.
24	SDA	I/O	Serial data. Connect to external host and/or to other Renesas devices. Requires a pull-up resistor to a 3.3V or 5.5V source. A V5 source is recommended.
PAD	-	PWR	Exposed thermal pad. Connect to a low impedance ground plane. Internal connection to SGND.

Note:
4. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pins.

1.4 Block Diagram

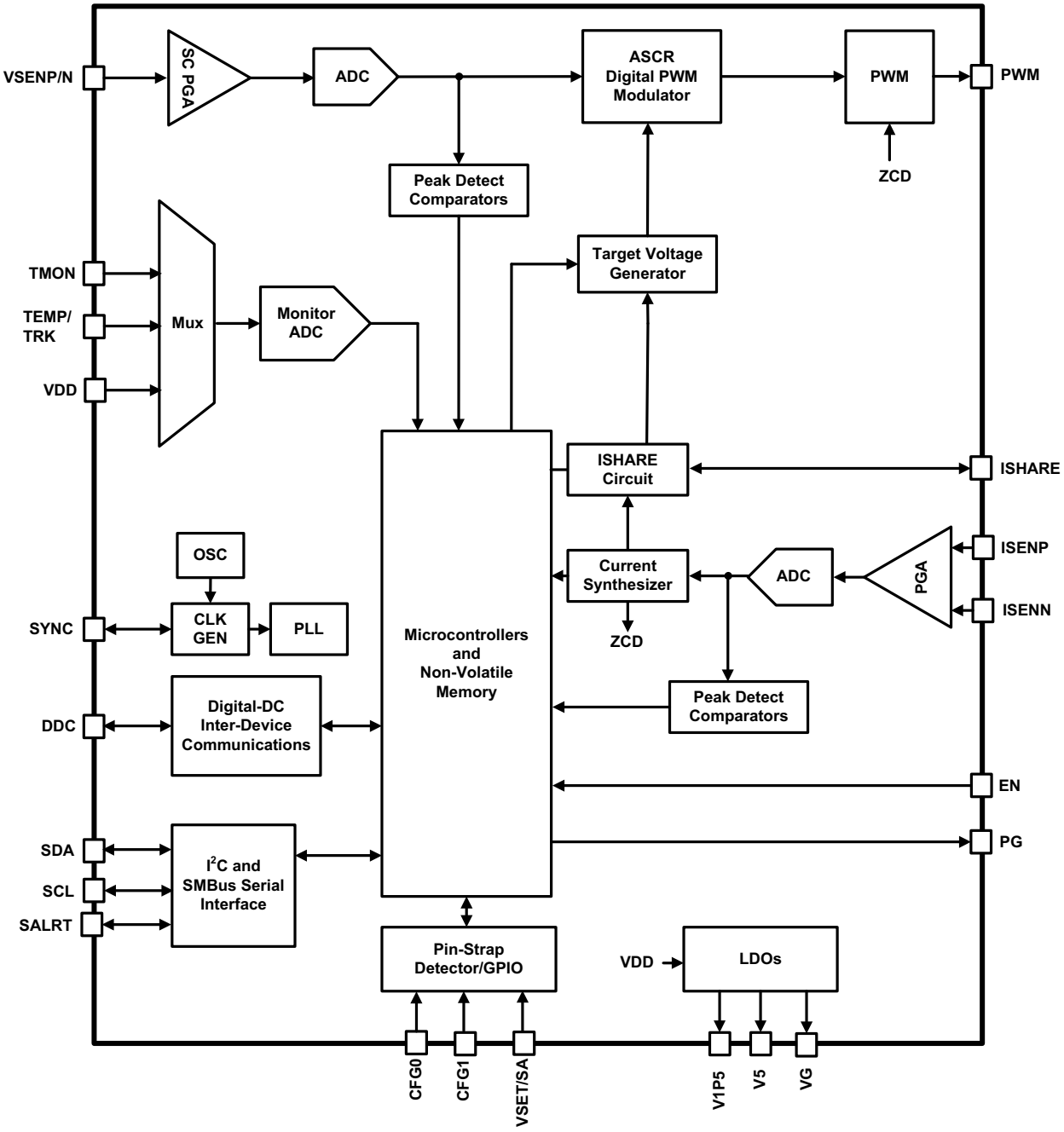


Figure 2. Block Diagram

1.5 Typical Applications

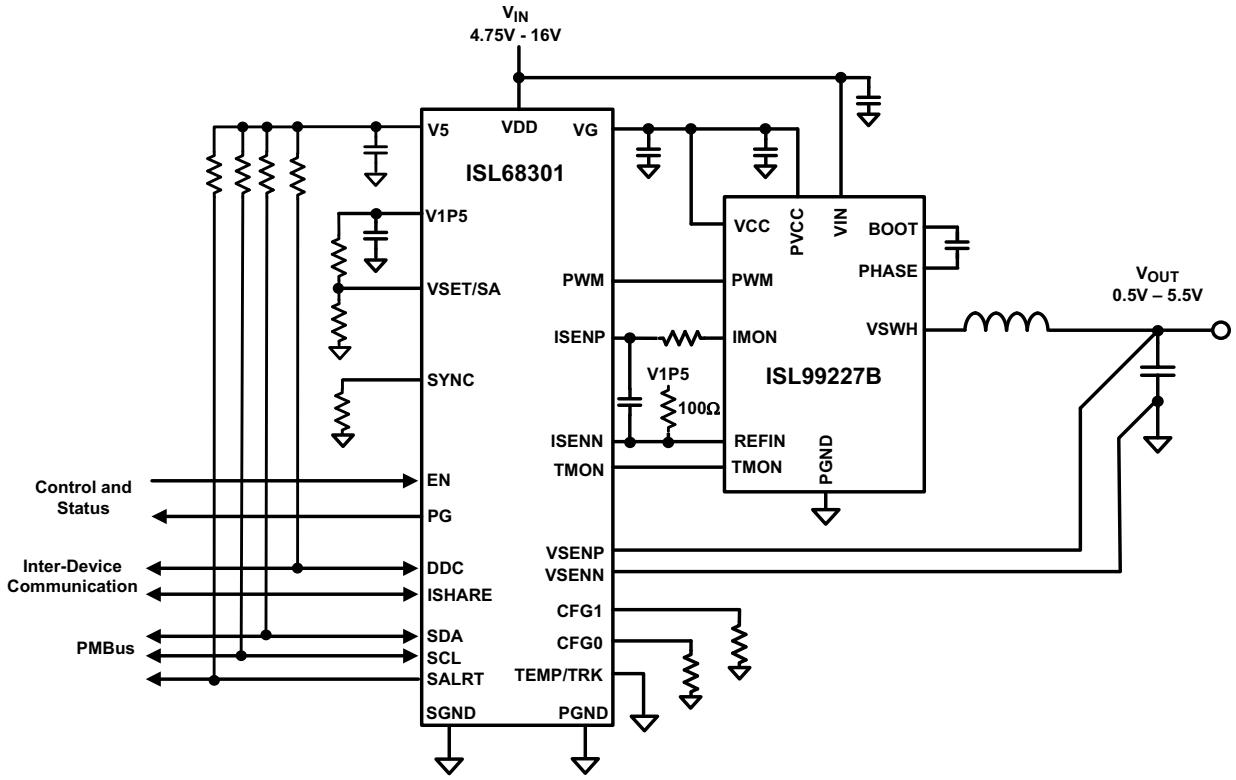


Figure 3. SPS with the ISL99227B

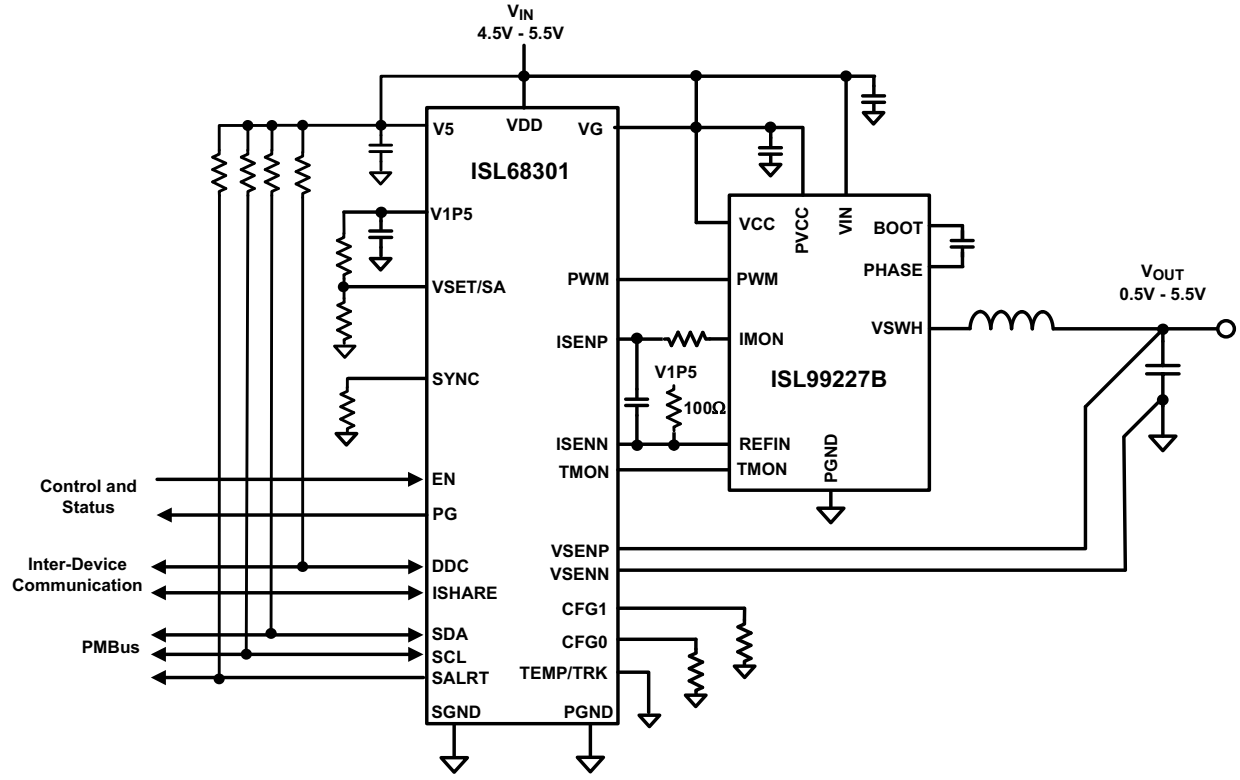


Figure 4. 5V Nominal Input with the ISL99227B

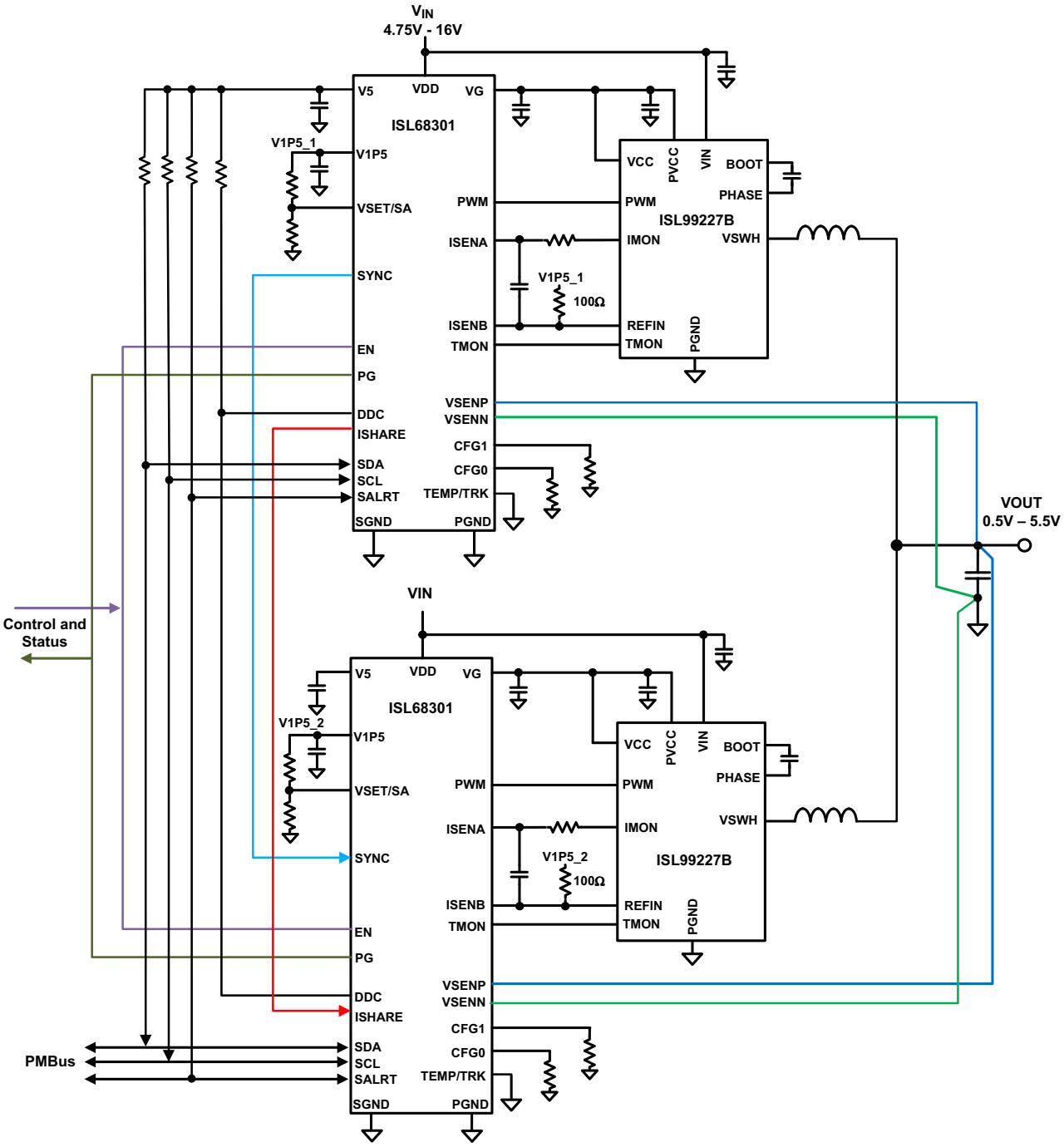


Figure 5. 2 Phase Current Sharing Rail

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
DC Supply Voltage: VDD	-0.3	+18	V
Logic I/O Voltage: SCL, SDA, SALRT, SYNC, PG, VSET/SA, EN, DDC, CFG0/1	-0.3	+6.0	V
Analog Input Voltages: TEMP/TRK, TMON, VSENP, VSENN, ISENP, ISENN	-0.3	+6.0	V
Logic Reference: V1P5. ISHARE	-0.3	+3	V
Bias Supplies: V5, VG	-0.3	+6.0	V
Ground Voltage Differential (PGND - SGND)	-0.3	+0.3	V
PWM Drive: PWM	-0.3	+6.0	V
ESD Ratings	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package (Notes 5, 6)	37	2

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature	-55	+150	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{DD}	4.75	16	V
Input Supply Voltage Range, V_{DD},V_5, and V_G tied together	4.5	5.5	V
Output Voltage Range, V_{OUT}	0.45	5.5	V
Operating Junction Temperature Range, T_J	-40	+125	°C
Ambient Temperature Range, T_A	-40	+85	°C
5V (V5) Supply Total Supplied Current (Note 7)		5	mA
Drive Voltage (VG) Supply Total Supplied Current (Note 8)		40	mA

Notes:

7. θ_{JA} Total of current used by pull-ups to SDA, SCL, SALRT, DDC, EN, and PG (including Push-Pull configuration).
8. For Drive Voltage (VG), output current is limited by device thermal dissipation.

2.4 Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C.**

Parameter	Test Conditions	Min (Note 12)	Typ	Max (Note 12)	Unit
IC Input and Bias Supply Characteristics					
I_{DD} Supply Current	f_{SW} = 200kHz	-	20	30	mA
	f_{SW} = 1.00MHz	-	30	37	mA
I_{DD} Device Disabled Current	EN = 0V, SMBus inactive, V_{DD} = 12V, f_{SW} = 1MHz	-	20	28	mA
V5 Reference Output Voltage	V_{DD} > 6V, I < 5mA	4.75	5.0	5.25	V
V1P5 Reference Output Voltage	For reference only	1.45	1.5	1.55	V
VG Output Voltage	For reference only, V_{DD} = 12V	4.75	5.0	5.25	V
Output Characteristics					
Output Voltage Adjustment Range	V_{IN} > V_{OUT} + 1.1V	**0.45**	-	**5.5**	V
Output Voltage Set-Point Accuracy (Note 10)	Across line, load and temperature variation 1.0 ≤ V_{OUT} < 5.250; -40°C< T_A< 85°C	**-0.5**	±0.3	**0.5**	% V_{OUT}
	Across line, load and temperature variation 0.500 ≤ V_{OUT} < 1.0; 0°C< T_A <85°C	**-0.5**	±0.3	**0.5**	% V_{OUT}
	Across line, load and temperature variation 0.500 ≤ V_{OUT} < 1.0; -40°C< T_A <85°C	**-0.7**	±0.3	**0.7**	% V_{OUT}
Output Voltage Set-Point Resolution (Note 9)	Set using PMBus command	-	±0.05	-	% V_{OUT}
Output Voltage Positive Sensing Bias Current	VSENP = 5V (negative = out of pin)	0	-	20	µA
Output Voltage Negative Sensing Bias Current	VSENN = 0V, VSENP = 5V (negative = out of pin)	-20	-	0	µA
Logic Input/Output Characteristics					
Logic Input Leakage Current	Logic I/O - EN, DDC, SALRT, SDA, SCL, SYNC, PG (negative = out of pin)	-100	±20	100	nA
Logic Input Low, V_{IL}	ADVANCED_CONFIG[1] = 0	**-**	-	**0.8**	V
	ADVANCED_CONFIG[1] = 1			**0.4**	
Logic Input High, V_{IH}	ADVANCED_CONFIG[1] = 0	**2.05**	-	**-**	V
	ADVANCED_CONFIG[1] = 1	**1.2**			
Logic Output Pulldown Current	Open drain pins, V_{OL}= 0.5V	2	5		mA
PWM Output Characteristics					
PWM Output Low	2mA sinking	**-**	-	**0.5**	V
PWM Output High	2mA sourcing	**4.25**	-	**-**	V
Oscillator and Switching Characteristics					
Switching Frequency Range		**200**	-	**1000**	kHz
Switching Frequency Set-Point Accuracy		-7	-	7	%
Minimum SYNC Pulse Width	50% to 50%	**-**	200	**-**	ns
Input Clock Frequency Drift Tolerance	Maximum allowed drift of external clock	**-10**	-	**10**	%
External Clock Synchronization Window	Following POR	**50**			ms
PMBus Clock Frequency (Note 11)	Host cannot clock stretch such that clock frequency is ever below 10kHz	**10**	-	**1000**	kHz

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C. (Continued)**

Parameter	Test Conditions	Min (Note 12)	Typ	Max (Note 12)	Unit
Power Management					
Delay and Soft-Start Ramp Characteristics					
t_{ON} Delay/t_{OFF} Delay Range	Set using PMBus command	**0.1**	-	**125**	ms
t_{ON} Delay/t_{OFF} Delay Accuracy	Turn-on, turn-off delay < 50ms	-300	±50	300	µs
t_{ON} Ramp/t_{OFF} Ramp Duration Range	Set using PMBus command	**0**	-	**125**	ms
t_{ON} Ramp/t_{OFF} Ramp Duration Accuracy	t_{ON} Ramp, t_{OFF} Ramp <50ms	-300	±50	300	µs
Initialization Delay	V_{IN} > 4.5V, no other pending faults, device default settings only	-	10	15	ms
Tracking					
VTRK Input Bias Current	VTRK = 5V	**-**	25	**100**	µA
VTRK Regulation Accuracy	100% tracking, V_{OUT} -VTRK	**-2**		**2**	%V_{OUT}
Monitoring and Fault Management					
Input Voltage Monitor and Fault Detection					
V_{DD} UV Threshold Range		**4.25**	-	**16**	V
V_{DD} Monitor Accuracy	Full Scale (FS) = 16V	-2	-	+2	% FS
V_{DD} Monitor Resolution	Full Scale (FS) = 16V	-	±0.15	-	% FS
V_{DD} UV Fault Response delay		-	5	20	µs
Output Voltage Monitor and Fault Detection					
V_{OUT} Monitor Accuracy	VOUT_MAX = V_{SET} voltage (V_{OUT})	-1	-	+1	%
V_{OUT} Monitor Resolution	VOUT_MAX = V_{SET} voltage (V_{OUT})	-	±0.15	-	%
V_{OUT} UV/OV Fault Response Delay		-	5	20	µs
Output Current					
Output Current Sense Input Resolution					
Low Range	±15mV Full-Scale	-	15	-	µV
Medium Range	±30mV Full-Scale	-	30	-	µV
High Range	±60mV Full-Scale	-	60	-	µV
SPS Range	±400mV Full-Scale	-	0.4	-	mV
Output Current Sense Linearity Note: Total Error at Full Scale = Linearity + Offset					
Low Range	±15mV Full-Scale (Note 9)	-300	±200	300	µV
Medium Range	±30mV Full-Scale (Note 9)	-300	±200	300	µV
High Range	±60mV Full-Scale (Note 9)	-600	±300	600	µV
SPS Range	±400mV Full-Scale	-4.0	±3.0	4.0	mV
Output Current Sense Offset at 0V Input Note: Total Error at Full scale = Linearity + Offset					
Low Range	±15mV Full-Scale (Note 9)	-300	±200	300	µV
Medium Range	±30mV Full-Scale (Note 9)	-300	±200	300	µV
High Range	±60mV Full-Scale (Note 9)	-600	±300	600	µV
SPS Range	±400mV Full-Scale	-4.0	±3.0	4.0	mV

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A = -40°C to +85°C. (Continued)**

Parameter	Test Conditions	Min (Note 12)	Typ	Max (Note 12)	Unit
Temperature Sensing					
Internal Temperature Sensor					
Internal Temperature Accuracy		-	±2	-	°C
Internal Temperature Resolution		-	0.1	-	°C
External Temperature Sensor					
External Temperature Accuracy	Variation from device to device using reference diode. Tested with MMBT3904.	-	±2	-	°C
External Temperature Resolution		-	0.1	-	°C

Notes:

9. Percentage of Full Scale (FS) with temperature compensation applied.
10. V_{OUT} measured at the termination of the VSENP and VSENN sense points.
11. For operation at 400kHz and 1MHz, see PMBus Power System Management Protocol Specification Part 1, Section 5.2.6.2 for timing parameter limits.
12. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
13. 15mv, 30mV, and 60mV range characterized using a 2.74kΩ DCR time constant matching resistor.

3. ISL68301 Overview

The ISL68301 is an innovative mixed-signal power conversion and power management controller that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

The single channel ISL68301 can be configured to be part of a multiphase current sharing rail with up to eight phases.

The ISL68301's full digital loop achieves precise control of the entire power conversion process with no software required, resulting in a very flexible device that is very easy to use. The ChargeMode control algorithm is implemented to respond to output current changes within a single PWM switching cycle. This achieves a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

An extensive set of power management functions is fully integrated and can be configured using simple pin connections according to the tables provided in the following sections. The user configuration can be saved in an internal Nonvolatile Memory (NVRAM). Additionally, all functions can be configured and monitored through the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility. The ISL68301 is compliant with the PMBus specification. The "PMBus Command Summary" on page 34 contains a listing of all the PMBus commands supported by the ISL68301 and a detailed description of the use of each of these commands.

Additionally, a comprehensive set of tools and application notes is available to help simplify the design process. A demonstration board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. PowerNavigator, a Windows based GUI, is also provided to enable full configuration and monitoring capability through the PMBus interface and the included USB dongle.

3.1 Pin-Strap Pins

To simplify circuit design, the ISL68301 incorporates pin-strap pins that use a patented pin reader algorithm. This feature allows the user to easily configure many aspects of the device. When power is applied to the ISL68301, the IC reads the values of the pin-strap resistors and configures the IC accordingly. Each resistor value corresponds to a specific configuration setting. Values not listed as configuration resistor values should not be used. Resistors with a 1% tolerance must be used.

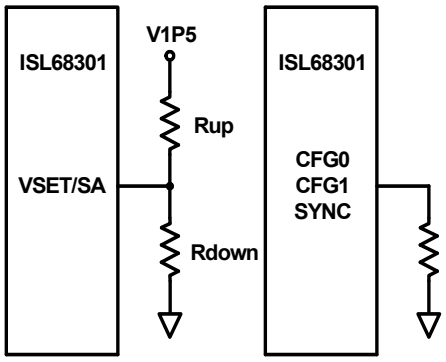


Figure 6. Pin-Strap Pins

3.1.1 Switching Frequency Setting (SYNC)

The device's switching frequency is set from 200kHz to 1MHz using the pin-strap method shown in Table 2 on page 16, or by using the FREQUENCY_SWITCH (33h) PMBus command. The ISL68301 generates the device switching frequency by dividing an internal precision 30MHz clock by integers from 30 (f_{SW} = 1MHZ) to 150 (f_{SW} = 200kHz). If a value other than f_{SW} = 30MHz/N is entered using a PMBus command, the internal circuitry selects the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 595kHz is entered, the device selects 600kHz (N = 50).

Table 2. SYNC Pin-Strap Settings

SYNC	kHz
6.98	250
8.45	300
10.0	353
11.5	400
13.3	455
15.4/Open	500
17.8	545
20.5	600

SYNC	kHz
23.7	652
27.4	698
31.6	750
36.5	811
42.2	857
48.7	909
56.2	968
64.9	1000

The ISL68301 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Renesas digital power devices.

When the SYNC pin is configured as an input pin, the incoming clock signal must be in the range of 200kHz to 1MHz and must be present within 50ms after POR and stable when the enable pin is asserted. The frequencies are not limited to discrete values as when using the internal clock. The internal switching frequency must be set as close as possible to the external clock signal frequency. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse-width of 200ns. In the event of a loss of the external clock signal, the ISL68301 sets the External Switching Period Fault bit in STATUS_MFR_SPECIFIC (80h) and shuts down. The device changes to its internal oscillator and switches at its programmed frequency upon re-enabling. To resume frequency synchronization, cycle POR with a valid clock signal applied at the SYNC pin or resend the USER_CONFIG_PMBUS command to “Select external clock”.

3.1.2 Configuration Setting (CFG0/1)

The configuration pins (CFG0, CFG1) set several device configuration settings, allowing the device to be used in applications without the need for loading configuration files with PMBus. The settings are shown in Table 3.

The device’s ChargeMode response can be optimized by adjusting the ASCR gain and residual settings, either by using the CFG1 pin-strap resistor method as shown in Table 3, or by using ASCR_CONFIG (DFh). When using Table 4 on page 17, the ASCR Residual is fixed at 79, and the ASCR integral gain is fixed at 100.

Table 3. CFG0/CFG1 Pin-Strap Settings

RCFG0 (kΩ)	Fault Response	Diode Emulation	Current Limit
6.98	Latch	Off	20
8.45/Open	Latch	Off	30
10.0	Latch	Off	40
11.5	Latch	Off	50
13.3	Latch	On	20
15.4	Latch	On	30
17.8	Latch	On	40
20.5	Latch	On	50
23.7	Retry	Off	20
27.4	Retry	Off	30
31.6	Retry	Off	40
36.5	Retry	Off	50

RCFG1 (kΩ)	ASCR Gain	Clock Sync
6.98	250	Internal Clock
8.45	300	Internal Clock
10.0/Open	400	Internal Clock
11.5	500	Internal Clock
13.3	600	Internal Clock
15.4	700	Internal Clock
17.8	800	Internal Clock
20.5	1000	Internal Clock
23.7	250	External Clock
27.4	300	External Clock
31.6	400	External Clock
36.5	500	External Clock

Table 3. CFG0/CFG1 Pin-Strap Settings (Continued)

RCFG0 (kΩ)	Fault Response	Diode Emulation	Current Limit
42.2	Retry	On	20
48.7	Retry	On	30
56.2	Retry	On	40
64.9	Retry	On	50

RCFG1 (kΩ)	ASCR Gain	Clock Sync
42.2	600	External Clock
48.7	700	External Clock
56.2	800	External Clock
64.9	1000	External Clock

Table 4. Current Limits

CFG0 Current Limit (A)	20	30	40	50
IOUT_OC_FAULT_LIMIT	20	30	40	50
IOUT_AVG_OC_FAULT_LIMIT	16	24	32	40
IOUT_OC_WARN_LIMIT	14	21	28	35
IOUT_AVG_UC_FAULT_LIMIT	-16	-24	-32	-40
IOUT_UC_FAULT_LIMIT	-20	-30	-40	-50

3.1.3 Output Voltage and SMBus Device Address Selection (VSET/SA)

When communicating with multiple SMBus devices using the SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 5.

Table 5. VSET/SA Pin-Strap Settings

V_{OUT}	Address 0x68		Address 0x69		Address 0x6A		Address 0x6B		Address 0x6C		Address 0x6D		Address 0x6E		Address 0x6F	
	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)
0.5	32.4	3.16	93.1	9.09	158	15.8	232	22.6	309	30.1	392	38.3	475	47.5	576	57.6
0.55	25.5	3.32	71.5	9.31	124	16.2	178	23.2	237	30.9	301	39.2	374	48.7	453	59.0
0.6	20.5	3.40	59.0	9.76	100	16.5	147	24.3	196	32.4	249	41.2	301	49.9	365	60.4
0.65	17.4	3.48	49.9	10.0	84.5	16.9	124	24.9	165	33.2	210	42.2	261	52.3	309	61.9
0.7	15.0	3.57	43.2	10.5	73.2	17.8	107	25.5	143	34.0	182	44.2	221	53.6	267	64.9
0.75	13.3	3.74	38.3	10.7	64.9	18.2	93.1	26.1	127	35.7	158	44.2	196	54.9	237	66.5
0.8	11.8	3.83	34.0	11.0	57.6	18.7	84.5	27.4	113	36.5	143	46.4	178	57.6	215	69.8
0.85	11.0	4.12	30.9	11.5	52.3	19.6	75.0	28.0	102	38.3	130	48.7	158	59.0	191	71.5
0.9	9.76	4.12	28.0	11.8	47.5	20.0	69.8	29.4	93.1	39.2	118	49.9	143	60.4	174	73.2
0.95	9.09	4.32	26.7	12.7	44.2	21.0	64.9	30.9	86.6	41.2	107	51.1	133	63.4	165	78.7
1	8.25	4.42	23.7	12.7	41.2	22.1	59.0	31.6	78.7	42.2	100	53.6	124	66.5	150	80.6
1.05	7.68	4.64	22.1	13.3	37.4	22.6	54.9	33.2	73.2	44.2	93.1	56.2	113	68.1	140	84.5
1.1	7.32	4.87	21.0	14.0	34.8	23.2	52.3	34.8	69.8	46.4	88.7	59.0	107	71.5	130	86.6
1.15	6.81	5.11	19.6	14.7	33.2	24.9	48.7	36.5	64.9	48.7	82.5	61.9	100	75.0	121	90.9
1.2	6.49	5.36	18.2	15.0	31.6	26.1	45.3	37.4	60.4	49.9	76.8	63.4	95.3	78.7	115	95.3
1.3	6.04	5.62	17.4	16.2	30.1	28.0	42.2	39.2	57.6	53.6	73.2	68.1	90.9	84.5	110	102
1.4	5.76	5.90	16.5	16.9	28.0	28.7	41.2	42.2	54.9	56.2	69.8	71.5	84.5	86.6	100	102
1.5	5.49	6.19	15.4	17.4	27.4	30.9	38.3	43.2	52.3	59.0	66.5	75.0	82.5	93.1	100	113
1.6	5.11	6.49	14.7	18.7	25.5	32.4	36.5	46.4	49.9	63.4	63.4	80.6	76.8	97.6	93.1	118

Table 5. VSET/SA Pin-Strap Settings (Continued)

V_{OUT}	Address 0x68		Address 0x69		Address 0x6A		Address 0x6B		Address 0x6C		Address 0x6D		Address 0x6E		Address 0x6F	
	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)	Rup (kΩ)	Rdown (kΩ)
1.7	4.99	6.98	14.3	20.0	24.3	34.0	35.7	49.9	47.5	66.5	60.4	84.5	75.0	105	88.7	124
1.8	4.87	7.68	13.7	21.5	23.2	36.5	33.2	52.3	45.3	71.5	57.6	90.9	69.8	110	84.5	133
1.9	4.52	7.87	13.0	22.6	22.6	39.2	32.4	56.2	43.2	75.0	54.9	95.3	69.8	121	84.5	147
2	4.42	8.66	12.4	24.3	21.5	42.2	30.9	60.4	42.2	82.5	53.6	105	64.9	127	78.7	154
2.1	4.22	9.31	12.1	26.7	20.5	45.3	30.1	66.5	40.2	88.7	51.1	113	63.4	140	75.0	165
2.2	4.12	10.2	11.5	28.7	20.0	49.9	28.7	71.5	39.2	97.6	49.9	124	60.4	150	73.2	182
2.3	4.02	11.5	11.0	31.6	19.1	54.9	27.4	78.7	37.4	107	46.4	133	59.0	169	69.8	200
2.4	3.92	12.7	11.0	35.7	19.1	61.9	26.7	86.6	35.7	118	47.5	154	57.6	187	68.1	221
2.5	3.65	14.0	10.5	40.2	17.8	68.1	26.1	100	34.8	133	44.2	169	54.9	210	64.9	249
Disabled	3.57	16.2	10.0	45.2	17.4	78.7	25.5	115	34	154	42.2	191	52.3	237	63.4	287
3.3	3.48	18.7	10.0	53.6	16.9	93.1	24.3	133	33.2	178	42.2	226	51.1	274	61.9	332
4.5	3.32	22.1	9.53	63.4	16.2	110	23.7	158	31.6	210	40.2	267	49.9	332	60.4	402
5	3.24	28.0	9.31	80.6	16.2	133	23.2	196	30.9	267	39.2	340	48.7	412	57.6	499

3.2 Start-Up and Shutdown Settings

Set the device's start-up and shutdown settings using the following PMBus Commands:

- TON_DELAY (60h): Sets the time from a low to high EN transition, or the receipt of an OPERATION command through PMBus, to the start of an output voltage ramp.
- TON_RISE (61h): Sets the time from the end of the TON_DELAY to the output voltage reaching regulation.
- TOFF_DELAY (64h): Sets the time from a high to low EN transition, or the receipt of an OPERATION command through PMBus, to the start of an output voltage ramp down.
- TOFF_FALL (65h): Sets the time from the end of the TOFF_DELAY to the output voltage reaching 0V.

3.3 Internal Bias Regulators and Input Supply Connections

The ISL68301 employs internal Low Dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

- **V5**: The V5 LDO provides a regulated 5V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X5R filter capacitor to SGND is required at the V5 pin. This supply can be used to provide a pull-up supply for DDC, SCL, SDA, SALRT and PG pins as long as load current does not exceed 5mA.
- **V1P5**: The V1P5 LDO provides a regulated 1.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 4.7µF ceramic X5R filter capacitor to SGND is required at the V1P5 pin. This voltage should only be used with the VSET/SA pin-strap resistors.
- **VG**: The VG LDO provides a regulated 5V bias supply for external MOSFET driver ICs or DrMOS integrated drivers/FETs. A 4.7µF ceramic X5R filter capacitor to PGND is required, however, additional capacitance is needed as specified by the MOSFET driver or DrMOS device selected. The maximum rated output current is 40mA, but device thermal limits must be considered. The power dissipated by the VG supply is (VDD-5V) x IDRV, where IDRV is the current supplied by the VG bias supply.

NOTE: The internal bias regulators, V5, and V1P5, are not designed to be outputs for powering other circuitry. The pin-strap resistors for VSET/SA must be connected to V1P5. The V5 supply can provide up to 5mA of pull-up current for the SDA, SCL, SALRT, DDC, and PG pins.

Operation with 5V V_{DD}: When operating the ISL68301 with 4.5V to 5.5V V_{DD}, the VG and V5 supplies should be connected directly to V_{DD} for best performance.

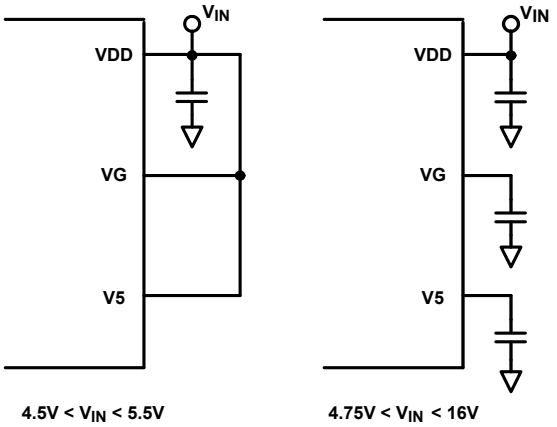


Figure 7. Supply Connections

3.4 Start-Up Procedure

The ISL68301 follows a specific internal start-up procedure after power is applied to the VDD pin, as shown in Figure 8. The device requires approximately 10-15ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values are loaded.

When this process is completed, the device is ready to accept commands through the serial interface and the device is ready to be enabled. If the device is synchronizing to an external clock source, the clock frequency must be stable before asserting the EN pin. When enabled, the device requires approximately 100µs before its output voltage is allowed to start its ramp-up process.

After the Ton-delay period expires, the output begins to ramp towards its target voltage according to the preconfigured Ton-rise time.

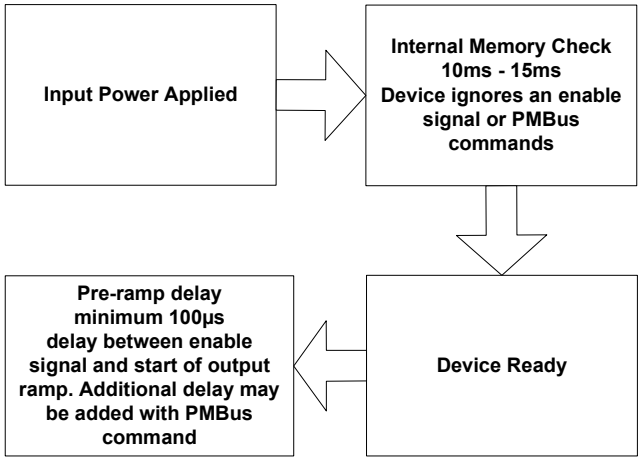


Figure 8. ISL68301 Internal Start-Up Procedure

V_{DD} should be above the ISL68301's VIN_UV_FAULT_LIMIT (59h) before the Enable pin is driven high. Following this sequence results in the most consistent turn-on delays. If a configuration file is needed to ensure

proper circuit operation (when V_{DD} is first applied to the ISL68301, for example) during initial PCB turn-on and test, the Enable pin must be driven low by some means until the ISL68301 configuration file is loaded. If the Enable pin is not held low, the ISL68301 may attempt to turn on with incorrect configuration settings, possibly causing circuit failure.

3.5 Ton-Delay and Rise Times

TON_RISE (61h) and TOFF_FALL (65h) are initially set to 5ms. TON_DELAY (60h) and TOFF_DELAY (64h) are initially set to 0ms. In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period expires. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL68301 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The Ton-delay time begins when the EN pin is asserted. Set the Ton-delay time using the PMBus command TON_DELAY (60h).

The Ton-rise time enables a precisely controlled ramp to the nominal V_{OUT} value that begins when the Ton-delay time expires. The ramp-up is monotonic and its slope can be precisely set using the PMBus command TON_RISE.

The Ton-delay and Ton-ramp times can be set using PMBus commands TON_DELAY (60h) and TON_RISE (61h) over the serial bus interface. When the Ton-delay time is set to 0ms, the device begins its ramp after the internal circuitry has initialized, which takes approximately 100µs to complete. The Ton-rise time can be set to values less than 125ms; however, the Ton-rise time should be set to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current. A lower Ton-rise time limit can be estimated using the formula:
Ton-rise = C_{OUT}*V_{OUT}/I_{LIMIT}, where C_{OUT} is the total output capacitance, V_{OUT} is the output voltage, and I_{LIMIT} is the current limit setting for the ISL68301.

When using interdevice current sharing, the TON_DELAY and the TON_RISE times of each device in the same current sharing rail must be set to the same values.

3.6 Enable Pin Operation and Timing

Use the enable pin (EN) to enable and disable the ISL68301. Drive the EN pin low whenever a configuration file or script is used to configure the ISL68301, or a PMBus command is sent that could potentially damage the application circuit. When the ISL68301 is used in a self-enabled mode, for example, when EN is tied to V5, or to a resistor divider from VIN, consider the ISL68301's default factory settings. When a configuration file is used to configure the ISL68301, the factory default settings are restored to both the user and default stores to set the device to an initialized state. Because the default state of the ISL68301 is to be enabled when the EN pin is high, the ISL68301 can be enabled while the PMBus commands are sent to the device during the configuration process.

The EN pin is edge triggered to achieve fast turn-off times. As a result, minimum Enable high and Enable low pulse-widths must be observed to ensure correct operation. The minimum high and low pulse widths are dependent on the configured rise, fall, and delay times and can be calculated using Equations 1 and 2:

$$\text{EN low} > \text{TOFF\_DELAY} + \text{TOFF\_FALL} + 10.5\text{ms} \quad \text{(EQ. 1)}$$

$$\text{EN high} > \text{TON\_DELAY} + \text{TON\_RISE}(\text{POWER\_GOOD\_DELAY} + 5.5\text{ms}) \quad \text{(EQ. 2)}$$

EN low and EN high times shorter than these minimums may result in the device not responding to the trailing edge of the pulse. For example, a EN low pulse below the EN low minimum pulse width may stay in the OFF state until a valid EN low pulse is applied to the EN pin.

The EN pin can be configured for fast fault-spreading through the USER_CONFIG (D1h) command. For example, in current sharing applications, the EN pins of the devices in the current sharing rail can be tied together, and can be configured for fault-spreading. When one device detects fault condition, it can disable other devices that are

connected to the same EN bus. When used in this manner, there is 20µs typical delay time for fault response. In the event of a fault, the EN pin is pulled down internally. As such, a pull-up resistor must be used for the EN bus.

3.7 Power-Good

The ISL68301 provides a Power-Good signal (PG) that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the configuration of the pin can be changed using the POWER_GOOD_ON (5Eh) and USER_CONFIG (D1h) commands.

A PG delay period is defined as the time from when all conditions within the ISL68301 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ISL68301 PG delay is set equal to 1ms. Set the PG delay using the PMBus command as described in POWER_GOOD_DELAY (D4h).

4. Power Management Functional Description

4.1 Input Voltage Undervoltage and Overvoltage Protections

The input undervoltage protection prevents the ISL68301 from operating when the input falls below a preset threshold, indicating that the input supply is out of its specified range. The input voltage undervoltage protection threshold can be set or changed using the VIN_UV_FAULT_LIMIT (59h) command. When an input undervoltage fault condition occurs, the user can determine the desired response to the fault condition. The following input undervoltage protection response options are available:

• **Latch:** Shut down and stay off until the fault has cleared and the device has been disabled and reenabled

• **Retry:** Shut down and restart continuously after a delay

When the VIN_UV_FAULT_RESPONSE is set to retry, the device periodically checks that the input voltage has risen above the VIN_UV_WARN_LIMIT before attempting to restart. Refer to VIN_UV_FAULT_RESPONSE (5Ah) for details about selecting specific undervoltage fault response options using the VIN_UV_FAULT_RESPONSE command.

The ISL68301 also offers input overvoltage protection. The input voltage overvoltage protection threshold can be set or changed using the VIN_OV_FAULT_LIMIT (55h) command. When an input overvoltage fault condition occurs, the user can determine the desired response to the fault condition. The following input overvoltage protection response options are available:

• **Latch:** Shut down and stay off until the fault has cleared and the device has been disabled and reenabled

• **Retry:** Shut down and restart continuously after a delay

When the VIN_OV_FAULT_RESPONSE is set to retry, the device periodically checks that the input voltage has fallen below the VIN_OV_WARN_LIMIT before attempting to restart. Refer to VIN_OV_FAULT_RESPONSE (56h) for details about selecting specific overvoltage fault response options using the VIN_OV_FAULT_RESPONSE command.

4.2 Output Overvoltage and Undervoltage Protections

The ISL68301 has internal output overvoltage protection circuitry that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. The output voltage sensed through the VSENSE pins is digitized and then compared to a programmable threshold set by VOUT_OV_FAULT_LIMIT. If the VSEN voltage exceeds this threshold, the PG pin deasserts and the device can respond as follows:

• **Latch:** Shut down and stay off until the fault has cleared and the device has been disabled and reenabled

• **Retry:** Shut down, and attempt to restart when the fault is no longer present

When the VOUT_OV_FAULT_RESPONSE is set to retry, the device periodically checks that the output voltage has fallen below the VOUT_OV_WARN_LIMIT prior to attempting restart.

Refer to VOUT_OV_FAULT_RESPONSE (41h) for details on how to select specific overvoltage fault response options using the VOUT_OV_FAULT_RESPONSE command.

The output voltage sensed through the VSEN pins is also used for the output voltage undervoltage protection circuit. This fault is masked during the output voltage ramps, before the power-good signal is asserted. The VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. When an output undervoltage condition is detected, the device can respond as follows:

• **Latch:** Shut down and stay off until the fault has cleared and the device has been disabled and reenabled

• **Retry:** Shut down, and when the fault is no longer present, attempt to restart

When the VOUT_UV_FAULT_RESPONSE is set to retry, the device attempts to soft-start the output voltage after the delay time expires. Refer to VOUT_UV_FAULT_RESPONSE (45h) for details about selecting specific overvoltage fault response options using the VOUT_UV_FAULT_RESPONSE command.

4.3 Output Prebias Protection

The ISL68301 supports prebiased start-up operation in single device and multi-phase operation. An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a prebias condition exists at the output. The ISL68301 provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the desired output voltage is present after the Ton-delay time the ISL68301 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-up from the prebias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command.

The resulting output voltage rise time varies depending on the prebias voltage, but the total time elapsed from the end of the Ton-delay time to when the Ton-rise time is complete and the output is at the desired value matches the preconfigured ramp time (see Figure 9).

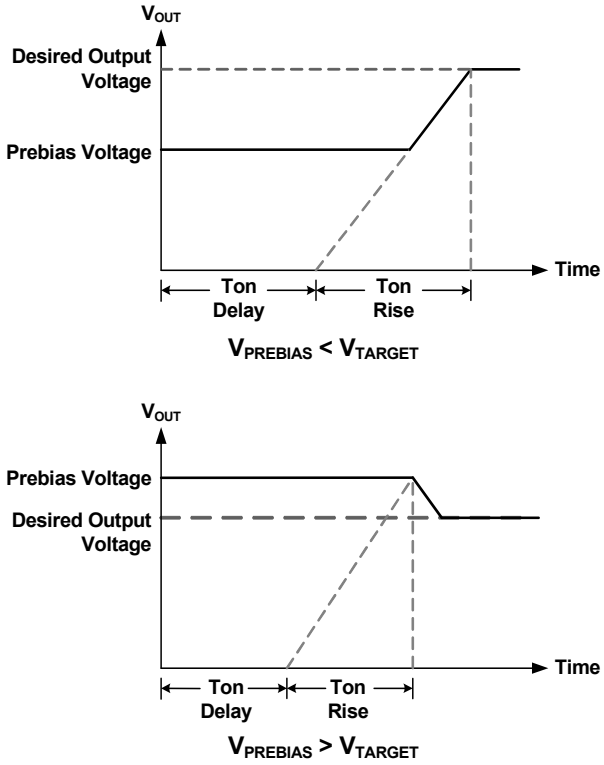


Figure 9. Output Responses to Prebias Voltages

If a prebias voltage higher than the target voltage exists after the preconfigured Ton-delay time and Ton-rise time have completed, the ISL68301 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-down from the prebias voltage is monotonic. The output voltage is then ramped down to the desired output voltage

Note: The ISL68301 uses the input voltage to calculate the initial duty cycle. To avoid an overshoot or undershoot on the output voltage, ISL68301's V_{DD} must be equal to the power stage's input voltage.

If a prebias voltage higher than the VOUT_OV_WARN_LIMIT (42h) limit exists, the device does not initiate a turn-on sequence and stays off.

4.4 Inductor Current Sensing

The ISL68301 supports DCR and SPS (IMON) current sensing schemes.

The ISENSE_CONFIG command contains two parameters related to current sensing. Current slope selection instructs the controller whether to use the up or down slope of the current signal. It is recommended that the down slope be used in low duty cycle applications and the up slope be used in high duty cycle applications. This command also sets the input range of the current sense ADC. The available options are ±15mV, 30mV, and 60mV for DCR sensing and ±400mV for SPS IMON.

4.4.1 SPS Current Sensing

By default, the ISL68301 is configured to sense inductor current using the IMON output from the ISL9922X Smart Power Stages (SPS). Connect the power stage IMON pin to the ISL68301 ISENP pin and the power stage REFIN pin to the ISL68301 ISENN/REFIN pin. In addition, connect the ISENN/REFIN pin to V1P5 through a 100Ω resistor, as shown in Figure 10.

Using an ISL9922x SPS device provides the best current sense accuracy with no action needed from the user.

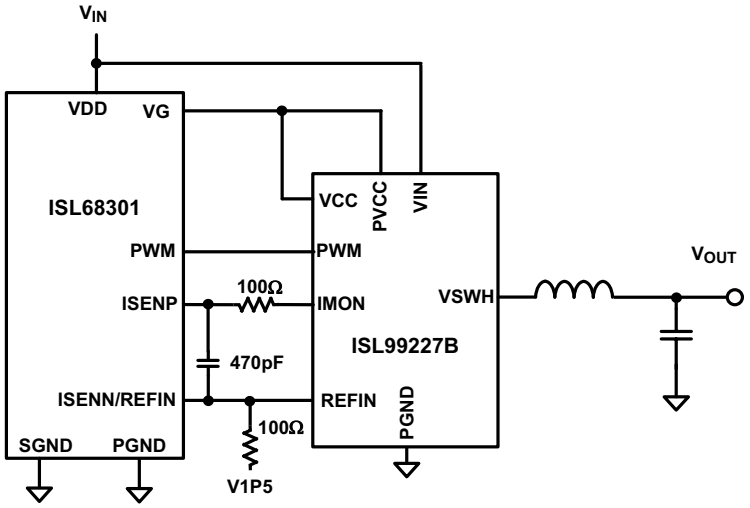


Figure 10. SPS Current Sensing

4.4.2 DCR Current Sensing

If using a DrMOS device, the ISL68301 can sense current through a wide range of inductor DCR values with matched RC networks. For the voltage across C_1 to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network.

$$\tau_{RC} = \tau_{L/DCR} \quad \text{(EQ. 3)}$$

$$R_1 \bullet C_1 = \frac{L}{DCR}$$

To achieve the best current sensing accuracy, it is recommended to use resistor value less than 5kΩ for R1. The capacitor, shown as C_1 in Figure 11, should be an X7R or better dielectric, and C_1 should be placed as close to the ISEN pins of ISL68301 as possible for the best noise performance.

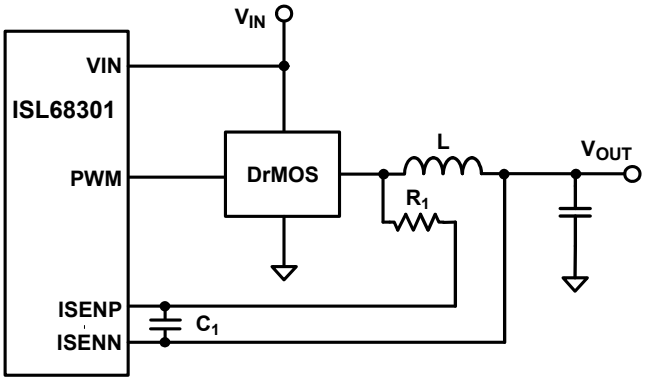


Figure 11. DCR Current Sensing

Set the L and DCR values using the INDUCTOR (D6h) and IOUT_CAL_GAIN (38h) commands. For L, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC bias, and switching frequency on the inductance when determining the minimum value of L. Use the typical room temperature value for DCR.

4.5 Diode Emulation Mode (DEM)

The ISL68301 features a Diode Emulation Mode (DEM) to improve the light load efficiency. DEM can be enabled by CFG0 pin strap setting or the POWER_MODE (34h) command.In this mode, when the ISL68301 detects a high-to-low zero crossing of the inductor current, the PWM signal is driven to the mid-level threshold (set by ADVANCED_CONFIG (E9h)), turning off both the high- and low-side MOSFETs until the next switching cycle.

4.6 Output Overcurrent and Undercurrent Protection

Depending on the configuration, the ISL68301 protects its load from overcurrent and reverse current conditions, for instance as the result of an output overload or a short to a higher voltage rail. The controller may perform the following actions:

- **Latch:** Shut off both the high and low output FETs until the output is disabled and re-enabled.
- **Retry:** Turn off the high and low output FETs, wait a configurable delay, then attempt to restart regulation. If the fault condition persists, the controller attempts to retry continuously.

Refer to the specifications of the MFR_IOUT_OC_FAULT_RESPONSE (E5h) and MFR_IOUT_UC_FAULT_RESPONSE (E6h) commands for more details.

The following commands configure OC/UC violation detection levels:

- IOUT_OC_FAULT_LIMIT (46h) and IOUT_UC_FAULT_LIMIT (4Bh) - These commands set the current value (A) above or below which the controller detects a peak or valley, respectively, violation.
- IOUT_AVG_OC_FAULT_LIMIT (E7h) and IOUT_AVG_UC_FAULT_LIMIT (E8h) - These commands set the value (A) above or below which controller detects the average of the entire sensed current slope during a switching cycle as a violation.

The ISENSE_CONFIG (D0h) command also allows the user to set the blanking time and the number of consecutive OC/UC readings required for a fault. The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after device switching (less accurate due to potential ringing). It is a configurable parameter from 0 to 832ns. The number of consecutive OC/UC readings that must occur before a fault and subsequent shutdown are initiated can be selected from the following: 1, 3, 5, 7, 9, 11, 13, or 15 consecutive readings.

4.7 Thermal Overload Protection

The ISL68301 includes an on-chip thermal sensor which continuously monitors internal die temperature, a TMON pin to monitor SPS die temperature, and the option to monitor the temperature of an external PN junction through the TEMP/TRK pin. The TEMP fault select bits of the USER_CONFIG (D1h) command select which of the available temperature telemetry signals the controller monitors to trigger over-temperature and under-temperature protection.

The OT_FAULT_LIMIT (4Fh) and UT_FAULT_LIMIT (53h) commands set the threshold above and below which the OT and UT fault response actions, respectively, are triggered. When the controller measures a temperature outside of those limits, it takes action specified by the settings of OT_FAULT_RESPONSE (50h) or UT_FAULT_RESPONSE (54h), accordingly. The available response actions are:

- **Latch:** Turn off both the high and low output FETs until the output is disabled and re-enabled
- **Retry:** Turn off the high and low output FETs until the temperature either falls below the value of OT_WARN_LIMIT (51h) (for OT faults) or above the value of UT_WARN_LIMIT (52h) (for UT faults). At that point, the controller waits a specified delay, then attempts to re-enable

Refer to the OT_FAULT_RESPONSE (50h) and UT_FAULT_RESPONSE (54h) commands for more details.

The default limits of OT_FAULT_LIMIT and UT_FAULT_LIMIT are 125ºC and -45ºC, respectively. Use of values outside of this range may result in permanent damage to the controller.

4.8 External Temperature Monitoring and Voltage Tracking (XTEMP/TRK)

The TEMP/TRK pin is a dual function pin which can either monitor the temperature of an external PN junction or provide input to the voltage tracking feature. The XTEMP/Tracking Select bits of the USER_CONFIG (D1h) command control this selection.

4.8.1 Temperature Monitoring Using XTEMP/TRK Pin

The ISL68301 supports measurement and reporting of an external temperature sensed through a PN junction such as a thermal diode integrated on a processor, FPGA, or ASIC, or a discrete diode connected BJT transistor (2N3904 recommended). Figure 12 illustrates the typical connections required. Use of the TEMP/TRK temperature sensing mode requires a capacitor (not exceeding 1000pF) connected in parallel with the sensing device to filter noise.

This temperature can trigger over temperature and under temperature faults if configured in USER_CONFIG (D1h). TEMPCO_CONFIG (DCh) allows use of this sensor for correction of DCR current sense signal for temperature, useful in the case that the inductor is placed far from the controller.

The XTEMP_SCALE (D9h) and XTEMP_OFFSET (DAh) commands provide calibration of the external temperature sense feature. The default values are intended for use with a diode connected 2N3904 NPN transistor. Use with other sensing devices may require adjustments to these commands due to differences in device parameters.

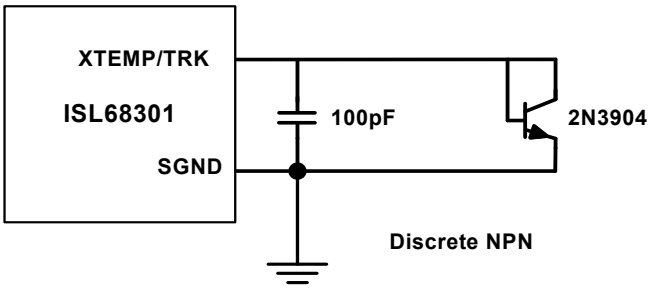


Figure 12. External Temperature Monitoring

4.8.2 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to manufacturer specifications.

The ISL68301 integrates a tracking scheme that allows one of its outputs to track a voltage that is applied to the XTEMP/VTRK pin with no external components required. The XTEMP/VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the XTEMP/VTRK pin to act as a reference for the device's output regulation. The ISl68301 provides two voltage tracking modes:

- **Coincident**. This mode configures the ISL68301 to ramp its output voltage at the same rate as the voltage applied to the XTEMP/VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady state output voltage, that is, the VOUT_COMMAND (21h) is set to the final output voltage.
- **Ratiometric**. This mode configures the ISL68301 to ramp its output voltage at a rate that is a percentage of the voltage applied to the XTEMP/VTRK pin. The two defined ratios are 50% and 100%. The default setting is 50%, but an external resistor string can be used to configure a different tracking ratio.

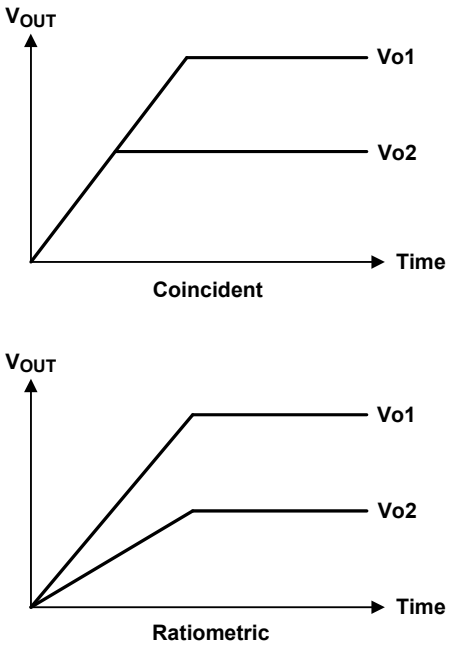


Figure 13. Tracking Modes

Soft-start settings (TON_DELAY and TON_RISE) are ignored when voltage tracking is enabled and the output takes the characteristics of the tracked voltage. POWER_GOOD_DELAY is still applied. Sequencing events, including enable and disable, are also ignored.

Limit - The output voltage of the tracking controller may be limited by either the target voltage of the tracking controller or the tracked voltage. If tracked voltage limitation is chosen, the controller ignores changes to VOUT_COMMAND (21h) and margins.

The maximum tracking signal input's rise time is 1V/ms. The device must be enabled at least 100µs before the tracking signal ramps up.

If the voltage at the TEMP/TRK pin is greater than 0V prior to the controller being enabled, the tracking voltage rises at the rate set by VOUT_TRANSITION_RATE (27h) until it reaches the correct ratio of the tracked

voltage. The input tracking signal should not ramp up until the output voltage completes the initial ramp. The time duration for the output voltage to complete the initial ramp can be estimated using Equation 4.

$$TRK_{INPUT\_DELAY} > \frac{Tracking\_Ratio \cdot Prebiased\_Input\_TRK\_Voltage}{VOUT\_TRANSITION\_RATE} + 100\mu s \quad \text{(EQ. 4)}$$

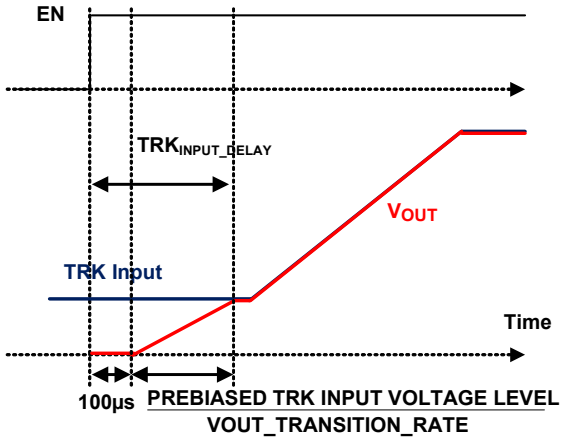


Figure 14. Tracking With Prebiased Input Tracking Signal, 100% Ratio, VTRK Limit Mode

To properly track during the turn-off ramp down, the TOFF_DELAY (64h) must be set be long enough to ensure that the IC is turned off after the tracking input signal ramps down to the final value.

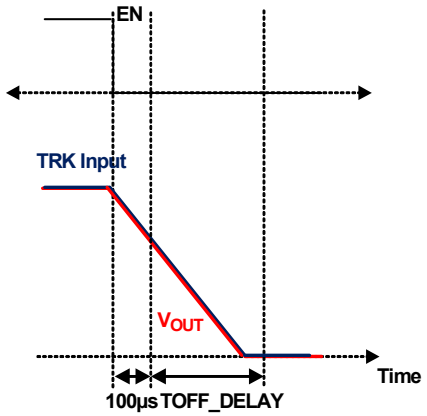


Figure 15. Tracking With Prebiased Input Tracking Signal, 100% Ratio, VTRK Limit Mode

4.9 Thermal Monitoring

The thermal monitoring (TMON) pin monitors the internal SPS device's temperature. Connect the ISL68301's TMON pin to the SPS's TMON pin (or TMON bus of the SPS devices for multiphase applications). The ISL68301 digitizes the voltage on the TMON pin and converts it into temperature data (degrees Celsius), which can be read with the READ_TEMPERATURE_3 (8Fh) command. The USER_CONFIG (D1h) command enables and disables the TMON functions and selects TMON for the temperature fault source.

The voltage is read on this pin and converted to a temperature by the following equation:

$$Temperature(°C) = \frac{V_{TMON} - 0.6}{0.008} \quad \text{(EQ. 5)}$$

Voltages above 2.5V on the TMON pin cause the device to automatically shut down and latch off, regardless of the OT_FAULT_LIMIT (4Fh) setting or if TMON is being used for over-temperature faults.

4.10 Control Loop Tuning

The ISL68301 incorporates the fully digital ChargeMode control modulation scheme. By default, this control loop is stable for a wide range of output filters and loads; however, it can be further tuned to achieve higher performance under more specific application requirements.

Because the control scheme is digital from end to end, it is implemented entirely within the controller. There is no dependence upon external compensation networks. This simplifies the design process by removing considerations such as temperature and process variation of passive components. Control parameters are instead set by the PMBus commands ASCR_CONFIG (DFh) and ASCR_ADVANCED (D5h).

The ASCR gain parameter (ASCR_CONFIG[15:0]) represents the scaling of the error voltage as applied to setting the PWM pulse-width. Increasing this parameter decreases the time the controller takes to respond to a transient event, but incorporates more high frequency noise into the loop. This value is the dominant parameter in transient response. Renesas recommends increasing this parameter until the loop response time is sufficient for the application, but no more. Setting the ASCR gain parameter too high can lead to excessive output voltage ripple due to increased PWM jitter. The default value of this parameter is controlled by setting the CFG1 pin-strap value.

Integral gain (ASCR_CONFIG[31:24]) controls DC accuracy and the time taken to return to the voltage set point following a transient event. When ASCR gain is set appropriately, decrease integral gain while output voltage deviation is still acceptable.

Residual gain (ASCR_CONFIG[23:16]) is analogous to damping. The residual gain removes or adds some fractional portion against the deviation of the PWM pulse width from steady state duty cycle in the next switch cycle created by the gain parameter. Increasing this parameter decreases output overshoot, but prolongs the recovery to DC following a load transient. Its effect is delayed by one cycle relative to the gain effect and as such it does not affect the peak voltage deviation during the transient, only the return to steady state.

In addition to the basic loop parameters, the ISL68301 incorporates a digital steady state gain reduction circuit to provide low jitter steady state operation while maintaining fast transient response. This circuit compares the error signal to the threshold set with ASCR_ADVANCED[11:0] over a period of time. If the error remains low, the controller begins dividing down the gain parameter according to the setting of ASCR_ADVANCED[13:12] to decrease the effect of high frequency noise on PWM pulse width. If the error exceeds the threshold in any cycle, the controller immediately reverts to the full gain setting to handle the transient.

When the ASCR_CONFIG (DFh) settings are chosen and the output voltage ripple is acceptable in the application steady state conditions, increase the ASCR threshold setting until the gain reduction activates.

4.11 SMBus Communications

The ISL68301 provides a SMBus digital interface. The ISL68301 can be used with any standard 2-wire SMBus host device. The device is also compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor can be tied to V5 or to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. Limit the minimum pull-up resistance to a value that enables any device to assert the bus to a voltage that ensures a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to V5) and the pull-down current capability of the ISL68301(nominally 4mA). A 10kΩ resistor on each line provides good performance on an SMBus with fewer than 10 devices.

Route SMBus data and clock lines with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V respectively causes command transmissions to be interrupted and results in slow bus operation or missed commands.

The ISL68301 accepts most standard PMBus commands. When enabling the device with the ON_OFF_CONFIG (02h) command, it is recommended that the EN pin is tied to SGND.

In addition to bus noise considerations, ensure that user connections to the SMBus are compliant to the PMBus command standards. Any device that can malfunction in a way that permanently shorts SMBus lines disables PMBus communications. Incomplete PMBus commands can also cause the ISL68301 to halt PMBus communications. This can be corrected by disabling, then reenabling the device.

4.12 Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Renesas Digital-DC devices, and within the ISL68301 itself. This dedicated bus provides the communication channel between devices for features such as sequencing, and fault spreading. **The DDC pin must be pulled-up to an external 3.3V or 5.0V supply**. In addition, the DDC pin must be pulled up before the EN pin is set high. The DDC pin on all Digital-DC devices that utilize sequencing, fault spreading, or current sharing must be connected together. A pull-up resistor is required on the DDC bus to guarantee the rise time as follows:

$$\text{Riset time} = R_{PU} \bullet C_{LOAD} \leq 1\mu s \quad \text{(EQ. 6)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading.

The pull-up resistor can be tied to V5 or to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. Generally, each device connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, consider whether to place the pull-up resistor on the module or on the PCB of the end application. Limit the minimum pull-up resistance to a value that enables any device to assert the bus to a voltage that ensures a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to V5) and the pull-down current capability of the ISL68301 (nominally 4mA). As with SMBus data and clock lines, route the DDC data line with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the DDC signal can cause the voltage on this line to cross the high and low logic thresholds of 2.0V and 0.8V, respectively, causes command transmissions to be interrupted, and results in slow bus operation or missed commands. A 10kΩ resistor provides good performance on a DDC bus with fewer than 10 devices.

4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device so that not all devices have coincident rising edges. Set each converter to start its switching cycle at a different point in time to dramatically reduce input capacitance requirements. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to I_{RMS}^2 are reduced.

To enable phase spreading, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in "Pin Descriptions" on page 6. The phase offset of each device can also be set to any value between 22.5° and 360° in 22.5° increments using the INTERLEAVE (37h) PMBus command.

4.14 Output Sequencing

A group of Renesas digital power devices can be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage before another supply reaching its operating voltage to avoid latch-up from occurring. Multidevice sequencing can be achieved by configuring each device using the SEQUENCE PMBus command.

Multiple device sequencing is achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows in the sequencing chain.

The Enable (EN) pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. EN must be driven low to initiate a sequenced turn-off of the group. To achieve sequenced turn-off of a group of sequenced devices, configure all the devices to turn off using the "soft-off", or ramped down behavior, in the ON_OFF_CONFIG (02h) PMBus command.

When sequencing on, the first device to ramp up, called the “prequel”, sends a message through the DDC bus to the next device, called the “sequel” when the prequel’s Power-Good (PG) signal is driven high.

When sequencing off, the sequel sends a message to the prequel to begin the prequel’s ramp down after the sequel completes its own ramp down.

Sequencing can also be accomplished by connecting the EN pin of a sequel device to the Power-Good pin of a prequel device. Sequencing is also achieved by using the TON_DELAY (60h) and TON_RISE (61h) commands and choosing appropriate delay and rise durations so that sequel devices start after their associated prequel devices. The drawback to this method is that if a prequel device fails to start properly, its sequel device still starts and ramps on according to its delay and rise time settings.

4.15 Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a fault occurs and the device is configured to shut down on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down together if configured to do so, and attempt to restart in their prescribed order if configured to do so.

4.16 Active Current Sharing

Up to eight ISL68301 devices can be paralleled together for current sharing operation. The device outputs share the current equally within a few percent, assuming all external sensing element variations and tolerances are negligible. Current sensing element tolerances must be taken into account, or adjusted for using the IOUT_CAL_GAIN (38h) and IOUT_CAL_OFFSET (39h) commands in any application.

In the current sharing operation, ISL68301 uses a digital current sharing bus to communicate and balance the current from each devices. Use DDC_CONFIG (D3h) to set current sharing rail operation. The master device in the current sharing rail drives the ISHARE bus with its sensed current information. The slave devices then use the current information from the master device as the reference current for current balancing. Only one master device is allowed per one current sharing rail. By default, the phase spreading is configured automatically based on the number of devices on the current sharing rail.

For the current sharing operation, connect the ISHARE, EN, DDC, and SYNC pins to their buses for the devices in the same current sharing rail, as shown in Figure 5 on page 10.

NOTE: the VSENP and VSENN for each device in the current sharing rail must be connected to the output voltage.

4.17 Nonvolatile Memory and Security Features

The ISL68301 stores user configurations in internal nonvolatile memory. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. During the initialization process, the ISL68301 checks for stored values contained in its internal nonvolatile memory. The ISL68301 offers two internal memory storage units that are accessible by the user as follows:

- **User Store**: The user store is the most commonly used store. It provides the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the user store to achieve this goal.
- **Default Store**: The default store is less commonly used. It provides a means to protect the circuit from damage by preventing the user from modifying certain values that are related to the physical construction of the circuit. In this case, the Original Equipment Manufacturer (OEM) would use the default store in a protected mode and allow the user to restore the device to its default settings. In this case the user store would be available to the end-user for making changes, but would restrict the user from restoring the device to the factory settings or modifying the default store.

The user store takes priority over the default store. If no values are set in the user or default store, the device uses the pin-strap setting value.

For details about protection of the user and default stores, see the PASSWORD (FBh) command.

4.18 Monitoring Through SMBus

A system controller can monitor a wide variety of different ISL68301 parameters through the SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which is asserted when any number of preconfigured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including, but not limited to, the following:

- Input voltage
- Output voltage
- Input current
- Output current
- Internal junction temperature
- Temperature of an external device
- Switching frequency
- Duty cycle
- Fault status information

The PMBus Host should respond to SALRT as follows:

(1) Device pulls SALRT low.

(2) PMBus host detects that SALRT is now low, and performs transmission with Alert Response Address to find which device is pulling SALRT low.

(3) PMBus host talks to the device that pulled SALRT low. The actions that the host performs are up to the system designer.

If multiple devices are faulting, SALRT is still low after the above events and requires transmission with the Alert Response Address repeatedly until all faults are cleared.

Refer to "PMBus Command Detail" on page 40 for information about how to monitor specific parameters through the SMBus interface.

4.19 General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

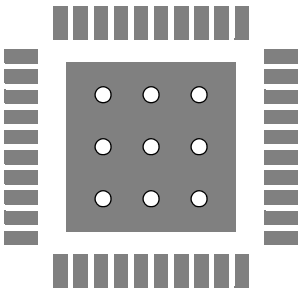


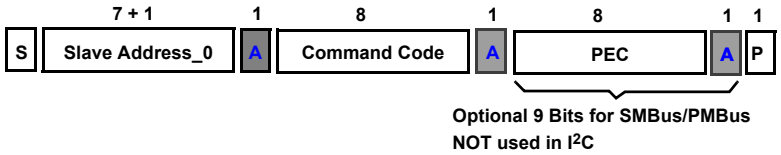
Figure 16. PCB Via Pattern

Renesas recommends filling the thermal pad area with vias. A typical via array fills the thermal pad footprint so that their centers are three times the radius apart from each other. Keep the vias small, but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated-through hole to each plane.

5. PMBus Protocol

1. Send Byte Protocol



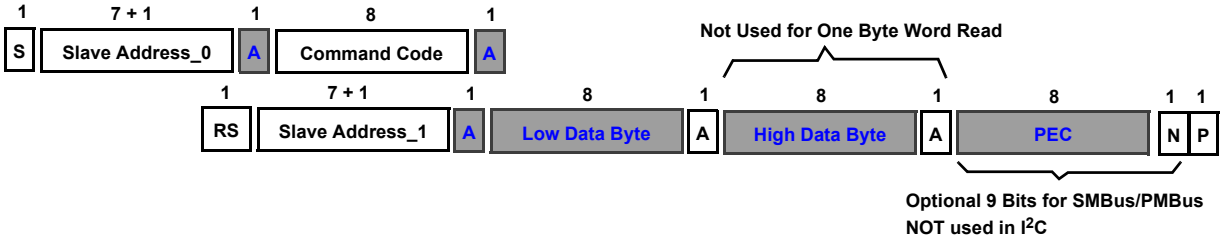
S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition
Acknowledge or DATA from Slave, ISL68301 Controller

Example command: 03h Clear Faults
(This will clear all of the bits in Status Byte for the selected Rail)

2. Write Byte/Word Protocol

Example command: 21h VOUT_COMMAND

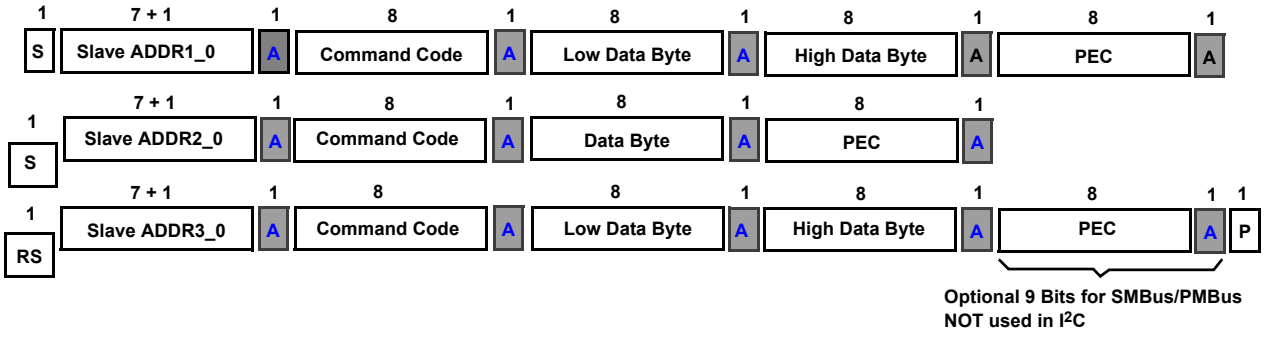
3. Read Byte/Word Protocol



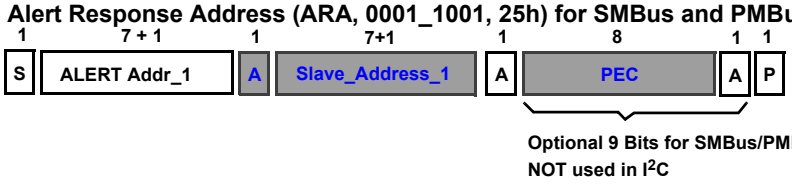
Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

The STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

4. Group Command Protocol - No more than one command can be sent to the same Address



5. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus, not used for I²C



6. PMBus Command Summary

Code	Command Name	Description	Type	Apply	Data Format	Default Value	Default Setting
01h	OPERATION	Enable/disable, margin settings	R/W	I	BIT	N/A	N/A
02h	ON_OFF_CONFIG	On/off configure settings	R/W	I	BIT	17h	EN pin control, active high
03h	CLEAR_FAULTS	Clears faults	Write	I	N/A	N/A	N/A
11h	STORE_DEFAULT_ALL	Transfers values to default store	Write	I	N/A	N/A	N/A
12h	RESTORE_DEFAULT_ALL	Restores values from default store	Write	I	N/A	N/A	N/A
15h	STORE_USER_ALL	Transfers values to user store	Write	I	N/A	N/A	N/A
16h	RESTORE_USER_ALL	Restores values from user store	Write	I	N/A	N/A	N/A
19h	CAPABILITY	Reports on several device capabilities	Read	I	BIT	D0h	Device capabilities
20h	VOUT_MODE	Reports VOUT_COMMAND Mode value	Read	I	BIT	13h	-13d, fixed value
21h	VOUT_COMMAND	Sets nominal V_{OUT} setpoint	R/W	I	L16u	N/A	VSET/SA pin-strap setting
22h	VOUT_TRIM	Applies a trim voltage to V_{OUT} setpoint	R/W	I	L16u	0000h	0V
23h	VOUT_CAL_OFFSET	Applies offset voltage to V_{OUT} setpoint	R/W	I	L16u	0000h	0V
24h	VOUT_MAX	Sets maximum V_{OUT} setpoint	R/W	D	L16u	N/A	1.15 x VOUT_COMMAND pin-strap setting
25h	VOUT_MARGIN_HIGH	Sets V_{OUT} setpoint during margin high	R/W	I	L16u	N/A	1.05 x VOUT_COMMAND pin-strap setting
26h	VOUT_MARGIN_LOW	Sets V_{OUT} setpoint during margin low	R/W	I	L16u	N/A	0.95 x VOUT_COMMAND pin-strap setting
27h	VOUT_TRANSITION_RATE	Sets V_{OUT} transition rate during margin commands	R/W	I	L11	BA00h	1V/ms
32h	MAX_DUTY	Sets maximum PWM duty cycle	R/W	D	L11	EAD0h	90%
33h	FREQUENCY_SWITCH	Sets switching frequency	R/W	D	L11	N/A	SYNC pin-strap setting
34h	POWER_MODE	Sets Diode Emulation mode	R/W	I	BIT	N/A	Config 0 pin-strap setting
37h	INTERLEAVE	Configures phase offset during group operation	R/W	D	BIT	0000h	No phase shift
38h	IOUT_CAL_GAIN	Sets impedance of current sense circuit	R/W	I	L11	CA66h	4.8mΩ (mV/A)
39h	IOUT_CAL_OFFSET	Sets an offset to I_{OUT} sense circuit	R/W	I	L11	0000h	0A
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold	R/W	I	L16u	N/A	1.10 x VOUT_COMMAND pin-strap setting

Code	Command Name	Description	Type	Apply	Data Format	Default Value	Default Setting
41h	VOUT_OV_FAULT_RESPONSE	Sets the V_{OUT} overvoltage fault response	R/W	D	BIT	N/A	Config 0 pin-strap setting
42h	VOUT_OV_WARN_LIMIT	Sets the V_{OUT} overvoltage warn threshold	R/W	I	L16u	N/A	1.08 x VOUT_COMMAND pin-strap setting
43h	VOUT_UV_WARN_LIMIT	Sets the V_{OUT} undervoltage warn threshold	R/W	I	L16u	N/A	0.9 x VOUT_COMMAND pin-strap setting
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold	R/W	I	L16u	N/A	0.85 x VOUT_COMMAND pin-strap setting
45h	VOUT_UV_FAULT_RESPONSE	Sets the V_{OUT} undervoltage fault response	R/W	D	BIT	80h	Config 0 pin-strap setting
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold for each phase	R/W	I	L11	N/A	Config 0 pin-strap setting
4Ah	IOUT_OC_WARN_LIMIT	Sets the I_{OUT} peak overcurrent warn threshold for each phase	R/W	I	L11	N/A	0.70 x IOUT_OC_FAULT_LIMIT pin-strap setting
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold for each phase	R/W	I	L11	N/A	-1.0 x IOUT_OC_FAULT_LIMIT pin-strap setting
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault limit	R/W	I	L11	EBE8h	+125˚C
50h	OT_FAULT_RESPONSE	Sets the over-temperature fault response	R/W	D	BIT	80h	Config 0 pin-strap setting
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit	R/W	I	L11	EB70h	+110°C
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit	R/W	I	L11	DC40h	-30°C
53h	UT_FAULT_LIMIT	Sets the under-temperature fault limit	R/W	I	L11	E530h	-45°C
54h	UT_FAULT_RESPONSE	Sets the under-temperature fault response	R/W	D	BIT	80h	Config 0 pin-strap setting
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold	R/W	I	L11	DA00h	16V
56h	VIN_OV_FAULT_RESPONSE	Sets the V_{IN} overvoltage fault response	R/W	D	BIT	80h	Config 0 pin-strap setting
57h	VIN_OV_WARN_LIMIT	Sets the V_{IN} overvoltage warning threshold	R/W	I	L11	D3E0h	15.5V
58h	VIN_UV_WARN_LIMIT	Sets the V_{IN} undervoltage warning threshold	R/W	I	L11	CB80h	7.0V
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold	R/W	I	L11	CB40h	6.5V
5Ah	VIN_UV_FAULT_RESPONSE	Sets the V_{IN} undervoltage fault response	R/W	D	BIT	80h	Config 0 pin-strap setting
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication	R/W	D	L16u		0.90 x VOUT_COMMAND pin-strap setting

Code	Command Name	Description	Type	Apply	Data Format	Default Value	Default Setting
60h	TON_DELAY	Sets the delay time from enable to V_{OUT} rise	R/W	D	L11	0000h	0ms
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY	R/W	D	L11	CA80h	5ms
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall	R/W	D	L11	0000h	0ms
65h	TOFF_FALL	Sets the fall time for VOUT after DISABLE and TOFF_DELAY	R/W	D	L11	CA80h	5ms
78h	STATUS_BYTE	First byte of STATUS_WORD	Read	I	BIT	00h	No faults
79h	STATUS_WORD	Summary of critical faults	Read	I	BIT	0000h	No faults
7Ah	STATUS_VOUT	Reports V_{OUT} warnings/faults	Read	I	BIT	00h	No faults
7Bh	STATUS_IOUT	Reports I_{OUT} warnings/faults	Read	I	BIT	00h	No faults
7Ch	STATUS_INPUT	Reports input warnings/faults	Read	I	BIT	00h	No faults
7Dh	STATUS_TEMPERATURE	Reports temperature warnings/faults	Read	I	BIT	00h	No faults
7Eh	STATUS_CML	Reports communication, memory, logic errors	Read	I	BIT	00h	No errors
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock synchronization faults	Read	I	BIT	00h	No faults
88h	READ_VIN	Reports input voltage measurement	Read	I	L11	N/A	N/A
89h	READ_IIN	Reports input current measurement	Read	I	L11	N/A	N/A
8Bh	READ_VOUT	Reports output voltage measurement	Read	I	L16u	N/A	N/A
8Ch	READ_IOUT	Reports output current measurement	Read	I	L11	N/A	N/A
8Dh	READ_TEMPERATURE_1	Reports internal temperature measurement	Read	I	L11	N/A	N/A
8Eh	READ_TEMPERATURE_2	Reports external temperature measurement from TEMP/TRK (Pin 4) if configured	Read	I	L11	N/A	N/A
8Fh	READ_TEMPERATURE_3	Reports external temperature measurement from TMON (Pin 15)	Read	I	L11	N/A	N/A
94h	READ_DUTY_CYCLE	Reports actual duty cycle	Read	I	L11	N/A	N/A
95h	READ_FREQUENCY	Reports actual configured switching frequency	Read	I	L11	N/A	N/A
96h	READ_POUT	Reports calculated output power	Read	I	L11	N/A	N/A
97h	READ_PIN	Reports calculated input power	Read	I	L11	N/A	N/A
98h	PMBUS_REVISION	Reports the PMBus revision used	Read	I	BIT	33h	P1 R1.3, P2 R1.3
99h	MFR_ID	Sets a user defined identification	R/W	I	ASC	N/A	<null>
9Ah	MFR_MODEL	Sets a user defined model	R/W	I	ASC	N/A	<null>

Code	Command Name	Description	Type	Apply	Data Format	Default Value	Default Setting
9Bh	MFR_REVISION	Sets a user defined revision	R/W	I	ASC	N/A	<null>
9Ch	MFR_LOCATION	Sets a user defined location identifier	R/W	I	ASC	N/A	<null>
9Dh	MFR_DATE	Sets a user defined date	R/W	I	ASC	N/A	<null>
9Eh	MFR_SERIAL	Sets a user defined serialized identifier	R/W	I	ASC	N/A	<null>
ADh	IC_DEVICE_ID	Reports device identification information	Read	I	CUS	49A02F00h	Renesas, ISL68301
AEh	IC_DEVICE_REV	Reports device revision information	Read	I	CUS	0900080Dh	Initial release
B0h	USER_DATA_00	Sets a user defined data	R/W	I	ASC	N/A	<null>
B1h	USER_DATA_01	Sets a user defined data	R/W	I	ASC	N/A	<null>
B2h	USER_DATA_02	Sets a user defined data	R/W	I	ASC	N/A	<null>
D0h	ISENSE_CONFIG	Configures current sensing circuitry	R/W	D	BIT	1903h	Downslope, 3 fault count, 96ns blanking, SPS range
D1h	USER_CONFIG	Configures several user-level features	R/W	D	BIT	1400h or 1402h	Config 1 pin-strap setting
D3h	DDC_CONFIG	Configures the DDC addressing and current sharing	R/W	D	BIT	N/A	Set by pin strapped PMBus address
D4h	POWER_GOOD_DELAY	Sets the delay between PG threshold and PG assertion	R/W	D	L11	BA00h	1ms
D5h	ASCR_ADVANCED	Sets ASCR Threshold and Threshold Gain	R/W	I	BIT	2064h	Gain Select divide by 4, threshold 100
D6h	INDUCTOR	Sets the inductance of both phases	R/W	D	L11	AA66h	0.30µH
D7h	SNAPSHOT_FAULT_MASK	Masks faults that cause a snapshot to be taken	R/W	I	BIT	0000h	No faults masked
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection	R/W	D	BIT	00h	Two violations trigger fault
D9h	XTEMP_SCALE	Calibrates external temperature sensor	R/W	I	L11	BA00h	1/°C
DAh	XTEMP_OFFSET	Offset calibration for external temperature sensor	R/W	I	L11	0000h	No offset
DBh	MFR_SMBALERT_MASK	Identifies which fault limits do not assert SALRT	R/W	D	Custom	000000000 00000h	N/A
DCh	TEMPCO_CONFIG	Sets tempco settings	R/W	I	BIT	00h	0ppm/°C
DFh	ASCR_CONFIG	Configures the ASCR settings	R/W	I	BIT	644F0190h	Config 1 pin-strap setting
E0h	SEQUENCE	DDC rail sequencing configuration	R/W	D	BIT	00h	Prequel and sequel disabled
E1h	TRACK_CONFIG	Configures voltage tracking modes	R/W	D	BIT	00h	Tracking disabled
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION, and V_{OUT}	R/W	D	BIT	001F1F1Fh	Ignore broadcast, sequenced shutdown, and fault spreading

Code	Command Name	Description	Type	Apply	Data Format	Default Value	Default Setting
E3h	STORE_CONTROL	Stores command settings in the USER and DEFAULT Stores while the device is enabled. Used in conjunction with STORE_DATA.	Write	I	BIT	N/A	N/A
E4h	DEVICE_ID	Returns the device identifier string	Read	I	ASC	ISL68301-0-G0101	Part number/die revision/firmware revision
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response	R/W	D	BIT	N/A	Config 0 pin-strap setting
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response	R/W	D	BIT	N/A	Config 0 pin-strap setting
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold for each phase	R/W	I	L11	N/A	0.8 x IOUT_OC_FAULT_LIMIT pin-strap setting
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold for each phase	R/W	I	L11	N/A	-0.8 x IOUT_OC_FAULT_LIMIT pin-strap setting
E9h	ADVANCED_CONFIG	Set PWM mid-drive voltage, SMBus I/O and enable/disable the VG LDO	R/W				
EAh	SNAPSHOT	32-byte read-back of parametric and status values	Read	I	BIT	N/A	N/A
EBh	BLANK_PARAMS	Indicates recently saved parameter values	Read	I	BIT	FF..FFh	N/A
F0h	LEGACY_FAULT_GROUP	Configures fault group compatibility with older Renesas digital power devices	R/W	D	BIT	00..00h	No fault groups selected.
F2h	STORE_DATA	Stores command settings in the USER and DEFAULT Stores while the device is enabled. Used in conjunction with STORE_CONTROL.	Write	I	Custom	N/A	N/A
F3h	SNAPSHOT_CONTROL	Snapshot feature control	R/W	I	BIT	00..00h	N/A
F4h	RESTORE_FACTORY	Restores device to the hard-coded default values	Write	I	N/A	N/A	N/A
F5h	PINSTRAP_READ_STATUS	Reads back an index for each pin-strap setting, CFG0, CFG1, VSET/SA, SYNC	Read	I	BIT	N/A	Pin-strap resistor indexes
F6h	IIN_CAL_OFFSET	Sets an offset to Iin sense circuit	R/W	I	L11	8BD7h	0.03A
FAh	SECURITY_CONTROL	Sets the security functions mode	R/W	I	BIT	N/A	N/A
FBh	PASSWORD	Sets the password string	Write	I	ASCII	00..00h	<null>
FDh	WRITE_PROTECT	Identifies which commands are protected	R/W	I	Custom	00..00hh	N/A

Read = Read only, Write = Write-only, R/W = Read and Write.
I = Command or command setting takes effect immediately, D = Command setting takes effect after device is disabled.
N/A = Not Applicable, <null> = All bytes are 00h.
For Data Type explanations, see "PMBus Data Formats" on page 39.

6.1 PMBus Use Guidelines

PMBus is a powerful tool that allows users to optimize circuit performance by configuring the ISL68301 for their application. When configuring the ISL68301 in a circuit, the ISL68301 should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL, and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Summary:

All commands can be read at any time.

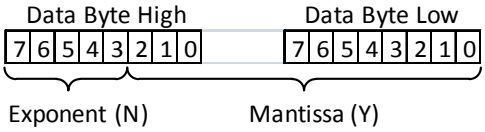
Always disable the ISL68301 when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then disable and re-enable the device.

6.2 PMBus Data Formats

Linear-11 (L11)

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X).



The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)

The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)

The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X).
The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)

A description of the Bit Field format is provided in "PMBus Command Detail" on page 40.

Custom (CUS)

A description of the Custom data format is provided in "PMBus Command Detail" on page 40. A combination of Bit Field and integer are a common type of Custom data format.

ASCII (ASC)

A variable length string of text characters that uses the ASCII data format.

7. PMBus Command Detail

OPERATION (01h)

Definition: Sets Enable, Disable, and V_{OUT} Margin settings. Writing Immediate off turns off the output and ignores TOFF_DELAY and TOFF_FALL settings. With Immediate off, the PWM signal is set to tri-state level without delay. This command is not stored like other PMBus commands. When this command is written, the command takes effect, but if a STORE _USER_ALL written and the device is re-enabled, the OPERATION settings may not be the same settings that were written before the device was re-enabled. This command reflects only the last value written. Read the STATUS_BYTE/WORD command for the enable state.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: No

Default Value: 00h

Units: N/A

Command	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A							

Bits	Purpose	Bit Value	Meaning
7	Controls device output state	0	Off (see ON_OFF_CONFIG)
		1	On (see ON_OFF_CONFIG)
6	Turn off behavior. This bit is ignored if Bit 7 = 1	0	Ignore TOFF_DELAY and TOFF_FALL
		1	Observe TOFF_DELAY and TOFF_FALL.
5:4	Output voltage.	00	V_{OUT} is set by VOUT_COMMAND
		01	V_{OUT} is set by VOUT_MARGIN_LOW
		10	V_{OUT} is set by VOUT_MARGIN_HIGH
		11	Not used
3:2	Margin Fault Response	00	Not used
		01	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are ignored.
		10	Faults caused by VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW are acted on.
		11	Not used
1:0	Not used	00	Not used

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the Enable pin (EN). When Bit 0 is set to 1 (turn off the output immediately), the TOFF_FALL setting is ignored. Note that when Bits 3 and 2 are set to “1”, the device turns on only when the EN pin is high and the OPERATION command instructs the device to enable. With Bits 3 and 2 set to “1”, the device turns off when EN is set low or the OPERATION command instructs the device to disable.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 17h (EN pin control, active high, turn off output immediately – no ramp down)

Units: N/A

Command	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

Bits	Purpose	Bit Value	Meaning
7:5	Not Used	000	Not used
4	Sets the default for the on/off behavior of the device to be controlled by the EN pin and OPERATION command	0	Device is always on
		1	Device does not power up until commanded by the EN pin and OPERATION command (as programmed in Bits [3:0])
3	Controls how the device responds to commands received through the PMBus	0	Device ignores the on/off portion of the OPERATION command
		1	To start, the device requires that the on/off portion of the OPERATION command is instructing the device to enable the output. Depending on Bit 2, the device may also require the EN pin to be asserted for the device to start and enable the output
2	Controls how the device responds to the EN pin	0	Device ignores the EN pin (on/off controlled only by the OPERATION command)
		1	Device requires the EN pin to be asserted to start the unit. Depending on Bit 3, the OPERATION command may also be required to instruct the device to start before the output is energized.
1	Polarity of EN pin - active low not used	0	Not used
		1	Active high only
0	EN pin action when commanding the unit to turn off	0	Use the configured ramp-down settings (“soft-off”)
		1	Turn off the output immediately

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down; it only clears the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Protectable: No

Default Value: N/A

Units: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores all current PMBus values from the operating memory into the nonvolatile DEFAULT store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. Do not use this command during device operation; the device is unresponsive for 100ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus settings from the nonvolatile DEFAULT store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in USER store. Do not use this command during device operation; the device is unresponsive for 100ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: No

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. Do not use this command during device operation; the device is unresponsive for 100ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Do not use this command during device operation; the device is unresponsive for 100ms while restoring values.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: No

Default Value: N/A

Units: N/A

CAPABILITY (19h)

Definition: Reports some of the device's communications capabilities and limits.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: D0h (PEC supported, 1MHz bus speed, SMBALERT# supported, Linear format, AVSBus not supported)

Units: N/A

Command	CAPABILITY (19h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	1	0	1	0	0	0	0

Bits	Field Name	Value	Description
7	Packet Error Checking	0	Packet Error Checking not supported
		1	Packet Error Checking is supported
6:5	Maximum Bus Speed	00	Maximum supported bus speed is 100kHz
		01	Maximum supported bus speed is 400kHz
		10	Maximum supported bus speed is 1MHz
		11	Not used
4	SMBALERT#	0	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol
		1	The device has a SMBALERT# pin and supports the SMBus Alert Response protocol
3	Numeric Format	0	Numeric data is in LINEAR or DIRECT format
		1	Numeric data is in IEEE half precision floating point format
2	AVSBus Support	0	AVSBus is not supported
		1	AVSBus is supported
1:0	Not Used	00	Not Used

Note: If Bit 7 is zero, then the rest of the bits are reported as "0".

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Protectable: Yes (read only)

Default Value: 13h (Linear Mode, Exponent = -13)

Units: N/A

Command	VOUT_MODE (20h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1

Mode	Bits 7:5	Bits 4:0 (Parameter)
Linear	000	5-bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set higher than VOUT_MAX. If a value is written to this command below or above the range given below, the device sets the value to the lower or upper limit, respectively, and a warning is recorded in STATUS_VOUT.

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: VSET/SA pin-strap setting

Units: V

Equation: $VOUT = VOUT\_COMMAND \times 2^{-13}$

Range: 0.1V to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27034

Target voltage equals $27034 \times 2^{-13} = 3.3V$

Command	VOUT_COMMAND (21h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET/SA Pin-Strap setting															

VOUT_TRIM (22h)

Definition: Applies a fixed trim voltage to the output voltage command value. This command is typically used by the manufacturer of a power supply subassembly to calibrate a device in the subassembly circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h (0V)

Units: V

Equation: V_{OUT} trim = VOUT_TRIM $\times 2^{-13}$

Range: ±0.15V

Command	VOUT_TRIM (22h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa and used in conjunction with the exponent of -13h. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h (0V)

Units: V

Equation: V_{OUT} calibration offset = VOUT_CAL_OFFSET $\times 2^{-13}$

Range: ±0.15V

Command	VOUT_CAL_OFFSET (23h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. A VOUT_COMMAND greater than the existing VOUT_MAX will not be set and VOUT_COMMAND remains the same. If a VOUT_MAX sent is less than the current VOUT_COMMAND, output voltage is limited to VOUT_MAX. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VSET/SA pin-strap setting

Units: V

Equation: V_{OUT} max = VOUT_MAX × 2^{-13}

Range: 0.1V to 5.5V

Command	VOUT_MAX (24h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VSET/SA Pin-Strap setting															

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.05 x VSET/SA pin-strap setting

Units: V

Equation: VOUT margin high = VOUT_MARGIN_HIGH x 2^{-13}

Range: 0.1V to VOUT_MAX

Command	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET/SA Pin-Strap setting															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned.

Type: R/W

Protectable: Yes

Default Value: 0.95 x VSET/SA pin-strap setting

Units: V

Equation: VOUT margin low = VOUT_MARGIN_LOW

Range: 0.1V to VOUT_MAX

Command	VOUT_MARGIN_LOW (26h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET/SA Pin-Strap setting															

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change for any reason beside enable/disable, such as a change to VOUT_COMMAND or a margin change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible. This commanded rate does not apply when the device is commanded to turn on or to turn off.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0V/ms)

Units: V/ms

Equation: VOUT_TRANSITION_RATE = $Y \times 2^N$

Range: 0.1 to 4V/ms

Command	VOUT_TRANSITION_RATE (27h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

MAX_DUTY (32h)

Definition: Sets the maximum allowable duty cycle of the PWM output. NOTE: Do not use MAX_DUTY to set the output voltage of the device. VOUT_COMMAND is the proper method to set the output voltage.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EAD0h (90%)

Units: Percent (%)

Equation: MAX_DUTY = $Y \times 2^N$

Range: 0 to 90%

Command	MAX_DUTY (32h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	0	1	1	0	1	0	0	0	0

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. The initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is used, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation f_{SW} = 30MHz/n, where $30 \leq n \leq 150$. The actual switching frequency is the nearest available frequency to the FREQUENCY_SWITCH value.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC pin-strap setting

Units: kHz

Equation: FREQUENCY_SWITCH = $Y \times 2^N$

Range: 200kHz to 1000kHz

Command	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	SYNC Pin-strapped Value															

POWER_MODE (34h)

Definition: Enables and disables Diode Emulation Mode (DEM).

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: N/A

Command	POWER_MODE (34h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Purpose	Value	Description
7:1	Not Used	0	Not used
0	Maximum Efficiency	1	DEM enabled
		0	DEM disabled

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. INTERLEAVE sets the phase offset between individual devices, current sharing groups, and/or combinations of devices and current sharing groups. The phase offset is set automatically by default for devices within a single current sharing group.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: N/A

Command	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**

Bits	Purpose	Value	Description
15:12	Not Used	0	Not used
11:8	groupID	0	Group ID (used for current sharing group number)

Bits	Purpose	Value	Description
7:4	groupNo	0	Number in group
3:0	Order	0 to 15d	Device phase order in group

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA66h (4.8mΩ)

Units: mΩ

Range: >0mΩ to 1000mΩ

Equation: IOUT_CAL_GAIN = $Y \times 2^N$

Command	IOUT_CAL_GAIN (38h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	0	1	1	0	0	1	1	0

IOUT_CAL_OFFSET (39h)

Definition: Nulls out any offsets in the output current sensing circuit and compensates for delayed measurements of current ramp due to the current sense blanking time (see "ISENSE_CONFIG (D0h)" on page 89).

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0A)

Units: A

Range: -10A to 10A

Equation: IOUT_CAL_OFFSET = $Y \times 2^N$

Command	IOUT_CAL_OFFSET (39h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage falls below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_FAULT_LIMIT being exceeded, the device sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_FAULT bit in STATUS_VOUT, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned.

Type: R/W

Protectable: Yes

Default Value: 1.10 x VSET/SA pin-strap setting.

Units: V

Equation: V_{OUT} OV fault limit = VOUT_OV_FAULT_LIMIT $\times 2^{-13}$

Range: 0V to 6.0V

Command	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.10 x VSET/SA Pin-Strap Setting															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response between latch off or retry continuously. The delay time is the time between fault detected to restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time = 35ms increments

Command	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted
		001-111	Attempts to restart continuously until it is commanded OFF (by the EN pin, the OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output voltage falls below the VOUT_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

VOUT_OV_WARN_LIMIT (42h)

Definition: Sets the V_{OUT} overvoltage warning threshold. VOUT_OV_WARN_LIMIT must be set below the VOUT_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VOUT_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the output voltage falls below the VOUT_OV_WARN_LIMIT. In response to the VOUT_OV_WARN_LIMIT being exceeded, the device sets the VOUT bit in STATUS_WORD, sets the VOUT_OV_WARNING bit in STATUS_VOUT, and notifies the host. In the case of a fast VOUT overvoltage transition, a VOUT_OV_WARN_LIMIT fault may not be recorded.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.08 x VSET/SA pin-strap setting

Units: V

Equation: V_{OUT} OV fault limit = VOUT_OV_FAULT_LIMIT $\times 2^{-13}$

Range: 0V to 5.5V

Command	VOUT_OV_WARN_LIMIT (42h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.08 x VSET/SA Pin-Strap Setting															

VOUT_UV_WARN_LIMIT (43h)

Definition: Sets the V_{OUT} undervoltage warn threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_WARN_LIMIT must be set to a value below POWER_GOOD_ON and above VOUT_UV_FAULT_LIMIT. In response to the VOUT_UV_WARN_LIMIT being exceeded, the devices sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_WARNING bit in STATUS_VOUT, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.9 x VSET/SA pin-strap setting

Units: V

Equation: V_{OUT} UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}

Range: 0V to 5.5V

Command	VOUT_UV_WARN_LIMIT (43h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET/SA Pin-Strap Setting															

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT must be set to a value below VOUT_UV_WARN_LIMIT and POWER_GOOD_ON. In response to the VOUT_UV_FAULT_LIMIT being exceeded, the device: Sets the VOUT bit in STATUS_WORD, sets the VOUT_UV_FAULT bit in STATUS_VOUT and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.85 x VSET/SA pin-strap setting

Units: V

Equation: V_{OUT} UV fault limit = VOUT_UV_FAULT_LIMIT × 2^{-13}

Range: 0V to 5.5V

Command	VOUT_UV_FAULT_LIMIT (44h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.85 x VSET/SA Pin-Strap Setting															

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response. Note that V_{OUT} UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances this causes the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The delay time is the time between fault detected to restart attempts. TON_DELAY is still observed during a retry attempt after the retry delay has expired.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response Behavior: the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0].
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. See "ISENSE_CONFIG (D0h)" on page 89. A fault occurs after this limit is exceeded for the number of consecutive cycles as defined in ISENSE_CONFIG. This feature shares the OC fault bit operation (in STATUS_IOUT) and MFR_IOUT_OC_FAULT_RESPONSE with IOUT_AVG_OC_FAULT_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: 0A to 100A

Command	IOUT_OC_FAULT_LIMIT (46h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	CFG0 Pin-Strap setting															

IOUT_OC_WARN_LIMIT (4Ah)

Definition: Sets the I_{OUT} peak overcurrent warn threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. See "ISENSE_CONFIG (D0h)" on page 89. A warning occurs after this limit is exceeded for the number of consecutive cycles as defined in ISENSE_CONFIG. When a warning occurs, the corresponding bit is set in STATUS_IOUT. Values outside of the range are not accepted. This limit must be set below IOUT_OC_FAULT_LIMIT for fault responses with restart attempts to function properly.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0.7 x IOUT_OC_FAULT_LIMIT pin-strap setting

Units: A

Equation: IOUT_OC_WARN_LIMIT = $Y \times 2^N$

Range: 0A to 100A

Command	IOUT_OC_WARN_LIMIT (4Ah)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0.7 x IOUT_OC_FAULT_LIMIT Pin-Strap setting															

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. See "ISENSE_CONFIG (D0h)" on page 89. A fault occurs after this limit is exceeded for the number of consecutive cycles as defined in ISENSE_CONFIG. This feature shares the UC fault bit operation (in STATUS_IOUT) and IOUT_UC_FAULT_RESPONSE with IOUT_AVG_UC_FAULT_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -1.0 x IOUT_OC_FAULT_LIMIT pin strap setting

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 0A

Command	IOUT_UC_FAULT_LIMIT (4Bh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-1.0 x IOUT_OC_FAULT_LIMIT Pin-Strap setting															

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature falls below the OT_WARN_LIMIT. In response to the OT_FAULT_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_FAULT bit in STATUS_TEMPERATURE, and notifies the host. NOTE: Voltages above 2.5V on the TMON pin cause the device to automatically shut down and latch off, regardless of the OT_FAULT_LIMIT setting or if TMON is being used for over-temperature faults. This fault is recorded in Bit 1 of STATUS_MFR_SPECIFIC.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EBE8h (+125°C)

Units: °C

Equation: OT_FAULT_LIMIT = $Y \times 2^N$

Range: 0°C to 175°C

Command	OT_FAULT_LIMIT (4Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin, OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature falls below the OT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. OT_WARN_LIMIT must be set below the OT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the OT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature falls below the OT_WARN_LIMIT. In response to the OT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110°C)

Units: °C

Equation: OT_WARN_LIMIT = $Y \times 2^N$

Range: 0°C to 175°C

Command	OT_WARN_LIMIT (51h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature rises above the UT_WARN_LIMIT. In response to the temperature falling below UT_WARN_LIMIT, the device sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30°C)

Units: °C

Equation: UT_WARN_LIMIT = $Y \times 2^N$

Range: -55°C to +25°C

Command	UT_WARN_LIMIT (52h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, at which the device should indicate an under-temperature fault. UT_WARN_LIMIT must be set above the UT_FAULT_LIMIT in order for fault responses with restart attempts to function properly. When the UT_FAULT_RESPONSE is set to retry, a retry is not attempted until the temperature rises above the UT_WARN_LIMIT.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: E530h (-45°C)

Units: °C

Equation: UT_FAULT_LIMIT = $Y \times 2^N$

Range: -55°C to +25°C

Command	UT_FAULT_LIMIT (53h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the table below. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 pin-strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior. The device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin, OPERATION command, or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature rises above UT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage falls below the VIN_OV_WARN_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DA00h (16V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 18V

Command	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the table below.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: N/A

Command	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior. The device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and Retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the input voltage falls below the VIN_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold as defined by the table below. VIN_OV_WARN_LIMIT must be set below the VIN_OV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_OV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage falls below the VIN_OV_WARN_LIMIT. In response to the OV_WARN_LIMIT being exceeded, the device sets the INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D3E0h (15.5V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 18V

Command	VIN_OV_WARN_LIMIT (57h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	1	1	1	0	0	0	0	0

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage rises above the VIN_UV_WARN_LIMIT. In response to the input voltage falling below VIN_UV_WARN_LIMIT, the device sets the INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB80h (7.0V)

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0V to 16V

Command	VIN_UV_WARN_LIMIT (58h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	1	0	0	0	0	0	0	0

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold. VIN_UV_WARN_LIMIT must be set above the VIN_UV_FAULT_LIMIT for fault responses with restart attempts to function properly. When the VIN_UV_FAULT_RESPONSE is set to retry, a retry is not attempted until the input voltage rises above the VIN_UV_WARN_LIMIT. In response to the input voltage falling below VIN_UV_FAULT_LIMIT, the device sets the INPUT bits in STATUS_WORD, sets the VIN_UV_FAULT bit in STATUS_INPUT, and notifies the host. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CB40h (6.5V)

Units: V

Equation: VIN_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0V to 16V

Command	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	1	0	1	0	0	0	0	0	0

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the table below. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior. The device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01,11	Not used
		10	Disable and retry according to the setting in Bits [5:3]
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared
		001-111	Attempts to restart continuously, until it is commanded OFF (by the EN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the input voltage rises above the VIN_UV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_WARN_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_WARN_LIMIT. Power-Good may not assert if the device is enabled for less than 2ms.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.90 x VSET/SA pin-strap setting

Units: V

Range: 0V to 5.5V

Command	POWER_GOOD_ON (5Eh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET/SA Pin-Strap setting															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0ms)

Units: milliseconds (ms)

Equation: TON_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Command	TON_DELAY (60h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TON_RISE (61h)

Definition: Sets the rise time of VOUT after the TON_DELAY time has elapsed. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: milliseconds (ms)

Equation: TON_RISE = $Y \times 2^N$

Range: 0ms to 125ms. Although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

Command	TON_RISE (61h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} ramps down. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0ms)

Units: milliseconds (ms)

Equation: TON_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Command	TOFF_DELAY (64h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after the TOFF_DELAY has expired. Setting the TOFF_FALL to values less than 0.5ms causes the device to turn off both the high and low-side FETs immediately after the expiration of the TOFF_DELAY time. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: milliseconds (ms)

Equation: TOFF_FALL = $Y \times 2^N$

Range: 0ms to 125ms. Values less than 0.5ms cause the device to turn off both the high and low-side FETs immediately after the expiration of the TOFF_DELAY time.

Command	TOFF_FALL (65h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

STATUS_BYTE (78h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD (79h) is the same register as the STATUS_BYTE command.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled
5	VOUT_OV_FAULT	An output overvoltage fault occurred
4	IOUT_OC_FAULT	An output overcurrent fault occurred
3	VIN_UV_FAULT	An input undervoltage fault occurred
2	TEMPERATURE	A temperature fault or warning occurred
1	CML	A communications, memory, or logic fault occurred
0	Not used	Not used

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 0000h (no faults)

Units: N/A

Command	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
15	VOUT	An output voltage fault or warning occurred
14	IOUT	An output current fault occurred
13	INPUT	An input voltage fault or warning occurred
12	MFR_SPECIFIC	A manufacturer specific fault or warning occurred
11	POWER_GOOD #	The POWER_GOOD signal, if present, is negated (Note 1)
10	NOT USED	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set
8	Not Used	Not used
7	Not Used	Not used
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled
5	VOUT_OV_FAULT	An output overvoltage fault occurred
4	IOUT_OC_FAULT	An output overcurrent fault occurred
3	VIN_UV_FAULT	An input undervoltage fault occurred
2	TEMPERATURE	A temperature fault or warning occurred
1	CML	A communications, memory, or logic fault occurred
0	Not used	Not used

Note:

1. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good. POWER_GOOD may not assert if the device is enabled for less than 2ms.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage. **Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.**

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault
6	VOUT_OV_WARNING	Indicates an output overvoltage warning. Cannot be set when an overvoltage fault occurs
5	VOUT_UV_WARNING	Indicates an output undervoltage warning. Cannot be set when an undervoltage fault occurs
4	VOUT_UV_FAULT	Indicates an output undervoltage fault
3	VOUT_MAX_WARNING	Attempted to set VOUT_COMMAND greater than VOUT_MAX or below 0.1V
2:0	Not used	Not used

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current. **Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.**

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault occurred
6	Not Used	Not used
5	IOUT_OC_WARNING	An output overcurrent warning occurred. Cannot be set when an output overcurrent fault occurs
4	IOUT_UC_FAULT	An output undercurrent fault occurred.
3:0	Not Used	Not used

STATUS_INPUT (7Ch)

Definition: Returns one byte of information with a summary of input voltage related faults or warnings. **Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.**

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault occurred
6	VIN_OV_WARNING	An input overvoltage warning occurred. Cannot be set when an overvoltage fault occurs
5	VIN_UV_WARNING	An input undervoltage warning occurred. Cannot be set when an undervoltage fault occurs
4	VIN_UV_FAULT	An input undervoltage fault occurred
3:0	Not Used	Not used

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings. **Note that warning bits may not be set when the corresponding fault bits are set. This can occur with rapidly changing fault waveforms.**

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_TEMP (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault occurred
6	OT_WARNING	An over-temperature warning occurred. Cannot be set when an over-temperature fault occurs
5	UT_WARNING	An under-temperature warning occurred. Cannot be set when an under-temperature fault occurs
4	UT_FAULT	An under-temperature fault occurred
3:0	Not Used	Not used

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors. Status bits can only be cleared with the CLEAR_FAULTS command or by disabling, then re-enabling the device.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bit Number	Meaning
7	Invalid or unsupported PMBus command was received
6	The PMBus command was sent with invalid or unsupported data
5	A Packet Error Check (PEC) failed on a PMBus command
4:2	Not used
1	A PMBus command tried to write to a read only or protected command, or too few or too many bytes were received for a given command
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of miscellaneous system faults.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 00h (no faults)

Units: N/A

Command	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Field Name	Meaning
7	Not Used	Not used
6	Phase Fault	A phase in the current sharing group has failed, when configured as part of a current sharing rail
5	Not Used	Not used
4	DDC fault	An error was detected on the DDC bus
3	External Switching Period Fault	Loss of external clock synchronization has occurred
2	Fault Group	A fault was spread using DDC fault group
1	SPS fault	The SPS device set the TMON voltage above 2.5V to indicate a general SPS fault
0	Fault Bus	Device was shutdown by the enable pin when using the enable pin as a fault bus

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: V

Equation: READ_VIN = $Y \times 2^N$

Range: N/A

Command	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IIN (89h)

Definition: Returns the input current reading. This is a calculated value based on the output current, duty cycle, and IIN_CAL_OFFSET. It is not accurate when the device is in Diode Emulation Mode (DEM).

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: A

Equation: READ_IIN = $Y \times 2^N$

Range: N/A

Command	READ_IIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: V

Equation: READ_VOUT = READ_VOUT $\times 2^{-13}$

Range: N/A

Command	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IOUT (8Ch)

Definition: Returns the output current reading. No reading is returned if the PWM output is not active; that is, the output is not being regulated. It is not accurate when the device is in Diode Emulation Mode (DEM).

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: A

Equation: READ_IOUT = Y $\times 2^{N}$

Range: N/A

Command	READ_IOUT (8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading internal to the device.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_1 = $Y \times 2^N$

Range: N/A

Command	READ_TEMPERATURE_1 (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_2 (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to TEMP/TRK if the device is configured to do so in USER_CONFIG.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_2 = $Y \times 2^N$

Range: N/A

Command	READ_TEMPERATURE_2 (8Eh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the TMON pin. The voltage is read on this pin and converted to a temperature by the following equation: T°C = (Vtmon - 0.6V)/0.008. NOTE: Voltages above 2.5V on the TMON pin cause the device to automatically shut down and latch off, regardless of the OT_FAULT_LIMIT setting when using TMON for over-temperature faults.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_3 = $Y \times 2^N$

Range: N/A

Command	READ_TEMPERATURE_3 (8Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter while the device is enabled.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: Percent (%)

Equation: READ_DUTY_CYCLE = $Y \times 2^N$

Range: N/A

Command	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_FREQUENCY (95h)

Definition: Reports the actual configured switching frequency of the device.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: kiloHertz (kHz)

Equation: READ_FREQUENCY = $Y \times 2^N$

Range: N/A

Command	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_POUT (96h)

Definition: Returns the calculated output power in W.

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: W

Equation: READ_POUT = $Y \times 2^N$

Range: N/A

Command	READ_POUT (96h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_PIN (97h)

Definition: Returns the calculated input power in W. It is not accurate when the device is in Diode Emulation Mode (DEM).

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read only

Protectable: Yes (read only)

Default Value: N/A

Units: W

Equation: READ_PIN = $Y \times 2^N$

Range: N/A

Command	READ_PIN(97h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read only

Protectable: Yes (read only)

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

Units: N/A

Command	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	1	0	0	1	1

Bits 7:4	Part 1 Revision	Bits 3:0	Part 2 Revision
0011	1.3	0011	1.3

MFR_ID (99h)

Definition: Sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Data Length in Bytes: 4

Data Format: CUS

Type: Read only: Block read

Protectable: Yes (Read only)

Default Value: 49A02F00h (ISL68301)

Units: N/A

Command	IC_DEVICE_ID (ADh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	Reserved	ID Low Byte	ID High Byte	MFR code
Default Value	00h	2Fh	A0h	49h

IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Data Length in Bytes: 4

Data Format: CUS

Type: Read only: Block read

Protectable: Yes (read only)

Default Value: 0900080Dh

Units: N/A

Command	IC_DEVICE_REV (AEh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	Firmware Minor	Firmware Major	Interface Minor	Interface Major
Default Value	01h	08h	00h	09h

USER_DATA_00 (B0h)

Definition: Sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

USER_DATA_01 (B1h)

Definition: Sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

USER_DATA_02 (B2h)

Definition: Sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL USER_DATA_00, USER_DATA_01, and USER_DATA_02 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W word

Protectable: Yes

Default Value: 1903h (96ns blanking, fault count of 3, downslope, SPS range)

Units: N/A

Range: N/A

Command	ISENSE_CONFIG (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1

Bits	Field Name	Value	Setting	Description
15:11	Current Sense Blanking Time	00000	0	Sets the blanking time current sense blanking time in increments of 32ns
		00001	32	
		00010	64	
		00011	96	
		00100	128	
		00101	160	
		00110	192	
		00111	224	
		01000	256	
		01001	288	
		01010	320	
		01011	352	
		01100	384	
		01101	416	
		01110	448	
		01111	480	
		10000	512	
		10001	544	
		10010	576	
		10011	608	
		10100	640	
		10101	672	
		10110	704	
		10111	736	
		11000	768	
		11001	800	
		11010	832	
10:8	Current Sense Fault Count	000	1	Sets the number of consecutive overcurrent (OC) or undercurrent (UC) events required for a fault. An event can occur once during each switching cycle. For example, if 5 is selected, an OC or UC event must occur for five consecutive switching cycles, resulting in a delay of at least five switching periods
		001	3	
		010	5	
		011	7	
		100	9	
		101	11	
		110	13	
		111	15	
7:3	Not Used	0000	Not used	Not used
2	Current Sense Control	0	(Down Slope)	Selection of current sensing method
		1	(Up Slope)	

Bits	Field Name	Value	Setting	Description
1:0	Current Sense Range	00	Low Range	Low range ±15mV, medium range ±30mV, high range ±60mV; SPS range ±400mV
		01	Medium Range	
		10	High Range	
		11	SPS Range	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command should be saved immediately to the desired user or default store after being written. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 1400h/1402h Sync set by CFG1 pinstrap. (Min Duty 1.17%, Boot Cap refresh, XTEMP disabled, fault bus disabled, PG open drain, Internal Temp Fault, TMON enabled, SYNC uses internal/external clock)

Units: N/A

Command	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	1	0	1	0	0	0	0	0	0	0	0	CFG1	

Bits	Field Name	Value	Setting	Description
15:11	Minimum Duty Cycle	00000	0-31d	Sets the Minimum Duty Cycle in percent (%). The percentage value is defined by the following expression: Minimum Duty Cycle = 2 x (Setting+1) / 512. This feature must be enabled by setting Bit 10 to 1 (enabled)
10	Minimum Duty Cycle Enable	0	Disable	Minimum duty cycle disabled
		1	Enable	Minimum duty cycle enabled
9	DEM Boot Cap Refresh	0	Disable	Low-side gate minimum pulse-width disabled
		1	Enable	Low-side gate minimum pulse-width enabled during diode emulation mode. This ensures that the top FET bootstrap capacitor is re-charged every switch cycle
8	Not Used	0	Not Used	Not used
7	Enable Fault Bus	0	Disable	Disable fault bus
		1	Enable	Enable fault bus
6	XTEMP/Tracking Select	0	Disable	Disable external temperature sensor. Enables TRK (tracking) input to TEMP/TRK pin
		1	Enable	Enable external temperature sensor. Disables TRK input
5	Power-Good Pin Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-Pull	1 = PG is push-pull output

Bits	Field Name	Value	Setting	Description
4:3	TEMP Fault Select	00	Internal temperature sensor selected	Selects internal temperature sensor to determine temperature faults
		01	External temperature sensor selected	Selects external temperature sensor to determine temperature faults. Bit 2 above must be set to 1 (enable XTEMP)
		10	TMON SPS temperature input selected	Selects the TMON Smart Power Stage temperature sensor input to determine temperature faults. Bit 2 must be set to 1 (enable TMON). NOTE: Voltages above 2.5V on the TMON pin cause the device to automatically shut-down and latch off, regardless of the OT_FAULT_LIMIT setting when using TMON for overtemperature faults
		11	Not used	Not used
2	TMON enable	0	Disable	Disable TMON input
		1	Enable	Enable TMON input
1:0	Sync Pin Configuration	00	Internal Clock	Use internal clock (frequency initially set with pin-strap)
		01	Use and Output Internal Clock	Use internal clock and output internal clock (not for use with pin-strap)
		10	External Clock	Use external clock
		11	Not used	Not used

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing for up to eight phases. To operate as a 2-phase controller, set both phases (devices) to the same rail ID, set phases in rail to 2, then set each phase ID **sequentially** as 0 and 1. The devices automatically equally offset the phases in the rail. For example, in a 2-phase rail the phases are offset by 180º. When a device is configured to be part of a current sharing rail, DDC_GROUP must be configured so that all phases in the current sharing rail have the same DDC_GROUP ID and are set to respond to DDC_GROUP OPERATION and VOUT COMMAND messages. See the DDC_GROUP command for more details.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: PMBus address pin-strap dependent.

Units: N/A

Command	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (shared output)
7:3	Not Used	00	00	Not used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 125ms. POWER_GOOD may not assert if the device is enabled for less than 2ms. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h, 1ms

Units: milliseconds (ms)

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0ms to 125ms

Command	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

ASCR_ADVANCED (D5h)

Definition: Allows user configuration of advanced ASCR settings which have an impact on PWM jitter. ASCR Threshold sets the level that determines when the output voltage is considered to be at a steady state level. ASCR Threshold gain sets the ASCR gain reduction amount when the output voltage is considered to be in the steady state condition.

Data Length in Bytes: 2

Data Format: Bit Field and non-signed binary

Type: Block R/W

Protectable: Yes

Default Value: 2064h (Divide by 4, 64h threshold setting)

Units: N/A

Command	ASCR_ADVANCED (D5h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not used						Thresh. Gain		ASCR Threshold							
Default Value	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0

Bits	Purpose	Value	Description
15:14	Not used	00	Not used
13:12	ASCR Threshold Gain Select Setting	00	Divide by 1
		01	Divide by 2
		10	Divide by 4
		11	Divide by 8
11:0	ASCR Threshold Setting	0-FFFh	ASCR Threshold

INDUCTOR (D6h)

Definition: Informs the device of the circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: AA66h (0.3µH)

Units: µH

Equation: INDUCTOR = $Y \times 2^N$

Range: >0µH to 100µH

Command	INDUCTOR (D6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0

SNAPSHOT_FAULT_MASK (D7h)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Protectable: Yes

Default Value: 0000h (no faults masked)

Units: N/A

Range: N/A

Command	SNAPSHOT_FAULT_MASK (D7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Status Bit Name	Meaning
15	Fault Phase	Ignore phase faults in a current sharing rail
14	Fault Group	Ignore rail faults in a fault spreading group
13	Fault CPU	Ignore CPU faults
12	Fault UT	Ignore under-temperature faults
11	Fault OT	Ignore over-temperature faults
10	Fault peak OC	Ignore peak output overcurrent faults
9	Fault peak UC	Ignore peak output undercurrent faults
8	Fault EN pin as fault bus	Ignore Enable pin faults when the Enable pin is used as a fault bus
7	Fault VIN_OV	Ignore input overvoltage faults
6	Fault VOUT_OV	Ignore output overvoltage faults
5	Fault VOUT_UV	Ignore output undervoltage faults
4	Fault SPS	Ignore Smart Power Stage (SPS) faults
3	Fault Sync	Ignore loss of synchronization faults
2	Fault VIN_UV	Ignore input undervoltage faults
1	Fault IOUT_OC	Ignore output average overcurrent faults
0	Fault IOUT_UC	Ignore output average undercurrent faults

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection parameters.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

Command	OVUV_CONFIG (D8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	1	0

Bits	Purpose	Value	Description
7:4	Not used	0	Not used
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response

XTEMP_SCALE (D9h)

Definition: Sets a scalar value that is used for calibrating the external temperature.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0)

Units: 1/°C

Equation: $READ\_TEMPERATURE\_2 = ExternalTemperature\left(\frac{1}{XTEMP\_SCALE}\right) + XTEMP\_OFFSET$

Range: 0.1 to 10

Command	XTEMP_SCALE (D9h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

XTEMP_OFFSET (DAh)

Definition: Sets an offset value that calibrates the external temperature.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0 °C)

Units: °C

Equation: $READ\_TEMPERATURE\_2 = ExternalTemperature\left(\frac{1}{XTEMP\_SCALE}\right) + XTEMP\_OFFSET$

Range: -100°C to +100°C

Command	XTEMP_OFFSET (DAh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MFR_SMBALERT_MASK (DBh)

Definition: Prevents faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.

Data Length in Bytes: 7

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00 00 00 00 00 00 00h (No faults masked)

Units: N/A

Command	MFR_SMBALT_MASK (DBh)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

Byte	Status Byte Name	Meaning
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte
5	STATUS_OTHER	Not used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte
3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values range from 0 to 127, representing 0 to 12700 parts per million (ppm) temperature coeffient of resistance. In other words, for Temperature Coefficient (TC) enter values in hundreds of ppm. TEMPCO_CONFIG should be set to 3900ppm (39d, 27h) when using inductor DCR current sensing to compensate for the variation in inductor resistance due to the temperature coefficient of copper.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Units: ppm/°C

Default Value: 00h (0ppm/°C, SPS current sensing)

Equation: In order to apply the proper temperature compensation to the current sensing element, enter the temperature coefficient in hundreds of parts per million (ppm) in Bits 6:0 as shown below. The ISL68301 automatically compensates the value of IOUT_CAL_GAIN so that current sense readings remain accurate throughout the circuit's operating temperature range. The value entered for IOUT_CAL_GAIN represents the resistance of the current sensing element at +25ºC, and is the value of DC resistance in the output inductor in DCR current sensing applications. The ideal value for Temperature compensation for copper wire is 3900ppm/ºC (27h); however, each application should be characterized to determine the actual temperature compensation value for each application. When using Smart Power Stages, such as the ISL99226/7, the Temperature Coefficient should be set to 0, because SPS devices automatically compensate for temperature effects.

Bit 7 selects either the IC internal temperature or external temperature for temperature compensation. An external temperature reading, with the temperature sensing 2N3904 junction as close as possible to the output inductor as possible.

The ISL68301 uses the Temperature Coefficient to adjust the value used for IOUT_CAL_GAIN when calculating output current using the following equation:

IOUT_CAL_GAIN(compensated) = IOUT_CAL_GAIN(25ºC) * (1 + (Temperature Coefficient/10^6) * (Measured Temperature - 25)

Range: 0 to 12700ppm/ºC

Command	TEMPCO_CONFIG (DCh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Purpose	Value	Description
7	Selects the temp sensor source for tempco correction	0	Selects the internal temperature sensor
		1	Selects the TEMP/TRK pin for temperature measurements (2N3904 Junction) Note that TEMP must be enabled in USER_CONFIG, Bit 1.
6:0	Sets the tempco correction in units of 100ppm/°C for IOUT_CAL_GAIN	TC	RSEN (DCR) = IOUT_CAL_GAIN x (1+TC x (T-25)) Where RSEN = resistance of sense element

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR Gain is analogous to bandwidth, ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR Gain settings range from 100 to 1000, and typical ASCR Residual settings range from 10 to 90.

Data Length in Bytes: 4

Data Format: Bit Field and non-signed binary

Type: Block R/W

Protectable: Yes

Default Value: CFG1 pin-strap setting (Integral Gain = 100), ASCR Gain = CFG1 setting, Residual = 90)

Units: N/A

Command	ASCR_CONFIG (DFh)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Integral Gain								ASCR Residual							
Default Value	0	1	1	0	0	1	0	0	0	1	0	0	1	1	1	1
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	ASCR Gain															
Default Value	CFG1 Pin-Strap setting															

Bits	Purpose	Value	Description
31:24	Integral gain	0-7Fh	Error signal gain
23:16	ASCR residual	0-7Fh	ASCR residual
15:0	ASCR gain	0-FFh	ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device enables its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus as a result of the prequel's Power-Good (PG) signal going high. The device disables its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V).

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode.

Fault spreading is not automatic in devices that have a prequel or sequel. When a device shuts down due to a fault, it does not disable its output and does not send a message to its sequel or prequel to disable. If fault spreading behavior is desired, use the DDC_GROUP or LEGACY_FAULT_GROUP commands. **Automatic fault retry behavior is not supported for fault spreading or sequencing groups.**

A device that is tracking another device (is tracking the signal on its VTRK pin, see TRACK_CONFIG), cannot be a sequel or prequel in a sequencing group.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (prequel and sequel disabled)

Units: N/A

Command	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device. When tracking, the TOFF_DELAY in the tracking device must be greater than TOFF_DELAY + TOFF_FALL in the device being tracked. When configured to track, the VOUT_COMMAND must be set to the desired steady state output voltage. Devices that are providing the VTRK signal and the tracking device must have their EN pins tied together. If PMBus enabling is used using the OPERATION command, DDC_GROUP must be configured on both devices with the same BROADCAST_OPERATION group ID (Bits 12:8) and have BROADCAST_OPERATION response enabled (Bit 13 set to 1).

Pre-biased tracking: The device tracking the voltage applied to the VTRK pin (called the “tracker”) slews to whatever voltage is present at the VTRK pin when the tracker is enabled. Depending on how much pre-bias voltage is present on the VTRK pin, the output voltage may overshoot, or an overcurrent fault may occur as the device attempts to rapidly track to this voltage. For this reason, it is recommended that prebias voltage on the VTRK pin be no more than 20% of the tracker’s desired steady state output voltage.

Sequencing: A tracking device cannot be part of a sequencing group and it cannot be a prequel or sequel.

Margining: VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW do not apply to devices that are tracking.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (tracking disabled)

Units: N/A

Command	TRACK_CONFIG (E1h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
7	Voltage Tracking Control	0	Disable	Tracking is disabled
		1	Enable	Tracking is enabled
6:3	Not Used	000	Not Used	Not used
2	Tracking Ratio Control	0	100%	Output tracks at 100% ratio of VTRK input
		1	50%	Output tracks at 50% ratio of VTRK input
1	Target Limit	0	Target Voltage	Output voltage is limited by target voltage
		1	VTRK Voltage	Output voltage is limited by VTRK voltage
0	Not Used	0	Not Used	Not used

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned Group numbers to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Rail IDs (see "DDC_CONFIG (D3h)" on page 92). Current sharing rails must be in the same DDC Group to respond to broadcast VOUT_COMMAND and OPERATION commands.

Devices in a current sharing rail are not required to have the same POWER_FAIL group ID. Faults are automatically spread when a device is configured to be part of a current sharing rail. If you want a current sharing rail to spread faults with another rail, then all the devices in that current sharing rail should have the same POWER_FAIL group ID as the rail it is expected to share POWER_FAIL faults with. **Automatic fault retry behavior is not supported for fault spreading or sequencing groups.**

When a device is set to ignore DDC GROUP messages, the device still transmits DDC messages with its own DDC ID. Note that the default DDC_GROUP ID is set to 0d, which is a valid DDC_GROUP number, so even a device with the default setting (ignore all DDC groups, all DDC group IDs set to 0d) still transmits DDC GROUP messages, despite ignoring DDC_GROUP messages from other devices on the DDC bus.

DDC Rail IDs should not use the same ID as DDC_GROUPS. In other words, if a device is using a DDC Rail ID of 0x02, no devices should be using GROUP_ID 0x02.

Data Length in Bytes: 34

Data Format: Bit Field

Type: Block R/W

Protectable: Yes

Default Value: 001F1F1Fh (DDC groups not used)

Units: N/A

Command	DDC_GROUP (E2h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used										EN>	VOUT_COMMAND Group ID				
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		EN>	OPERATION Group ID					Not Used		EN>	Power Fail Group ID				
Default Value	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bits	Purpose	Value	Description
31:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events
15:14	Not Used	00	Not used

Bits	Purpose	Value	Description
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast OPERATION events
7:6	Not Used	00	Not used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID
		0	Ignores POWER_FAIL events with same Group ID
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

STORE_CONTROL (E3h)

Definition: Used to store command settings in the USER and DEFAULT Stores while the device is enabled. Used in conjunction with STORE_DATA.

Data Length in Bytes: 11

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: N/A

Units: N/A

Command	STORE_CONTROL (E3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bits	Field Name	Value	Description
7:4	Store to be read or written to	0001	User store
		0010	Default store
		0000, 0011-1111	Not used
3:0	Command	0000	Read store
		0001	Erase store
		0010	Start write
		0011	End write
		0100-1111	Not used

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string. The format is: Part Number, Release Type Letter, Major Revision, Minor Revision.

Data Length in Bytes: 16

Data Format: ASCII. ISO/IEC 8859-1

Type: Block Read

Protectable: Yes (read only)

Default Value: ISL68301, current release type letter, current major revision, current minor revision

Units: N/A

Command	DEVICE_ID (E4h)															
Format	Characters (Bytes)															
Characters	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Minor Revision		Major Revision		Rel. Type		Part Number									
Default Value	1	0	1	0	G	-	0	-	1	0	3	8	6	L	S	I
* Current revision at time of manufacture																

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are cleared by the CLEAR_FAULTS command only.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3
		11	Not used

Bits	Field Name	Value	Description
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared
		001-111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the table below. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The delay time is the time between fault detected and restart attempts.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: CFG0 pin-strap setting

Units: Retry time unit = 35ms

Command	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	CFG0 Pin-Strap setting							

Bits	Field Name	Value	Description
7:6	Response behavior. For all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are cleared by the CLEAR_FAULTS command only.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared
		001-111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in Bits [2:0]
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_OC_FAULT_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11.

Type: R/W

Protectable: Yes

Default Value: 0.8 x IOUT_OC_FAULT_LIMIT pin-strap setting

Units: A

Equation: IOUT_AVG_OC_FAULT_LIMIT = $Y \times 2^N$

Range: 0A to 100A

Command	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0.8 x IOUT_OC_FAULT_LIMIT Pin-Strap setting															

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT. Values outside of the range are not accepted.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -0.8 x IOUT_OC_FAULT_LIMIT pin-strap setting

Units: A

Equation: IOUT_AVG_UC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 0A

Command	IOUT_AVG_UC_FAULT_LIMIT (E8h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-0.8 * IOUT_OC_FAULT_LIMIT Pin-Strap setting															

ADVANCED_CONFIG (E9h)

Definition: Sets the PWM mid-drive voltage, SMBus I/O voltage and enables/disables the VG LDO.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W

Protectable: Yes

Default Value: 01h

Command	ADVANCED_CONFIG (E9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	Reserved					R/W	R/W	R/W
Function	See Following Table							
Default Value	N/A	N/A	N/A	N/A	N/A	0	0	1

Bits	Field Name	Value	Description
7:3	Reserved	N/A	Reserved
2	vgDisable	0	1 = disable, 0 = enable
1	pmbusVolt	0	0 sets V_{IN} = 2V, V_{IL} = 0.8V for 5V/3.3V logic compatible 1 sets V_{IN} = 1.17V, V_{IL} = 0.552V for 1.8V logic compatible
0	midDrvVolt	1	1 sets PWM mid-drive voltage to 1.5V 0 sets PWM mid-drive voltage to 2.5V

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: Yes (read only)

Default Value: N/A

Units: N/A

Byte	Value	PMBus Command	Format
31:30	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
29:28	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
27:26	External Temperature 2 (TMON)	READ_TEMPERATURE_3 (8Fh)	2 Byte Linear-11
25:24	External Temperature 1	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
23:22	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Highest Measured Output Current	N/A (Peak measured output current)	2 Byte Linear-11
13:12	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
11:10	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
9:8	Input Voltage	READ_VIN (88h)	2 Byte Linear-11
7:6	All Faults	N/A	2 Byte Bit Field
5	First Fault	N/A	1 Byte Bit Field
4:1	Uptime	N/A	4 Byte Integer
0	Flash Memory Status Byte	N/A	1 Byte Bit Field

First Fault		
Bit Number	**Status Bit Name**	**Meaning**
7:4	Not Used	Not Used
3	IOUT_PEAK_OC	Peak output overcurrent was the first fault
2	IOUT_AVG_OC	Average output overcurrent was the first fault
1	VOUT_OV	Output overvoltage was the first fault
0	VIN_UV	Input undervoltage was the first fault

All Faults		
Bit Number	**Status Bit Name**	**Meaning**
15	Fault Phase	A DDC rail fault occurred
14	Fault Group	A DDC group fault occurred
13	Fault CPU	A CPU fault occurred
12	Fault UT	An under-temperature fault occurred
11	Fault OT	An over-temperature fault occurred
10	Fault peak OC	A peak output overcurrent fault occurred
9	Fault peak UC	A peak output undercurrent fault occurred
8	Fault EN pin as fault bus	The EN pin was pulled low in response to a fault
7	Fault VIN_OV	An input overvoltage fault occurred
6	Fault VOUT_OV	An output overvoltage fault occurred
5	Fault VOUT_UV	An output undervoltage fault occurred

All Faults		
Bit Number	**Status Bit Name**	**Meaning**
4	Fault SPS	A MOSFET driver fault occurred
3	Fault Sync	A loss of clock synchronization fault occurred
2	Fault VIN_UV	An input undervoltage fault occurred
1	Fault IOUT_OC	An average output overcurrent fault occurred
0	Fault IOUT_UC	An average output undercurrent fault occurred

BLANK_PARAMS (EBh)

Definition: Returns a 32-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation. The 32-byte string, consisting of 256 bits, corresponds to the 256 possible PMBus commands: from 00h to FFh. Each bit references a PMBus command by command number, for example ON_OFF_CONFIG, command 02h corresponds to bit 2.If the setting of ON_OFF_CONFIG was changed and stored in the USER or DEFAULT stores, the last 2 bytes of BLANK_PARAMS would be 1111 1011.

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: Yes (read only)

Default Value: FF..FFh

Units: N/A

LEGACY_FAULT_GROUP (F0h)

Definition: Allows the ISL68301 to sequence and fault spread with devices other than the ISL683xx and ZL880x families of ICs. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit vector in which every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device responds upon receiving a fault spreading event. In this vector, Bit 0 of Byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of Byte 3 corresponds to the rail with DDC ID 31.

NOTE: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail (devices other than the ISL683xx and ZL880x family ICs) must shut down for the rail to report a shutdown. If fault spread mode is enabled in DDC_CONFIG, the device immediately shuts down if one of its DDC_GROUP members fail. The device/rail does not attempt its configured fault restart (retry).

If fault spread mode is disabled in DDC_CONFIG, the device immediately shuts down (not sequenced). The rails/devices in a sequencing set do not attempt their configured fault restart (retry). If fault spread mode is disabled and sequencing is also disabled, the device ignores faults from other devices and stays enabled.

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Protectable: Yes

Default Value: 00000000h (no fault spreading with legacy devices)

Units: N/A

Command	LEGACY_FAULT_GROUP (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															

Command	LEGACY_FAULT_GROUP (F0h)															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
31:0	Fault Group	N/A	00000000h	Identifies the devices in the fault spreading group.

STORE_DATA (F2h)

Definition: Stores the command settings in the USER and/or DEFAULT stores while the device is enabled. Used in conjunction with STORE_CONTROL (E3h). This command indicates to the device that the next 4 bytes are PMBus command codes and/or data. STORE_DATA commands, along with their 4 bytes of data, are repeatedly sent to the device until all configuration commands and data have been sent to the device. If the data that needs to be sent results in a STORE_DATA command that would have less than 4 bytes, the unused bytes should be filled with FFh. Note that these “filler” bytes are used when the CRC is calculated.

Data Length in Bytes: 4

Data Format: Custom

Type: R/W

Protectable: Yes

Default Value: N/A

Units: N/A

SNAPSHOT_CONTROL (F3h)

Definition: Controls, configures, and erases SNAPSHOT data. As shown in the following table, this command is used to arm and disarm SNAPSHOT, report back the number of SNAPSHOT data record locations that are available for new data, select the data record to read back, specify whether a single or multiple SNAPSHOT should be taken after a device is disabled, if a SNAPSHOT can only be taken when the device is enabled, enabling and disabling SNAPSHOT_CONTROL, and erasing all SNAPSHOT data.

The Erase All bit must be sent as a separate command. All other bits are ignored when the Erase All bit is sent. For example, 0000 0000 0000 0010b and 1111 1111 1111 1111b both (only) erase all SNAPSHOT data. The hose must wait at least 20ms before issuing any other PMBus commands after writing the Erase All bit.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00..00h

Units: N/A

Command	SNAPSHOT_CONTROL (F3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Setting	Description
15	SNAPSHOT Armed	0	Disabled	Not Armed
		1	Enabled	Armed. SNAPSHOT will happen on next fault (if it is not masked)
14:12	Not Used	000	Not used	Not used
11:8	Available SNAPSHOTs remaining	0000-1000	N/A	Number of 8 byte SNAPSHOT records available
7	One Time	0	Disabled	SNAPSHOT will be taken whenever a fault occurs
		1	Enabled	One SNAPSHOT will be taken when a fault occurs. Another SNAPSHOT will not be taken until the device has been disabled
6	After Enable	0	Disabled	SNAPSHOT may be taken at any time
		1	Enabled	SNAPSHOT will be taken only when the device is enabled (“turned on”)
5	Not Used	0	Not used	Not used
4:2	Read Location	000-111	NA/	Specifies which SNAPSHOT data record to return when the SNAPSHOT command is read
1	Erase All	1	(Write Only)	Erases all SNAPSHOT data. This ill cause Available Snapshots Remaining to become 8 (1000d) THIS BIT MUST BE SENT AS A SEPARATE COMMAND; that is, not combined with other bit settings
0	Enable	0	Disabled	Disables SNAPSHOT_CONTROL
		1	Enabled	Enables SNAPSHOT_CONTROL

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

PINSTRAP_READ_STATUS (F5h)

Definition: A 5-byte read-back of an index from 0 - 31 that corresponds to the resistor value for the designated pinstrap position.

Data Length in Bytes: 5

Data Format: Bit Field

Type: Block Read

Protectable: Yes (read only)

Default Value: N/A

Units: N/A

Byte	Value	Format
Byte 4	CFG0 resistor	8-bit integer
Byte 3	CFG1 resistor	8-bit integer
Byte 2	SYNC resistor index	8-bit integer
Byte 1	Factory Mode	8-bit integer
Byte 0 Bits 7:3	VSET/SA VSET resistor index	5-bit integer
Byte 0 Bits 2:0	VSET/SA Address resistor index	3-bit integer

IIN_CAL_OFFSET (F6h)

Definition: Used to account for input current that is consumed by bias currents which would not be consumed by the power supply's power train.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 8BD7h (0.03A)

Units: A

Range: -10A to 10A

Equation: IIN_OFFSET = $Y \times 2^N$

Command	IIN_OFFSET (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	0	0	1	0	1	1	1	1	0	1	0	1	1	1

SECURITY_CONTROL (FAh)

Definition: Used to read-back the security status of the USER and DEFAULT stores, clear protection status of non-password protected commands, and enable the automatic command protection mode (Auto Protect Mode). SECURITY_CONTROL is used along with the PASSWORD and WRITE_PROTECT commands to allow the user to disallow changes to selected commands.

Data Length in Bytes: 1

Data Format: Bit

Type: Read Byte

Protectable: No

Default Value: 01h

Units: N/A

Command	SNAPSHOT_CONTROL (F3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	Read	Read	Read	Read	Read	Read	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

Bits	Field Name	Value	Description
7:6	Not used	00	Not used
5	DEFAULT store protected	0	1 indicates that the DEFAULT store is protected
4	USER store protected	0	1 indicates that the USER store is protected
3:2	Not used	00	Not used
1	Clear protected	0	Writing a “1” clears all protected commands except the commands that are password protected
0	Auto protect	0	Writing a “1” enables auto protection mode

PASSWORD (FBh)

Definition: Sets the password string for the USER and DEFAULT stores. The USER and DEFAULT stores can have unique passwords. The initial (default) password for both stores is null (9 bytes of zeros in hexadecimal format - not 9 ASCII “0” characters). The DEFAULT store password has priority over the USER store password; that is, when the DEFAULT store password is written, protected commands in both the DEFAULT and USER stores can be written to.

Data Length in Bytes: 9

Data Format: ASCII. ISO/IEC 8859-1

Type: Block Write

Protectable: No

Default Value: 000000000000000000h (null)

Units: N/A

WRITE_PROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE - not used in this device) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are can be protected or are supported by the device. Setting a command's WRITE_PROTECT bit to "1" indicates that write-access to that command is allowed only if the appropriate password has been written to the device. Note that the USER and DEFAULT stores have unique passwords, and that writing the DEFAULT store password allows changes to both the USER and DEFAULT stores.

Data Length in Bytes: 32

Data Format: Custom

Type: Block R/W

Protectable: Yes

Default Value: 00..00h

Units: N/A

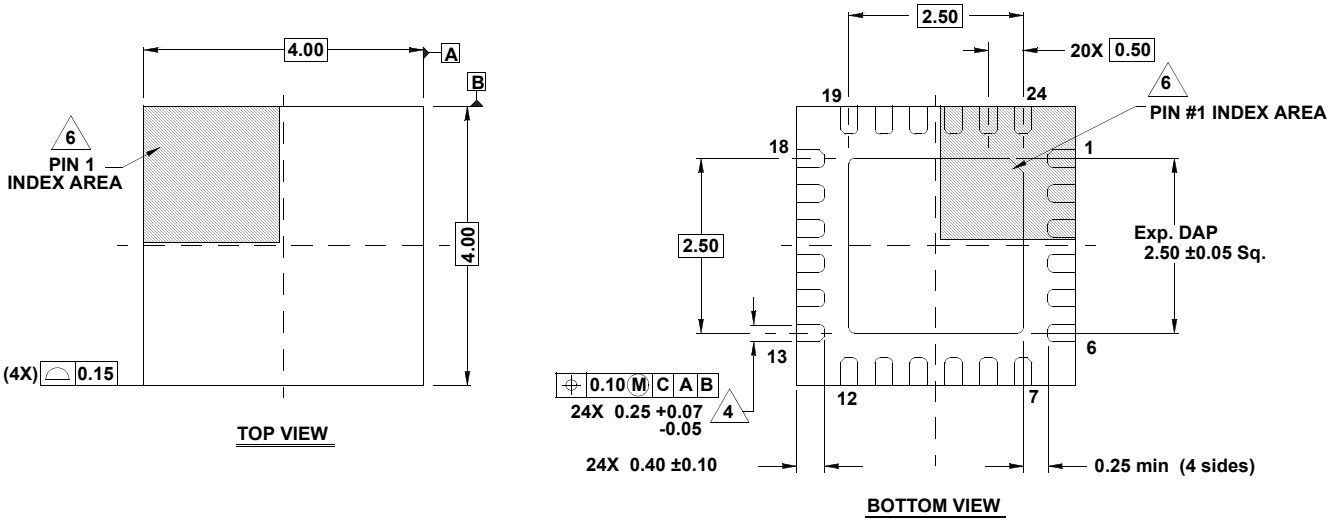
8. Revision History

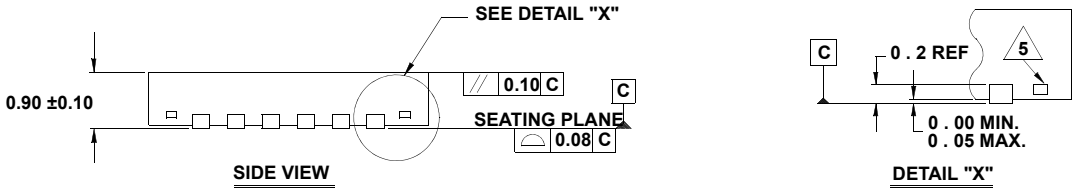
Rev.	Date	Description
0.00	Jun 7, 2018	Initial release.

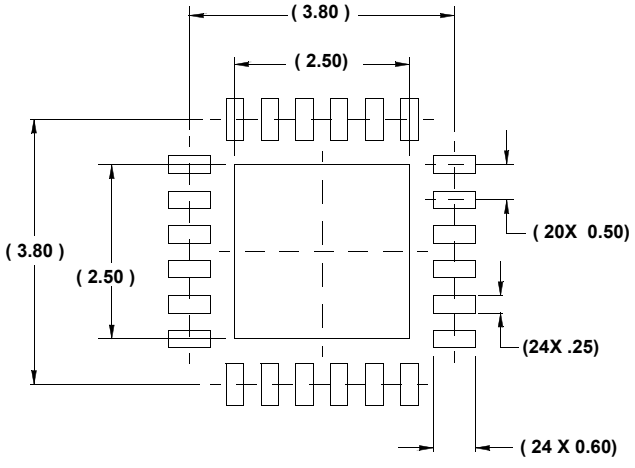
9. Package Outline Drawing

For the most recent package outline drawing, see L24.4x4H.

L24.4x4H
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 09/11







TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-220 VGGD-8

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