DATASHEET

ISL70040SEH, ISL73040SEH

Radiation Hardened Low-Side GaN FET Driver

FN8984
Rev.10.0
Jul 30, 2021

The ISL70040SEH and ISL73040SEH are low-side drivers designed to drive enhancement mode Gallium Nitride (GaN) FETs in isolated topologies and boost type configurations. The drivers operate with a supply voltage from 4.5V to 13.2V and have both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drives with a single device.

The ISL70040SEH and ISL73040SEH have a 4.5V gate drive voltage (V_{DRV}) generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of enhancement mode GaN FETs. The gate drive voltage also features an Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps OUTL turned on to ensure the GaN FET is in an OFF state whenever V_{DRV} is below the UVLO threshold.

The ISL70040SEH and ISL73040SEH inputs can withstand voltages up to 14.7V regardless of the V_{DD} voltage. This allows the ISL70040SEH and ISL73040SEH inputs to be connected directly to most PWM controllers. The ISL70040SEH and ISL73040SEH split outputs offer the flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance to the turn-on/off paths.

The ISL70040SEH and ISL73040SEH operate across the military temperature range from -55°C to +125°C and are offered in an 8 Ld hermetically sealed ceramic Surface Mount Device (SMD) package or die form.

Features

- **Wide operating voltage range of 4.5V to 13.2V**
- **Up to 14.7V logic inputs (regardless of V_{DD} level)**
    - **Inverting and non-inverting inputs**
- **Optimized to drive enhancement mode GaN FETs**
    - **Internal 4.5V regulated gate drive voltage**
    - **Independent outputs for adjustable turn-on/turn-off speeds**
- Full military temperature range operation
    - T_A = -55°C to +125°C
    - T_J = -55°C to +150°C
- Radiation acceptance testing - ISL70040SEH
    - HDR (50-300rad(Si)/s): 100krad(Si)
    - LDR (0.01rad(Si)/s): 75krad(Si)
- Radiation acceptance testing - ISL73040SEH
    - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE hardness (see the SEE Report for details)
    - No SEB/L LET_{TH}, V_{DD} = 14.7V: 86MeV•cm^2/mg
    - No SET, LET_{TH}, V_{DD} = 13.2V: 86MeV•cm^2/mg
- Electrically screened to DLA SMD 5962-17233

Applications

- Flyback and forward converters
- Boost and PFC converters
- Secondary synchronous FET drivers

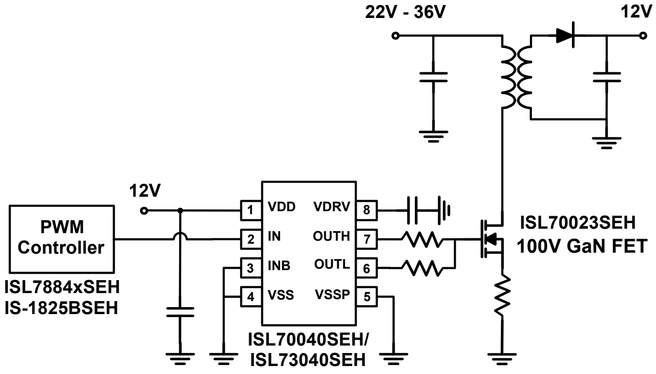


Figure 1. ISL70040SEH/ISL73040SEH 8 Ld SMD Package

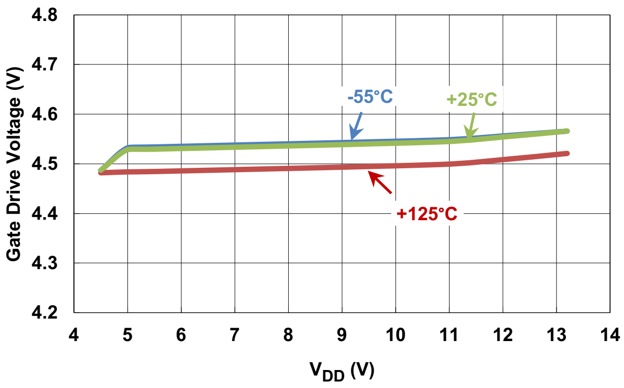


Figure 2. V_{DRV} Line Regulation vs Temperature

Contents

1. Overview

1.1 Typical Application Schematic

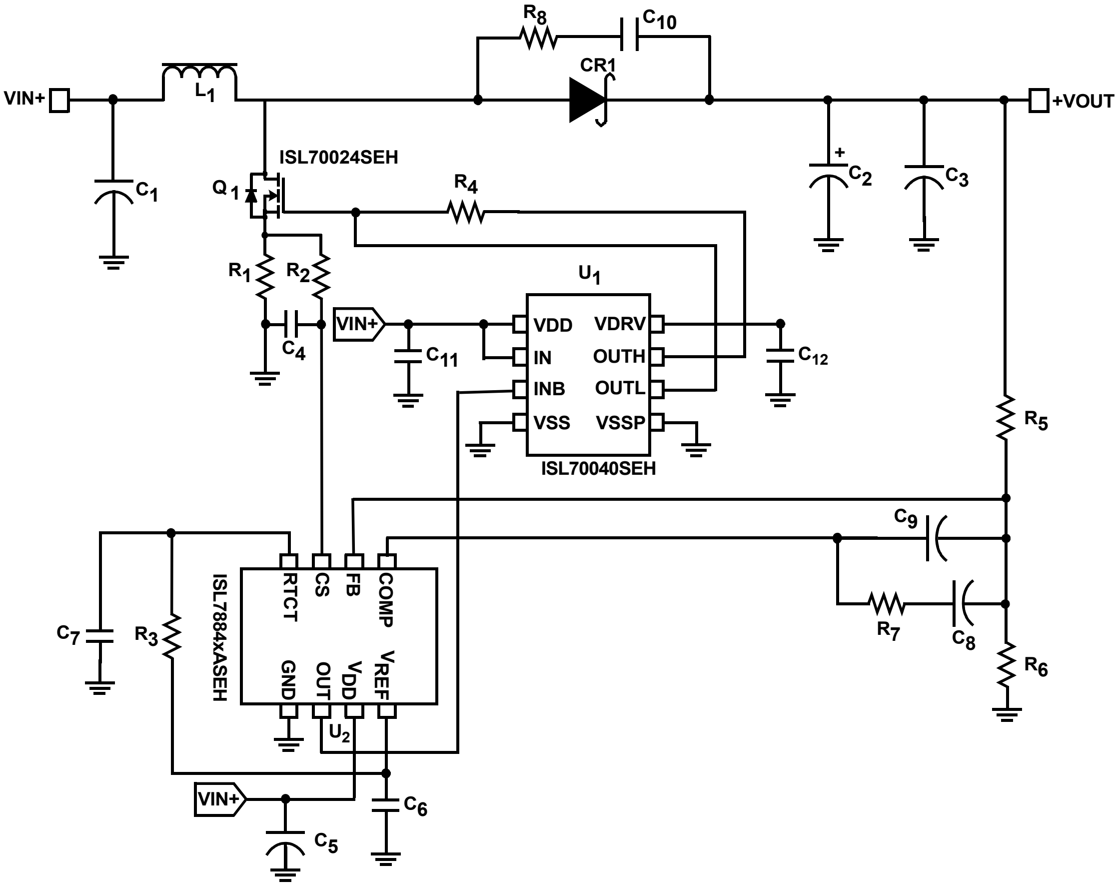


Figure 3. ISL70040SEH and ISL73040SEH Typical Application Schematic

1.2 Functional Block Diagram

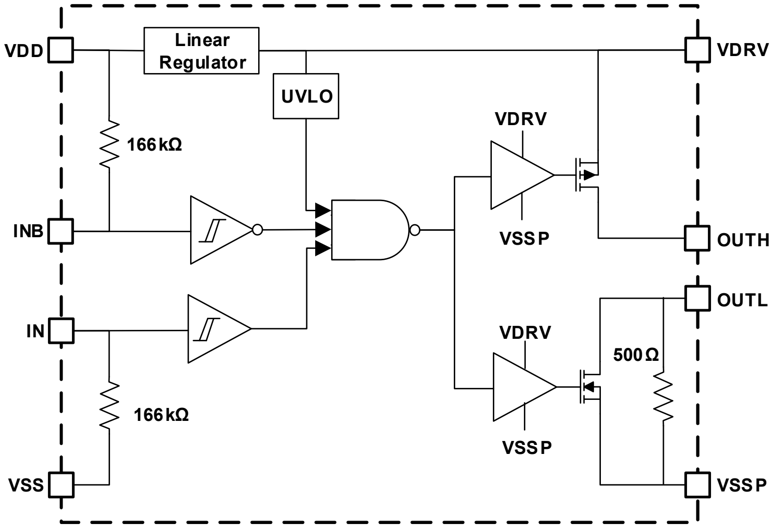


Figure 4. Block Diagram

1.3 Ordering Information

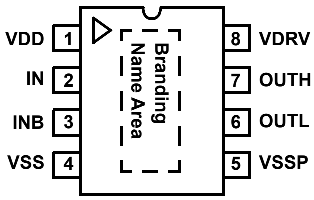
Ordering SMD Number (Note 1)	Part Number (Note 2)	Radiation Hardness (Total Ionizing Dose)		Package (RoHS Compliant)	Package Drawing	Temperature Range
		HDR	LDR			
5962R1723301VXC	ISL70040SEHVL	100krad(Si)	75krad(Si)	8 Ld SMD	J8.A	-55 to +125°C
5962R1723301V9A	ISL70040SEHVX (Note 3)	100krad(Si)	75krad(Si)	Die	-	
N/A	ISL70040SEHL/PROTO (Note 4)	-	-	8 Ld SMD	J8.A	
N/A	ISL70040SEHX/SAMPLE (Notes 3, 4)	-	-	Die	-	
5962L1723302VXC	ISL73040SEHVL	-	75krad(Si)	8 Ld SMD	J8.A	
5962L1723302V9A	ISL73040SEHVX(Note 3)	-	75krad(Si)	Die	-	
N/A	ISL73040SEHL/PROTO (Note 4)	-	-	8 Ld SMD	J8.A	
N/A	ISL73040SEHX/SAMPLE (Notes 3, 4)	-	-	Die	-	
N/A	ISL70040SEHEV2Z (Note 5)	Evaluation Board with ISL70040SEH/ISL70023SEH				
N/A	ISL70040SEHEV3Z (Note 5)	Evaluation Board with ISL70040SEH/ISL70024SEH				
N/A	ISL73040SEHEV4Z (Note 5)	Half Bridge Power Stage using the ISL73040SEH, ISL73024SEH, and the ISL71610M				
N/A	ISL70040SEHEV5Z (Note 5)	Evaluation Board with ISL70040SEH/ISL70020SEH				

Notes:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 7.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

1.4 Pin Configuration

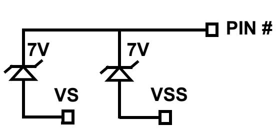
8 Ld SMD
Top View



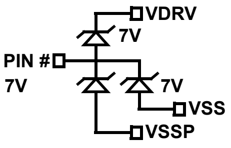
NOTE: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.5 Pin Descriptions

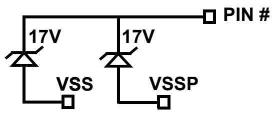
Pin Number	Pin Name	ESD Circuit	Description
1	VDD	3	Supply for the ISL70040SEH and ISL73040SEH internal linear regulator. Locally bypass the supply to VDD using at least a 4.7µF ceramic capacitor.
2	IN	3	Non-inverting input pin which controls the OUTH and OUTL outputs. This input has TTL/CMOS type thresholds. When using this device in an inverting application, tie this pin to VDD to enable the outputs. The IN pin has a 166kΩ internal pull-down resistor to VSS.
3	INB	3	Inverting input pin which controls the OUTH and OUTL outputs. This input has TTL/CMOS type thresholds. When using this device in a non-inverting application, tie this pin to VSS to enable the outputs. The INB pin has a 166kΩ internal pull-up resistor to VDD.
4	VSS	4	Supply ground. Connect this pin to VSSP from the PCB ground plane.
5	VSSP	4	Power supply ground. Connect this pin to VSS from the PCB ground plane.
6	OUTL	2	Output low pin which is the gate driver turn-off output. Connect to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-off speed.
7	OUTH	1	Output high pin which is the gate driver turn-on output. Connect to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-on speed.
8	VDRV	1	Internal linear regulator output and the gate drive voltage. Locally bypass this pin using at least a 4.7µF ceramic capacitor; 2µF to 10µF with variability.
N/A	LID	N/A	Internally connected to VSSP (Pin 5).



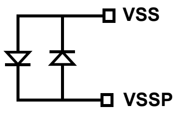
Circuit 1



Circuit 2



Circuit 3



Circuit 4

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	-0.3	+16.5	V
IN, INB	-0.3	+16.5	V
OUTL, OUTH, VDRV	-0.3	+6.5	V
V_{DD} (Note 6)	-0.3	+16.5	V
IN, INB (Note 6)	-0.3	+16.5	V
OUTL, OUTH, VDRV (Note 6)	-0.3	+6.2	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	6		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	2		kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

6. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg at +125°C (T_C).

2.2 Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}	Unit
SMD Package J8.A (Notes 7, 8)	59	10	°C/W

Notes:

7. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
8. For θ_{JC}, the “case temp” location is on the solder terminations adjacent to the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-55	+125	°C
V_{DD}	4.5	13.2	V
IN, INB	4.5	13.2	V

2.4 Electrical Specifications

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, r_{OUTH} = r_{OUTL} = 0Ω, no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at an HDR of 50-300rad(Si)/s (ISL70040SEH only); or over a total ionizing dose of 75krad(Si) with exposure at an LDR of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 10)	Typ (Note 9)	Max (Note 10)	Unit
Power Supply						
Quiescent Supply Current	I_{DDQ}	V_{DD} = 4.5V, IN = 0V, INB = V_{DD}	-	1.4	**2.5**	mA
		V_{DD} = 13.2V, IN = 0V, INB = V_{DD}	-	1.5	**2.5**	mA
Operating Supply Current	I_{DDO}	V_{DD} = 4.5V, f_{PWM} = 500kHz	-	6.8	**13.0**	mA
		V_{DD} = 13.2V, f_{PWM} = 500kHz	-	7.3	**15.0**	mA
Gate Drive Voltage						
Output Voltage	V_{DRV}	V_{DD} = 4.5V	**4.29**	4.44	-	V
		V_{DD} = 13.2V	**4.34**	4.57	**4.71**	V
Current Limit of V_{DRV}	I_{LIM}	V_{DD} = 4.5V, 13.2V	**50**	143	**300**	mA
Under Voltage Lockout (UVLO) on V_{DRV}						
UVLO Rising Threshold	V_{RDRV}		**3.75**	3.98	**4.15**	V
UVLO Falling Threshold	V_{FDRV}		**3.40**	3.74	**4.00**	V
UVLO Hysteresis	V_{HDRV}		**100**	238	**375**	mV
Input Pins						
High Level Threshold	V_{IH}		-	1.7	**2.0**	V
Low Level Threshold	V_{IL}		**1.0**	1.4	-	V
Input Hysteresis	V_{IHYS}		**120**	290	**450**	mV
Pull-Up/Down Resistor	$R_{INU/D}$	IN to V_{SS}, INB to V_{DD}	**97**	166	**362**	kΩ
Input Leakage Current	$I_{IN/INB}$		**-1**	-	**1**	µA
OUTH Output						
Peak Source Current (Note 11)	I_{SRC}	C_L = 220nF (Figure 6)	**1.0**	1.5	**3.0**	A
Driver Output Resistance	r_{ONP}	IOUTH = 45mA	-	2.2	**3.2**	Ω
Output Leakage Current	I_{LKP}	OUTH = 0V, 4.5V	**-1**	-	**1**	µA
OUTL Output						
Peak Sink Current (Note 11)	I_{SNK}	C_L = 220nF (Figure 6)	**1.5**	2.8	**4.0**	A
Driver Output Resistance	r_{ONN}	OUTH = VDRV, I_{OUTL} = -45mA	-	0.5	**1.0**	Ω
		OUTH = OUTL, I_{OUTL} = -45mA	-	1.7	**3.0**	Ω
Gate Hold-Off Resistance	$r_{OUTL\text{-}P}$	VDD = 0V, OUTL = 0.7V	**400**	500	**700**	Ω

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, r_{OUTH} = r_{OUTL} = 0Ω, no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at an HDR of 50-300rad(Si)/s (ISL70040SEH only); or over a total ionizing dose of 75krad(Si) with exposure at an LDR of <10mrad(Si)/s. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 10)	Typ (Note 9)	Max (Note 10)	Unit
Switching Characteristics						
Turn-ON Propagation Delay	t_{DON}	C_L = 1000pF (Figure 5)	**15**	40	**65**	ns
Turn-OFF Propagation Delay	t_{DOFF}	C_L = 1000pF (Figure 5)	**15**	39	**65**	ns
Propagation Delay Matching	t_{DM}	$\|t_{DON} - t_{DOFF}\|$	**-8**	1	**8**	ns
Rise Time (10% to 90%) (Note 11)	t_{RISE}	C_L = 200pF	-	5.5	-	ns
		C_L = 1500pF	-	12.5	-	ns
		C_L = 10000pF	**21**	57	**90**	ns
Fall Time (90% to 10%) (Note 11)	t_{FALL}	C_L = 200pF	-	4.0	-	ns
		C_L = 1500pF	-	7.5	-	ns
		C_L = 10000pF	**16**	32	**50**	ns

Notes:

9. Typical values shown are not guaranteed.
10. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
11. Test applies only to packaged parts due to hardware limitations at wafer probe.

2.5 Timing Diagrams

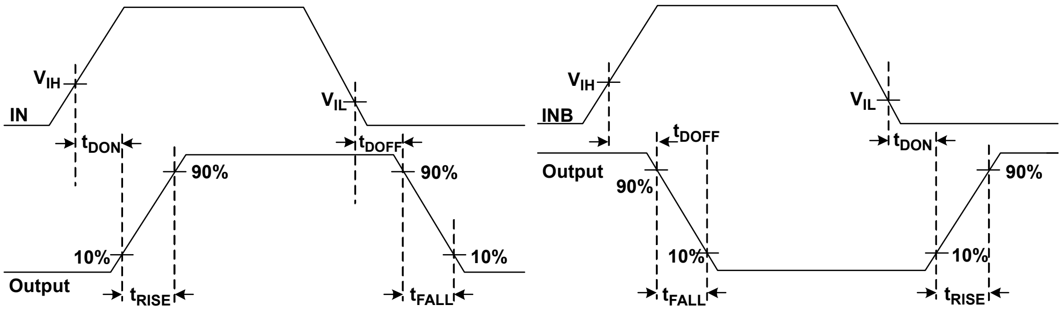


Figure 5. Timing Diagram, OUTH and OUTL Tied Together

$$i_{PEAK} = 200nF \times \frac{\Delta v}{\Delta t}$$

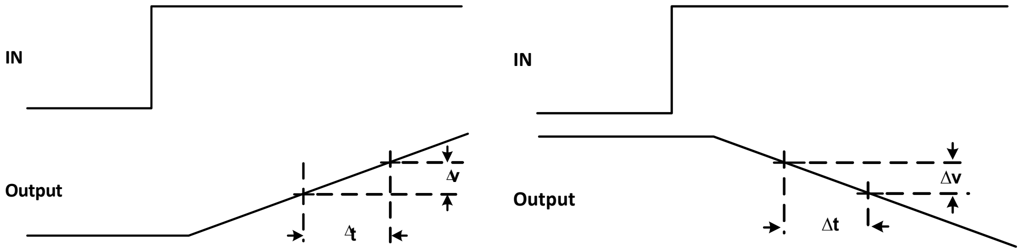


Figure 6. Peak Source/Sink Measurement

3. Typical Performance Curves

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, r_{OUTH} = r_{OUTL} = 0Ω.

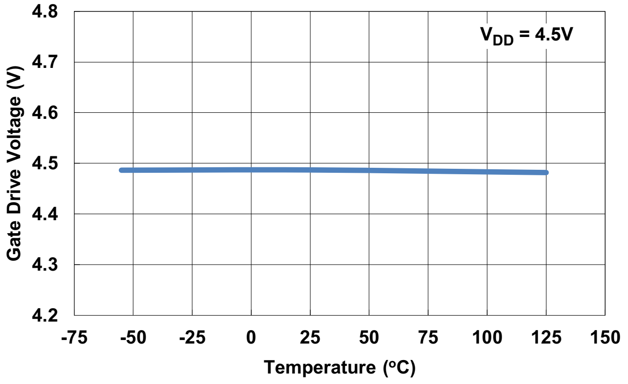


Figure 7. V_{DRV} vs Temperature

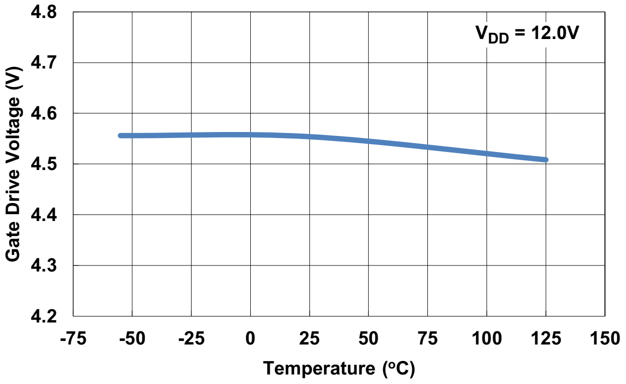


Figure 8. V_{DRV} vs Temperature

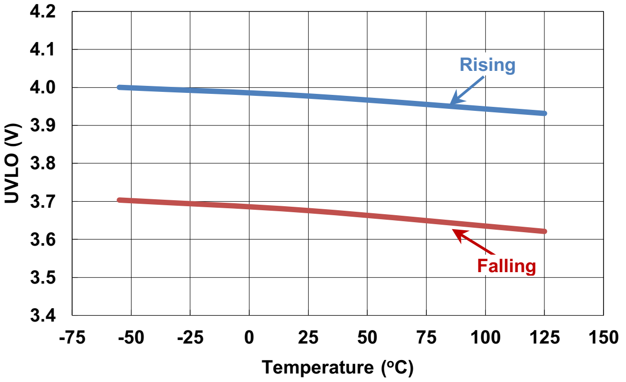


Figure 9. V_{DRV} Undervoltage Lockout Threshold

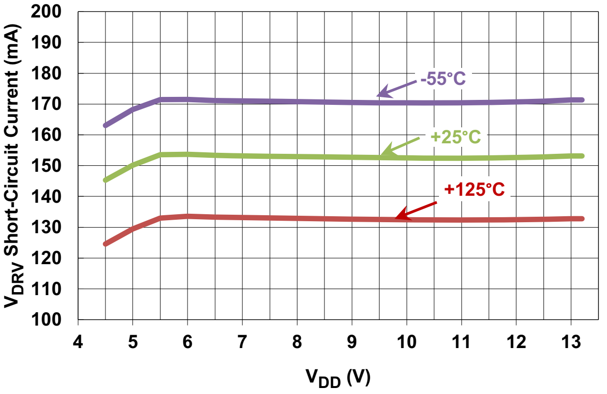


Figure 10. V_{DRV} Short-Circuit Current vs Temperature

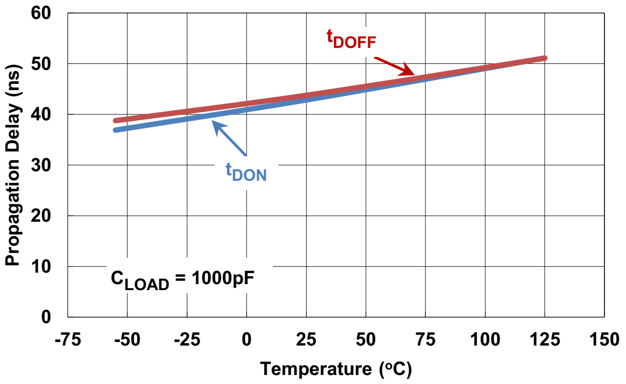


Figure 11. Input Propagation Delay vs Temperature

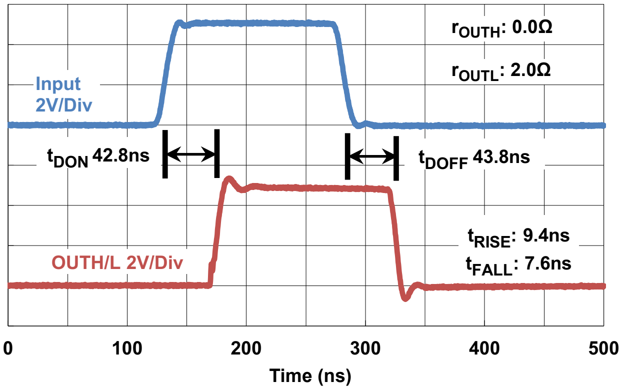


Figure 12. Input Propagation Delay

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, r_{OUTH} = r_{OUTL} = 0Ω. **(Continued)**

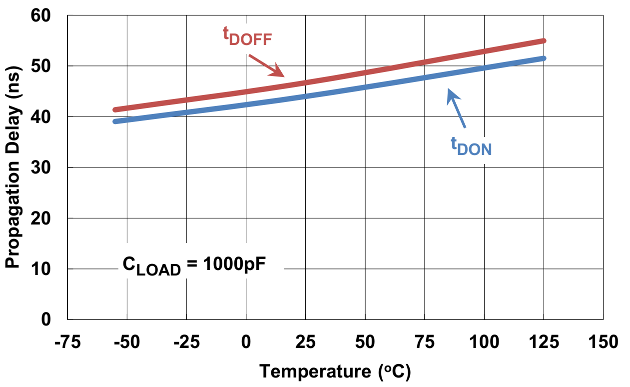


Figure 13. Input Bar Propagation Delay vs Temperature

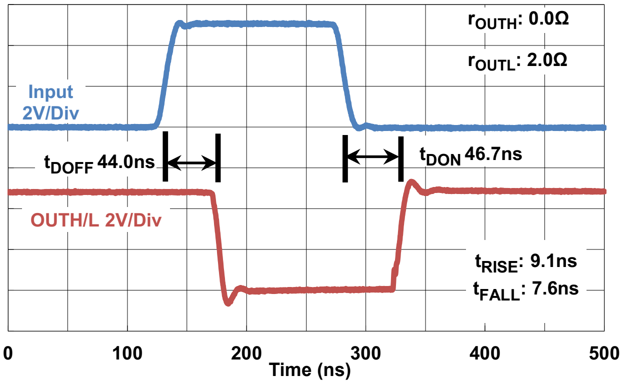


Figure 14. Input Bar Propagation Delay

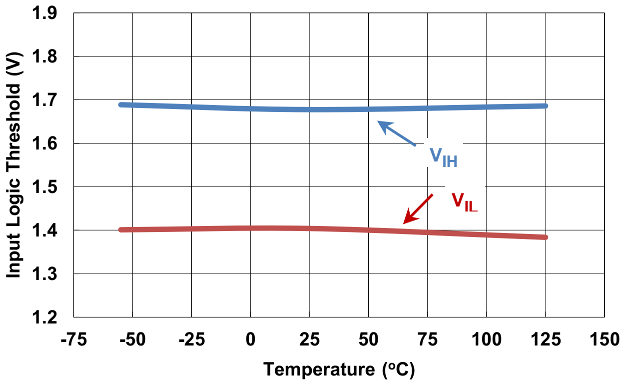


Figure 15. Input Logic Threshold vs Temperature

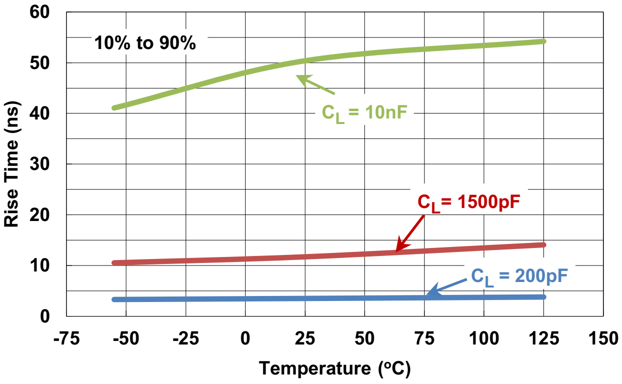


Figure 16. Output Rise Times vs Temperature

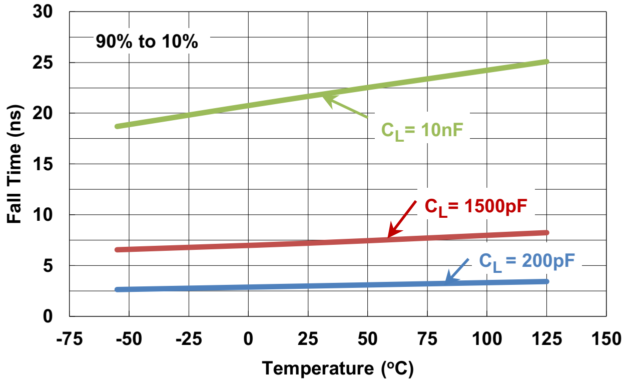


Figure 17. Output Fall Times vs Temperature

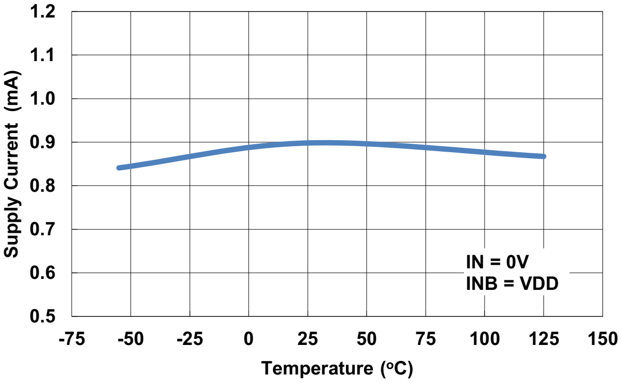


Figure 18. Quiescent Supply Current vs Temperature

Unless otherwise noted, V_{DD} = 4.5V, 13.2V, V_{SS} = VSSP = 0V, C_{VDRV} = 4.7µF, V_{IH} = 5.0V, V_{IL} = 0V, no load on OUTH/OUTL, r_{OUTH} = r_{OUTL} = 0Ω. **(Continued)**

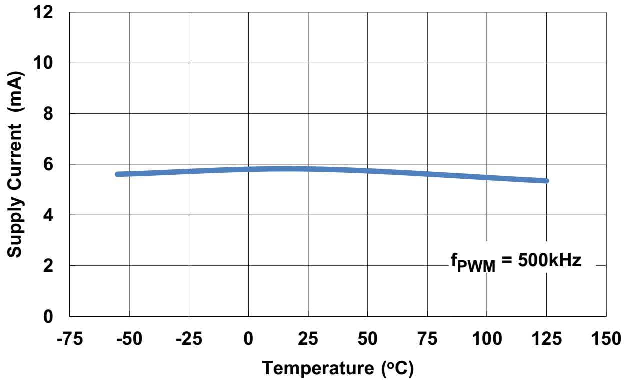


Figure 19. Operating Supply Current vs Temperature

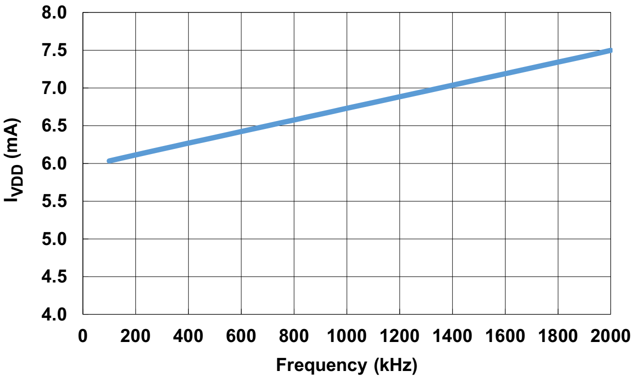


Figure 20. Operating Supply Current vs Frequency

4. Functional Description

4.1 Gate Drive for N-Channel GaN FETs

Technologies based on wide-band gap semiconductors produce High Electron Mobility Transistors (HEMT). An example of a HEMT is the GaN based power transistors such as the ISL70020SEH, ISL70023SEH, and ISL70024SEH, which offer very low $r_{DS(ON)}$ and gate charge (Qg). These attributes make the devices capable of supporting very high switching frequency operation while not suffering significant efficiency loss. However, GaN power FETs have special requirements in terms of gate drive, which the ISL70040SEH and ISL73040SEH are designed to specifically address.

The key properties of a gate driver for GaN FETs are:

(1) Gate drive signals need to be sufficiently higher than the V_{GS} threshold specified in GaN FET datasheets for proper operation.

(2) A well regulated gate drive voltage to keep the V_{GS} lower than specified absolute maximum level of 6V.

(3) Split pull-up and pull-down gate connections to add series gate resistors to independently adjust turn-on and turn-off speed, without the need for a series diode with a voltage drop that may cause an insufficient gate drive voltage.

(4) Driver pull-down resistance <0.5Ω (typical) to eliminate undesired Miller turn-on.

(5) High current source/sink capability and low propagation delay to achieve high switching frequency operation.

4.2 Functional Overview

The ISL70040SEH and ISL73040SEH are single channel high speed enhanced mode GaN FET low-side drivers for isolated power supplies and Synchronous Rectifier (SR) applications.

The ISL70040SEH and ISL73040SEH offer a wide operating supply range of 4.5V to 13.2V. The gate drive voltage is generated from an internal linear regulator to keep the gate-source voltage below the absolute maximum level of 6V for the ISL7002xSEH GaN FET devices.

The input stage can handle inputs to the 14.7V independent of V_{DD} and offers both inverting and non-inverting inputs. The split output stage is capable of sourcing and sinking high currents and allows for independent tuning of the turn-on and turn-off times. The typical propagation delay of 40ns enables high switching frequency operation.

5. Applications Information

5.1 Undervoltage Lockout

The VDD pin accepts a recommended supply voltage range of 4.5V to 13.2V and is the input to the internal linear regulator. VDRV is the output of the regulator and is equal to 4.5V. VDRV provides the bias for all internal circuitry and the gate drive voltage for the output stage.

An UVLO circuitry monitors the voltage on VDRV and is designed to prevent unexpected glitches when VDD is being turned on or turned off. When VDRV < ~1V, an internal 500Ω resistor connected between OUTL and ground helps keep the gate voltage close to ground. When ~1.2V < VDRV < UV, OUTL is driven low while ignoring the logic inputs and OUTH is in a high impedance state. This low state has the same current sinking capacity as during normal operation. This ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates from the Miller capacitance.

When VDRV > UVLO, the output responds to the logic inputs following the next rising edge on IN or falling edge on INB. In the non-inverting operation (PWM signal applied to the IN pin) the output is in phase with the input. In the inverting operation (PWM signal applied to the INB pin) the output is out of phase with the input.

For the negative transition of VDD through the UV lockout voltage, the OUTL is active low and OUTH is high impedance when VDRV < ~3.7VDC, regardless of the input logic states.

5.2 Input Stage

The ISL70040SEH and ISL73040SEH input thresholds are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. With typical high threshold = 1.7V and typical low threshold = 1.4V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

The ISL70040SEH and ISL73040SEH offer both inverting and non-inverting inputs. The state of the output pin is dependent on the bias on both input pins. Table 1 summarizes the inputs to output relation.

Table 1. Truth Table

IN	INB	OUT	OUTH	OUTL
0	0	0	Hi-Z	0
0	1	0	Hi-Z	0
1	0	1	1	Hi-Z
1	1	0	Hi-Z	0

Note: OUT is the combination of OUTH and OUTL connected together. Hi-Z represents a high impedance state.

As a protection mechanism, if any of the input pins are left in a floating condition, OUTL is held in the low state and OUTH is high impedance. This is achieved using a 166kΩ pull-up resistor on the INB pin to VDD and a 166kΩ pull-down resistor on the IN pin to VSS. For proper operation in non-inverting applications, connect INB to VSS. For proper operation in inverting applications, connect IN to VDD.

5.3 Enable Function

An enable or disable function can be easily implemented in the ISL70040SEH and ISL73040SEH using the unused input pin. The following guidelines describe how to implement an enable/disable function:

- In a non-inverting configuration, the INB pin can implement the enable/disable function. OUT is enabled when INB is biased low, acting as an active low enable pin
- In an inverting configuration, the IN pin can implement the enable and disable function. OUT is enabled when IN is biased high, acting as an active high enable pin

5.4 Power Dissipation of the Driver

The power dissipation of the ISL70040SEH and ISL73040SEH is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation, but is usually not significant compared to the gate charge losses.

For example, the ISL70024SEH has a total gate charge of 5nC when $V_{DS} = 100V$ and $V_{GS} = 4.5V$. This is the charge that a driver must source to turn on the GaN FET and must sink to turn off the GaN FET.

Use Equation 1 to calculate the power dissipation of the driver:

$$P_D = Q_c \bullet freq \bullet V_{GS} \bullet \frac{r_{DS(ON)}}{r_{gate} + r_{DS(ON)}} + I_{DD}(freq) \bullet V_{DD} + \frac{V_{GS}}{r_{PD}} \bullet VDD \bullet D \quad \text{(EQ. 1)}$$

where:

freq = Switching frequency

$V_{GS} = V_{DRV}$ bias of the ISL70040SEH and ISL73040SEH

Q_c = Gate charge for V_{GS}

$I_{DD}(freq)$ = Bias current at the switching frequency

$r_{DS(ON)}$ = ON-resistance of the driver

r_{gate} = External gate resistance (if any)

r_{PD} = Internal 500Ω pull-down resistance

D = Duty cycle that OUTL is equal to V_{GS} (V_{DRV}) during one switching cycle.

Note: The gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

5.5 General PCB Layout Guidelines

The AC performance of the ISL70040SEH and ISL73040SEH depends significantly on the design of the Printed Circuit Board (PCB). The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induces significant voltage transients on the associated traces
- Keep power loops as short as possible by paralleling the source and return traces
- Use planes where practical; they are usually more effective than parallel traces
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines
- When practical, minimize impedances in low level signal circuits. The noise that is magnetically induced on a 10kΩ resistor is 10 times larger than the noise on a 1kΩ resistor
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended
- Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{DRV}, V_{DD}, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If using vias, connect several paralleled vias to reduce the inductance of the vias

- It may be necessary to add resistance to dampen resonating parasitic circuits, especially on OUTH. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance
- Keep high dv/dt nodes away from low level circuits. Guard banding can shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL70040SEH and ISL73040SEH
- Avoid placing a signal ground plane under a high amplitude dv/dt circuit. This injects di/dt currents into the signal ground paths
- Calculate power dissipation and voltage drop for the power traces. Many PCB/CAD programs have built-in tools for calculating trace resistance
- Large power components (such as power FETs, electrolytic caps, and power resistors) have internal parasitic inductance which cannot be eliminated. Account for this in the PCB layout and circuit design
- If the circuits are simulated, consider including parasitic components, especially parasitic inductance
- The GaN FETs have a separate substrate connection which is internally tied to the source pin. Source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and thick as possible

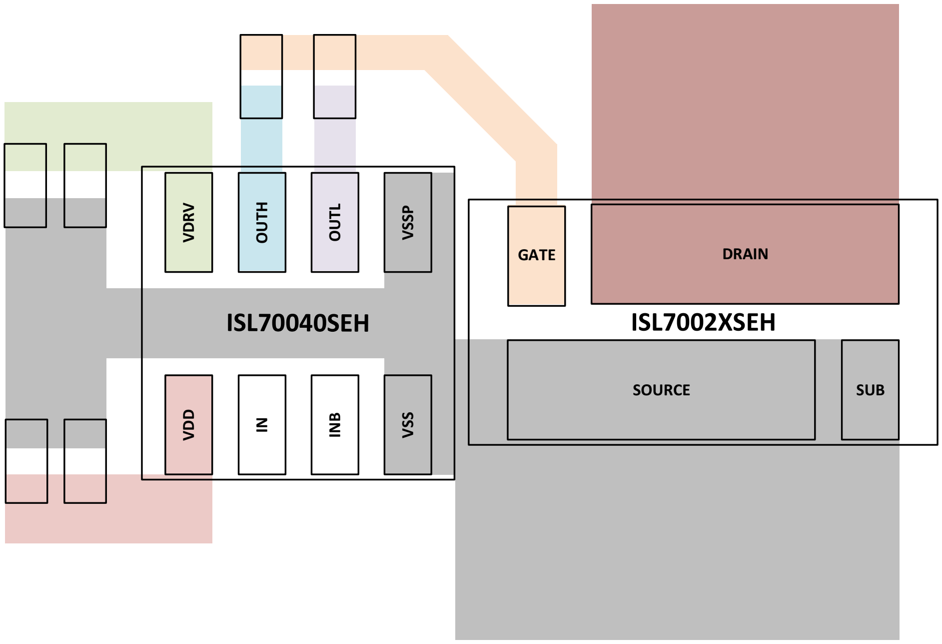


Figure 21. PCB Layout Recommendation

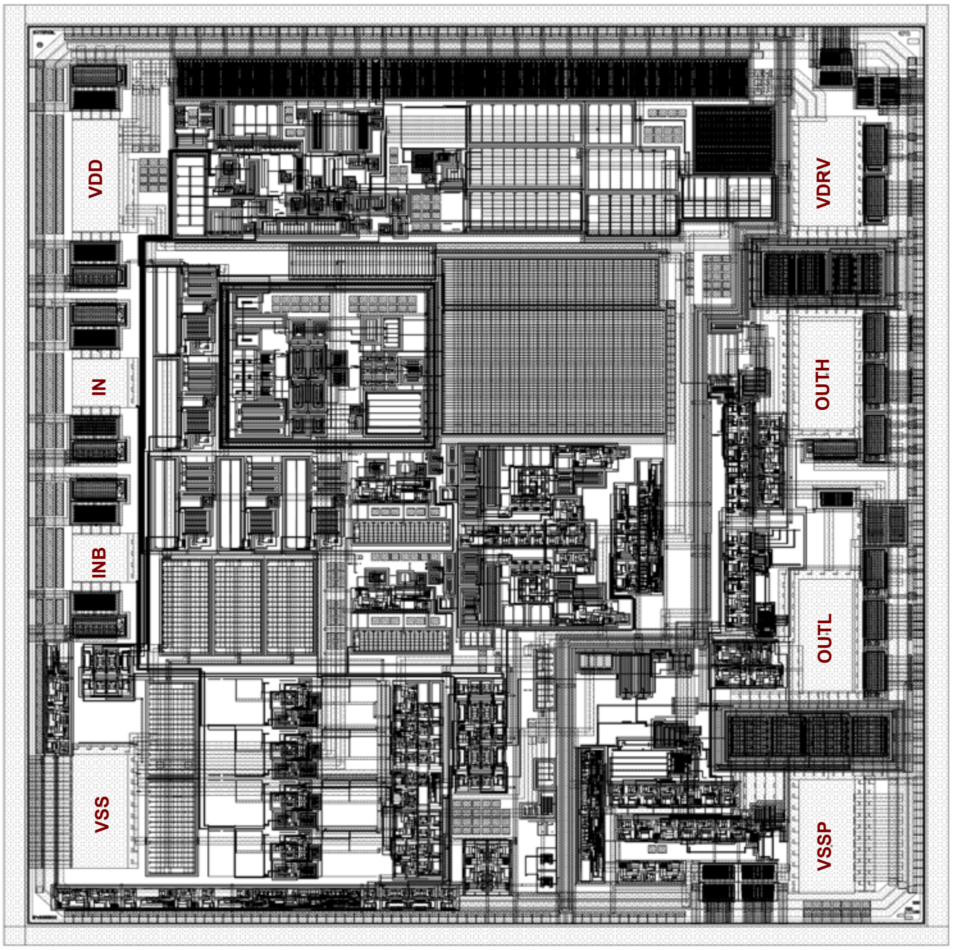
6. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Weight of Packaged Device	
Typical	0.22g (J8.A package)
Lid Characteristics	
Finish	Gold
Lid Potential	GND (VSSP)
Die Information	
Dimensions	2230µm x 2483µm (87.8 mils x 97.8 mils) Thickness: 305µm ±25.4µm (12 mils ±1 mil)
Interface Materials	
Glassivation	Type: Silicon Oxide and Silicon Nitride Thickness: 0.3µm ±0.03µm to 1.2µm ±0.12µm
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 2.7µm ±0.4µm
Backside Finish	Silicon
Process	0.6µm BiCMOS Junction Isolated
Assembly Information	
Substrate Potential	GND (VSS)
Additional Information	
Worst Case Current Density	$<2 \times 10^5 A/cm^2$
Transistor Count	1389

6.1 Metallization Mask Layout

ISL70040SEH and ISL73040SEH



6.2 Bond Pad Coordinates

Table 3. Layout X-Y Coordinates (Centroid of Bond Pad)

Pad Number	Pad Name	X (µm)	Y (µm)	ΔX (µm)	ΔY (µm)	Bond Wire Size (mils)
1	V_{DD}	171.0	1968.15	120	290	1.25
2	IN	171.0	1423.85	120	135	1.25
3	INB	171.0	964.25	120	135	1.25
4	VSS	171.0	298.2	120	290	1.25
5	VSSP	1878.65	231.0	120	290	1.25
6	OUTL	1878.65	758.5	120	290	1.25
7	OUTH	1878.65	1446.95	120	290	1.25
8	VDRV	1878.65	1973.85	120	290	1.25

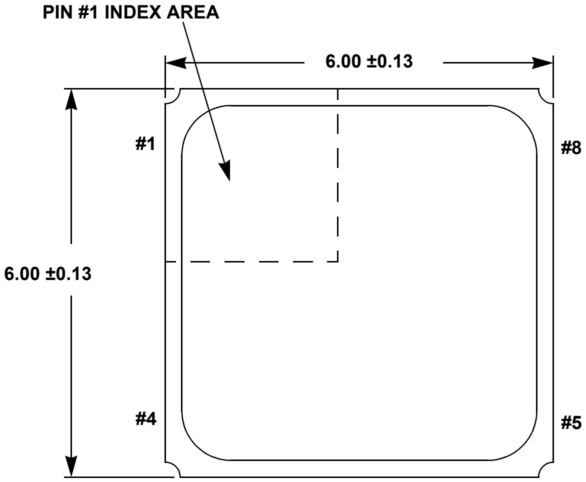
7. Revision History

Rev.	Date	Description
10.0	Jul 30, 2021	Updated block diagram. Updated pin descriptions for the IN and INB pins. Added labels to Figures 11, 13, 16, 18, and 19. Added Figure 20. Updated Input Stage section changing the 300kΩ to 166kΩ. Updated Equation 1.
9.0	Feb 4, 2021	Updated Radiation Assurance feature bullets to new standard. Added Note 3. Removed Table 1.
8.0	Mar 26, 2020	Added ISL70040SEHEV5Z to the ordering information table.
7.0	Jan 30, 2019	Added ISL73040SEHEV4Z to the ordering information table.
6.0	Nov 19, 2018	Corrected typographical error in Table 4 Bond Wire Size units to mils and values from 1.5 to 1.25.
5.0	Jul 12, 2018	Updated Figure 4 on page 3 and Figure 14 on page 10.
4.0	Apr 6, 2018	Updated the description of VDRV > UVLO conditions on page 13.
3.0	Feb 5, 2018	In Absolute Maximum Ratings on page 6, updated the maximum specification for V_{DD} and IN, INB.
2.0	Jan 19, 2018	Updated Figure 1. Removed About Intersil section. Updated Disclaimer.
1.0	Dec 7, 2017	Added Note 2 reference. Updated Pin 8 Description. Updated HBM value from 4kV to 6kV. Updated Electrical specification and Typical performance curve headings. Updated 36ms to 40ms on page 12 in last sentence.
0.0	Nov 29, 2017	Initial release

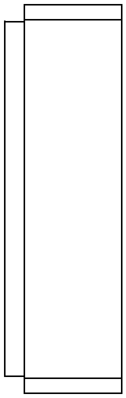
8. Package Outline Drawing

For the most recent package outline drawing, see J8.A.

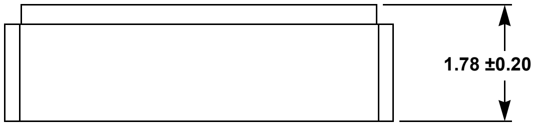
J8.A
8 Pin 6mm x 6mm Hermetic Surface Mount Package
Rev 0, 3/16



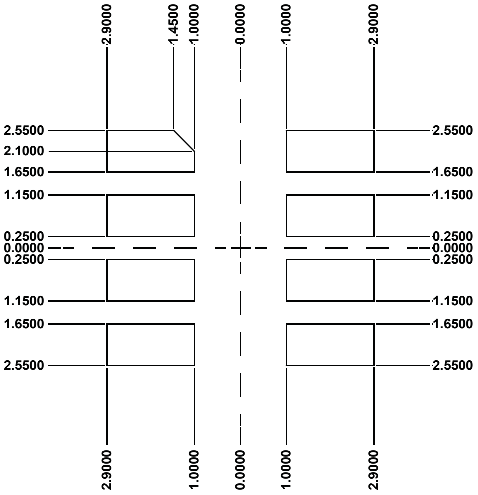
TOP VIEW



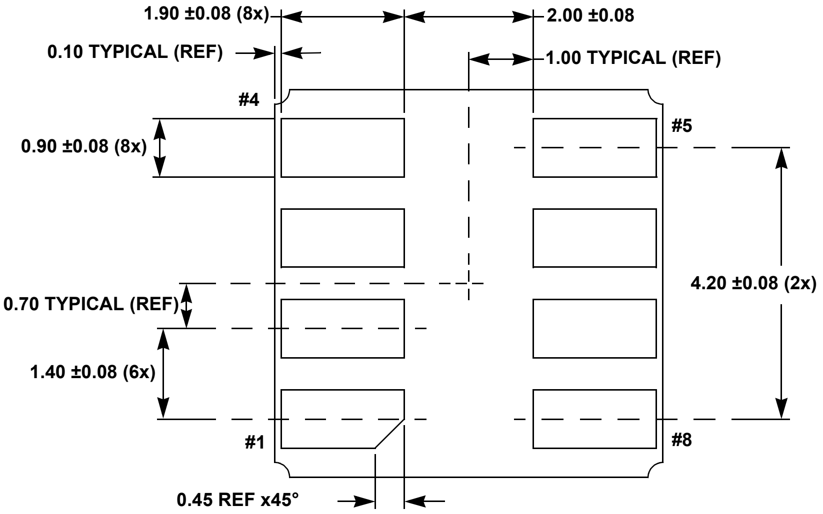
SIDE VIEW



END VIEW



TYPICAL RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

1. The corner shape (radius, chamfer, etc.) may vary at the manufacturers option from that shown on the drawing.
2. The package thickness dimension is the package height before being solder dipped.
3. Dimensions are in millimeters.

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(Rev.1.0 Mar 2020)

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