DATASHEET

# ISL70419SEH

Radiation Hardened 36V Quad Precision Low Power Operational Amplifier With Enhanced SET Performance

FN8653
Rev.2.00
Oct 15, 2018

The ISL70419SEH contains four very high precision amplifiers featuring the perfect combination of low noise vs power consumption. Low offset voltage, low $I_{BIAS}$ current, and low temperature drift make it the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of high precision, low noise, low power, and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ISL70419SEH is offered in a 14 Ld hermetic ceramic flatpack package. The device is offered in an industry standard pin configuration and operates across the extended temperature range from -55°C to +125°C.

## Applications

- Precision instrumentation
- Spectral analysis equipment
- Active filter blocks
- Thermocouples and RTD reference buffers
- Data acquisition
- Power supply control

## Features

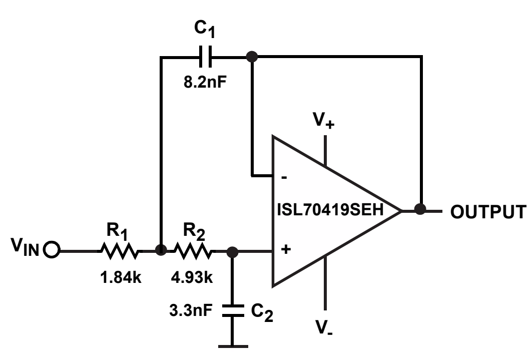
- Electrically screened to DLA SMD# 5962-14226
- Low input offset voltage. . . . . . . . . . . . . . . . . . ±110µV, Max.
- Superb offset temperature coefficient. . . . . . . 1µV/°C, Max.
- Input bias current . . . . . . . . . . . . . . . . . . . . . . . . . ±15nA, Max.
- Input bias current TC . . . . . . . . . . . . . . . . . . . . ±5pA/°C, Max.
- Low current consumption . . . . . . . . . . . . . . . . . . . . . . . 440µA
- Voltage noise . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 8nV/√Hz
- Wide supply range . . . . . . . . . . . . . . . . . . . . . . . . .4.5V to 36V
- Operating temperature range. . . . . . . . . . . .-55°C to +125°C
- Radiation environment
  - SEB $LET_{TH}$ ($V_S$ = ±18V) . . . . . . . . . . . . 86.4 MeV•$cm^2$/mg
  - SET recovery time . . . . . . . . . . ≤ 10µs at 60 MeV•$cm^2$/m
  - SEL immune (SOI process)
  - Total dose HDR (50-300rad(Si)/s) . . . . . . . . . . 300krad(Si)
  - Total dose LDR (10mrad(Si)/s) . . . . . . . . . . .100krad(Si) *

* Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

## Related Literature

For a full list of related documents, visit our website:

- ISL70419SEH product page




SALLEN-KEY LOW PASS FILTER ($f_C$ = 10kHz)

FIGURE 1. TYPICAL APPLICATION

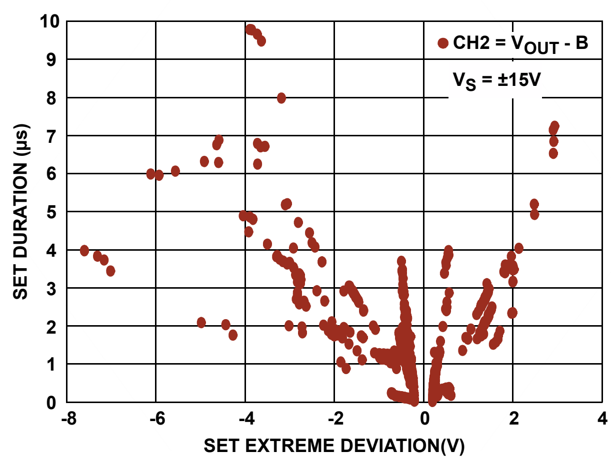



FIGURE 2. SET DEVIATION vs DURATION FOR LET = 60 MeV•$cm^2$/mg

# Ordering Information

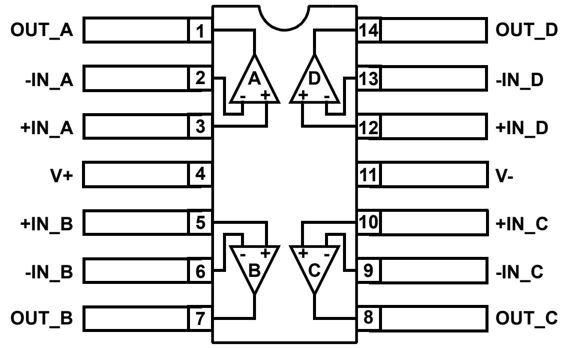
| ORDERING/SMD NUMBER (Note 2) | PART NUMBER (Note 1) | TEMPERATURE RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| 5962F1422601VXC | ISL70419SEHVF | -55 to +125 | 14 Ld Flatpack with EPAD | K14.C |
| N/A | ISL70419SEHF/PROTO (Note 3) | -55 to +125 | 14 Ld Flatpack with EPAD | K14.C |
| 5962F1422601V9AX | ISL70419SEHVX | -55 to +125 | DIE | |
| N/A | ISL70419SEHX/SAMPLE (Note 3) | -55 to +125 | DIE | |
| N/A | ISL70419SEHEV1Z (Note 4) | Evaluation Board | | |

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Evaluation boards use the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

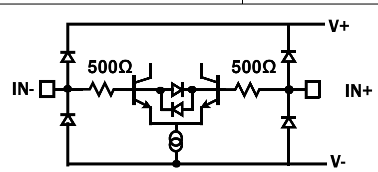
# Pin Configuration

**14 LD FLATPACK**
**TOP VIEW**

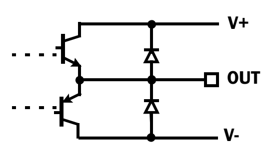



# Pin Descriptions

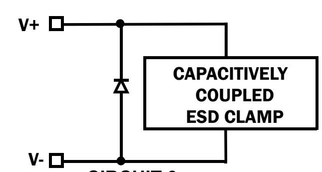
| PIN NUMBER | PIN NAME | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|
| 1 | OUT_A | Circuit 2 | Amplifier A output |
| 2 | -IN_A | Circuit 1 | Amplifier A inverting input |
| 3 | +IN_A | Circuit 1 | Amplifier A non-inverting input |
| 4 | V+ | Circuit 3 | Positive power supply |
| 5 | +IN_B | Circuit 1 | Amplifier B non-inverting input |
| 6 | -IN_B | Circuit 1 | Amplifier B inverting input |
| 7 | OUT_B | Circuit 2 | Amplifier B output |
| 8 | OUT_C | Circuit 2 | Amplifier C output |
| 9 | -IN_C | Circuit 1 | Amplifier C inverting input |
| 10 | +IN_C | Circuit 1 | Amplifier C non-inverting input |
| 11 | V- | Circuit 3 | Negative power supply |
| 12 | +IN_D | Circuit 1 | Amplifier D non-inverting input |
| 13 | -IN_D | Circuit 1 | Amplifier D inverting input |
| 14 | OUT_D | Circuit 2 | Amplifier D output |
|  | EPAD | N/A | EPAD under Package (unbiased, tied to package lid) |



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

## Absolute Maximum Ratings

Maximum Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 42V
Maximum Supply Voltage (LET = 86.4 MeV • cm$^2$/mg). . . . . . . . . . . . . 36V
Maximum Differential Input Current . . . . . . . . . . . . . . . . . . . . . . . . . . 20mA
Maximum Differential Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . 20V
Min/Max Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . V- - 0.5V to V+ + 0.5V
Max/Min Input current for Input Voltage >V+ or <V-. . . . . . . . . . . . . . . . ±20mA
Output Short-Circuit Duration (1 output at a time). . . . . . . . . . . . . . . Indefinite
ESD Rating
 Human Body Model (Tested per MIL-PRF-883 3015.7). . . . . . . . . . . 2kV
 Machine Model (Tested per EIA/JESD22-A115-A) . . . . . . . . . . . . . . 200V
 Charged Device Model (Tested per JESD22-C101D) . . . . . . . . . . . . 750V

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 14 Ld Flatpack (Notes 5, 6). . . . . . . . . . . . . | 35 | 8 |

Maximum Storage Temperature Range . . . . . . . . . . . . . .-65°C to +150°C
Maximum Junction Temperature ($T_{JMAX}$) . . . . . . . . . . . . . . . . . . . . .+150°C

## Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . . . . . . . . . .-55°C to +125°C
Maximum Operating Junction Temperature . . . . . . . . . . . . . . . . . .+150°C
Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . 10V (±5V) to 30V (±15V)

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
6. For $\theta_{JC}$, the "case temp" location is the center of the package underside.

## Electrical Specifications

$V_S$ ± 15V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300rad(Si)/s; or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | | 10 | 85 | µV |
| | | | | | **110** | µV |
| Offset Voltage Drift | $TCV_{OS}$ | Established by characterization not tested | | 0.1 | **1** | µV/°C |
| Input Bias Current | $I_B$ | | -2.5 | 0.08 | 2.5 | nA |
| | | $T_A$ = -55°C to +125°C | -5 | | 5 | nA |
| | | Over high and low dose radiation | -15 | | 15 | nA |
| Input Bias Current Temperature Coefficient | $TCI_B$ | Established by characterization not tested | **-5** | **1** | **5** | pA/°C |
| Input Offset Current | $I_{OS}$ | | -2.5 | 0.08 | 2.5 | nA |
| | | $T_A$ = -55°C to +125°C | -3 | | 3 | nA |
| | | Over high and low dose radiation | -10 | | 10 | nA |
| Input Offset Current Temperature Coefficient | $TCI_{OS}$ | Established by characterization not tested | **-3** | **0.42** | **3** | pA/°C |
| Input Voltage Range | $V_{CM}$ | Established by CMRR test | **-13** | | **13** | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = -13V to +13V | 120 | 145 | | dB |
| | | | **120** | | | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±2.25V to ±20V | 120 | 145 | | dB |
| | | | **120** | | | dB |
| Open-Loop Gain | $A_{VOL}$ | $V_O$ = -13V to +13V, $R_L$ = 10kΩ to ground | 3,000 | 14,000 | | V/mV |
| Output Voltage High | $V_{OH}$ | $R_L$ = 10kΩ to ground | 13.5 | 13.7 | | V |
| | | | **13.2** | | | V |
| | | $R_L$ = 2kΩ to ground | 13.3 | 13.55 | | V |
| | | | **13.0** | | | V |

**Electrical Specifications** $V_S$ ± 15V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300rad(Si)/s; or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| Output Voltage Low | $V_{OL}$ | $R_L$ = 10kΩ to ground | | -13.7 | -13.5 | V |
| | | | | | **-13.2** | V |
| | | $R_L$ = 2kΩ to ground | | -13.55 | -13.3 | V |
| | | | | | **-13.0** | V |
| Supply Current/Amplifier | $I_S$ | | | 0.44 | 0.625 | mA |
| | | | | | **0.75** | mA |
| Short-Circuit Current | $I_{SC}$ | | | 43 | | mA |
| Supply Voltage Range | $V_{SUPPLY}$ | Established by PSRR | **± 2.25** | | **± 20** | V |
| **AC SPECIFICATIONS** | | | | | | |
| Gain Bandwidth Product | GBWP | $A_V$ = 1k, $R_L$ = 2kΩ | | 1.5 | | MHz |
| Voltage Noise $V_{P-P}$ | $e_{nVp-p}$ | 0.1Hz to 10Hz | | 0.25 | | $\mu V_{P-P}$ |
| Voltage Noise Density | $e_n$ | f = 10Hz | | 10 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 100Hz | | 8.2 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 1kHz | | 8 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 10kHz | | 8 | | nV/√Hz |
| Current Noise Density | in | f = 1kHz | | 0.1 | | pA/√Hz |
| Total Harmonic Distortion | THD + N | 1kHz, G = 1, $V_O$ = 3.5$V_{RMS}$, $R_L$ = 2kΩ | | 0.0009 | | % |
| | | 1kHz, G = 1, $V_O$ = 3.5$V_{RMS}$, $R_L$ = 10kΩ | | 0.0005 | | % |
| **TRANSIENT RESPONSE** | | | | | | |
| Slew Rate, $V_{OUT}$ 20% to 80% | SR | $A_V$ = 11, $R_L$ = 2kΩ, $V_O$ = 4$V_{P-P}$ | 0.3 | 0.5 | | V/µs |
| | | | **0.2** | | | V/µs |
| Rise Time 10% to 90% of $V_{OUT}$ | $t_r$, $t_f$, small signal | $A_V$ = 1, $V_{OUT}$ = 50m$V_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | 130 | 450 | ns |
| | | | | | **625** | ns |
| Fall Time 90% to 10% of $V_{OUT}$ | | $A_V$ = 1, $V_{OUT}$ = 50m$V_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | 130 | 600 | ns |
| | | | | | **700** | ns |
| Settling Time to 0.1% 10V Step; 10% to $V_{OUT}$ | $t_s$ | $A_V$ = -1, $V_{OUT}$ = 10$V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 21 | | µs |
| Settling Time to 0.01% 10V Step; 10% to $V_{OUT}$ | | $A_V$ = -1, $V_{OUT}$ = 10$V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 24 | | µs |
| Settling Time to 0.1% 4V Step; 10% to $V_{OUT}$ | | $A_V$ = -1, $V_{OUT}$ = 4$V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 13 | | µs |
| Settling Time to 0.01% 4V Step; 10% to $V_{OUT}$ | | $A_V$ = -1, $V_{OUT}$ = 4$V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 18 | | µs |
| Output Positive Overload Recovery Time | $t_{OL}$ | $A_V$ = -100, $V_{IN}$ = 0.2$V_{P-P}$, $R_L$ = 2kΩ to $V_{CM}$ | | 5.6 | | µs |
| Output Negative Overload Recovery Time | | $A_V$ = -100, $V_{IN}$ = 0.2$V_{P-P}$, $R_L$ = 2kΩ to $V_{CM}$ | | 10.6 | | µs |
| Positive Overshoot | OS+ | $A_V$ = 1, $V_{OUT}$ = 10$V_{P-P}$, $R_f$ = 0Ω $R_L$ = 2kΩ to $V_{CM}$ | | 15 | | % |
| | | | | | **33** | % |
| Negative Overshoot | OS- | $A_V$ = 1, $V_{OUT}$ = 10$V_{P-P}$, $R_f$ = 0Ω $R_L$ = 2kΩ to $V_{CM}$ | | 15 | | % |
| | | | | | **33** | % |

## Electrical Specifications

$V_S$ ± 5V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{OS}$ | | | 10 | 150 | µV |
| | | | | | **250** | µV |
| Offset Voltage Drift | $TCV_{OS}$ | Established by characterization not tested | | 0.1 | **1** | µV/°C |
| Input Bias Current | $I_B$ | | -2.5 | 0.08 | 2.5 | nA |
| | | $T_A$ = -55°C to +125°C | -5 | | 5 | nA |
| | | Over high and low dose radiation | -15 | | 15 | nA |
| Input Bias Current Temperature Coefficient | $TCI_B$ | Established by characterization not tested | **-5** | **1** | **5** | pA/°C |
| Input Offset Current | $I_{OS}$ | | -2.5 | 0.08 | 2.5 | nA |
| | | $T_A$ = -55°C to +125°C | -3 | | 3 | nA |
| | | Over high and low dose radiation | -10 | | 10 | nA |
| Input Offset Current Temperature Coefficient | $TCI_{OS}$ | Established by characterization not tested | **-3** | **0.42** | **3** | pA/°C |
| Input Voltage Range | $V_{CM}$ | Established by CMRR test | **-3** | | **3** | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = -3V to +3V | 120 | 145 | | dB |
| | | | **120** | | | dB |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±2.25V to ±5V | 120 | 145 | | dB |
| | | | **120** | | | dB |
| Open-Loop Gain | $A_{VOL}$ | $V_O$ = -3.0V to +3.0V<br>$R_L$ = 10kΩ to ground | 3000 | 14000 | | V/mV |
| Output Voltage High | $V_{OH}$ | $R_L$ = 10kΩ to ground | 3.5 | 3.7 | | V |
| | | | **3.2** | | | V |
| | | $R_L$ = 2kΩ to ground | 3.3 | 3.55 | | V |
| | | | **3.0** | | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 10kΩ to ground | | -3.7 | -3.5 | V |
| | | | | | **-3.2** | V |
| | | $R_L$ = 2kΩ to ground | | -3.55 | -3.3 | V |
| | | | | | **-3.0** | V |
| Supply Current/Amplifier | $I_S$ | | | 0.44 | 0.625 | mA |
| | | | | | **0.75** | mA |
| Short-Circuit Current | $I_{SC}$ | | | 43 | | mA |
| **AC SPECIFICATIONS** | | | | | | |
| Gain Bandwidth Product | GBWP | $A_V$ = 1k, $R_L$ = 2kΩ | | 1.5 | | MHz |
| Voltage Noise | $e_{np-p}$ | 0.1Hz to 10Hz | | 0.25 | | $µV_{P-P}$ |
| Voltage Noise Density | $e_n$ | f = 10Hz | | 12 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 100Hz | | 8.6 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 1kHz | | 8 | | nV/√Hz |
| Voltage Noise Density | $e_n$ | f = 10kHz | | 8 | | nV/√Hz |
| Current Noise Density | in | f = 1kHz | | 0.1 | | pA/√Hz |

## Electrical Specifications

$V_S$ ± 5V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|---|
| **TRANSIENT RESPONSE** | | | | | | |
| Slew Rate, $V_{OUT}$ 20% to 80% | SR | $A_V$ = 11, $R_L$ = 2kΩ, $V_O$ = $4V_{P-P}$ | | 0.5 | | V/µs |
| Rise Time 10% to 90% of $V_{OUT}$ | $t_r$, $t_f$, small signal | $A_V$ = 1, $V_{OUT}$ = $50mV_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | 130 | | ns |
| Fall Time 90% to 10% of $V_{OUT}$ | | $A_V$ = 1, $V_{OUT}$ = $50mV_{P-P}$, $R_L$ = 10kΩ to $V_{CM}$ | | 130 | | ns |
| Settling Time to 0.1% 4V Step; 10% to $V_{OUT}$ | $t_S$ | $A_V$ = -1, $V_{OUT}$ = $4V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 12 | | µs |
| Settling Time to 0.01% 4V Step; 10% to $V_{OUT}$ | | $A_V$ = -1, $V_{OUT}$ = $4V_{P-P}$, $R_L$ = 5kΩ to $V_{CM}$ | | 19 | | µs |
| Output Positive Overload Recovery Time | $t_{OL}$ | $A_V$ = -100, $V_{IN}$ = $0.2V_{P-P}$ $R_L$ = 2kΩ to $V_{CM}$ | | 7 | | µs |
| Output Negative Overload Recovery Time | | $A_V$ = -100, $V_{IN}$ = $0.2V_{P-P}$ $R_L$ = 2kΩ to $V_{CM}$ | | 5.8 | | µs |
| Positive Overshoot | OS+ | $A_V$ = 1, $V_{OUT}$ = $10V_{P-P}$, $R_f$ = 0Ω $R_L$ = 2kΩ to $V_{CM}$ | | 15 | | % |
| Negative Overshoot | OS- | $A_V$ = 1, $V_{OUT}$ = $10V_{P-P}$, $R_f$ = 0Ω $R_L$ = 2kΩ to $V_{CM}$ | | 15 | | % |

NOTE:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

## Typical Performance Curves

$V_S = \pm15V$, $V_{CM} = 0V$, $R_L$ = Open, $T_A = +25°C$, unless otherwise specified.

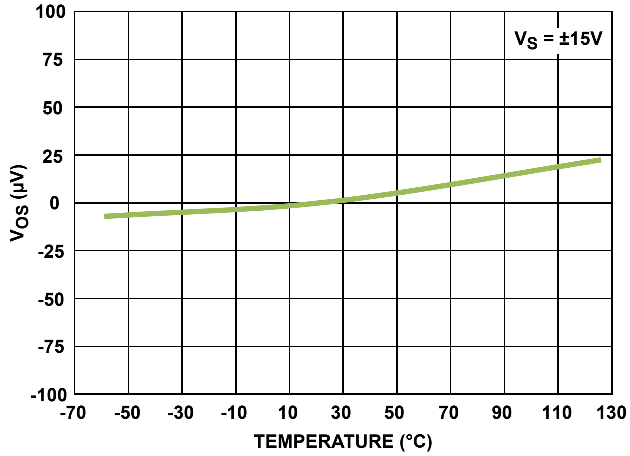



**FIGURE 3. $V_{OS}$ vs TEMPERATURE**

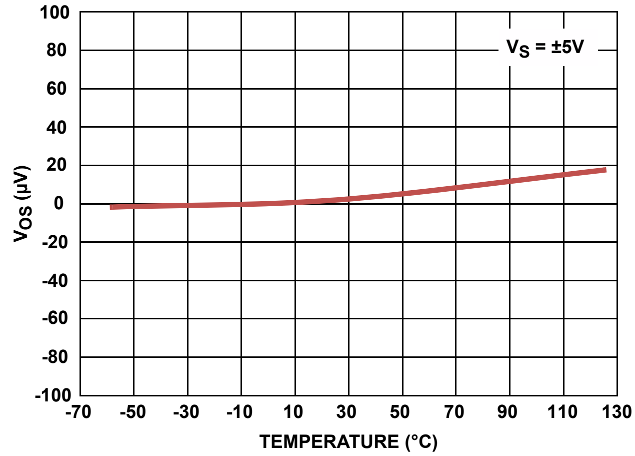



**FIGURE 4. $V_{OS}$ vs TEMPERATURE**

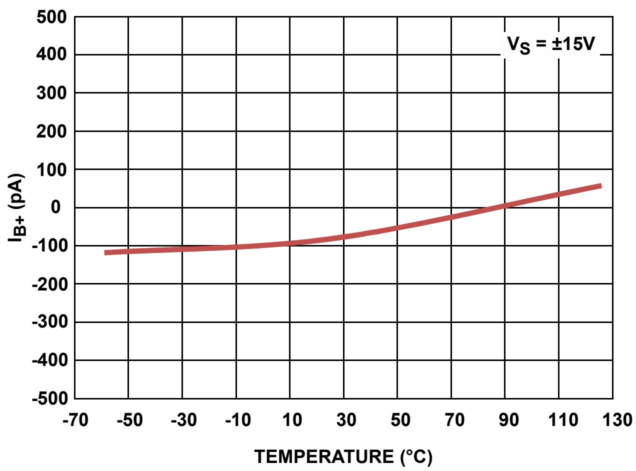



**FIGURE 5. $I_B$+ vs TEMPERATURE**

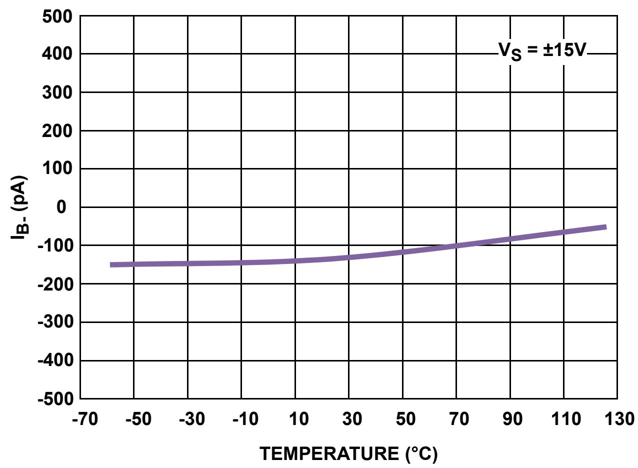



**FIGURE 6. $I_B$- vs TEMPERATURE**

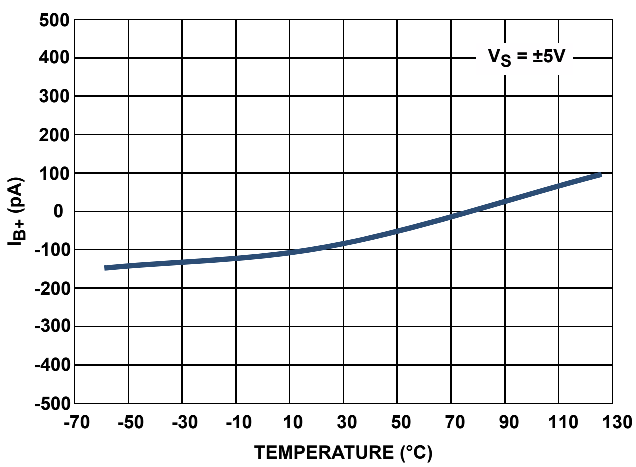



**FIGURE 7. $I_B$+ vs TEMPERATURE**

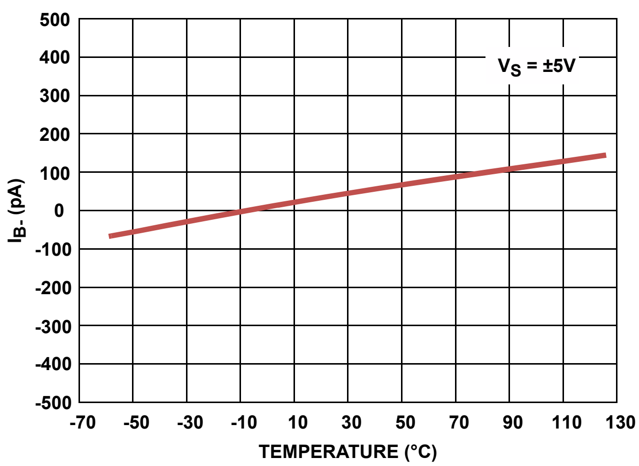



**FIGURE 8. $I_B$- vs TEMPERATURE**

## Typical Performance Curves

$V_S = \pm15V$, $V_{CM} = 0V$, $R_L$ = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

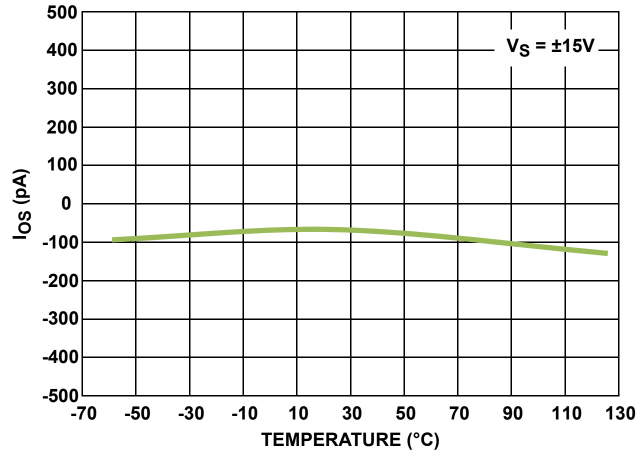



FIGURE 9. $I_{OS}$ vs TEMPERATURE

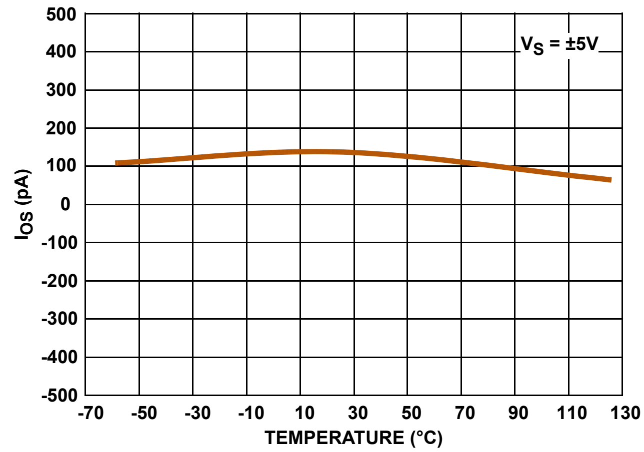



FIGURE 10. $I_{OS}$ vs TEMPERATURE

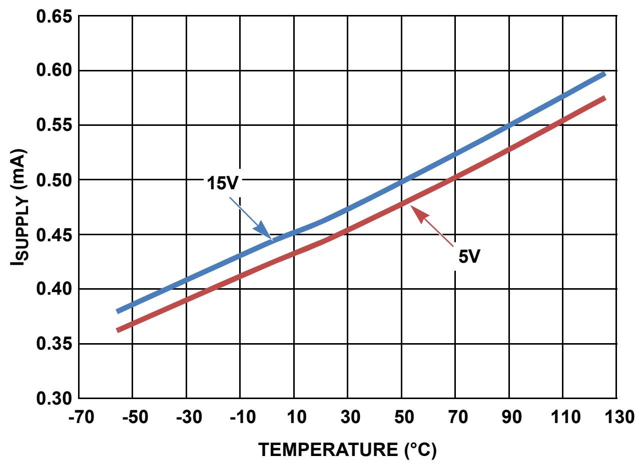



FIGURE 11. SUPPLY CURRENT PER AMP vs TEMPERATURE

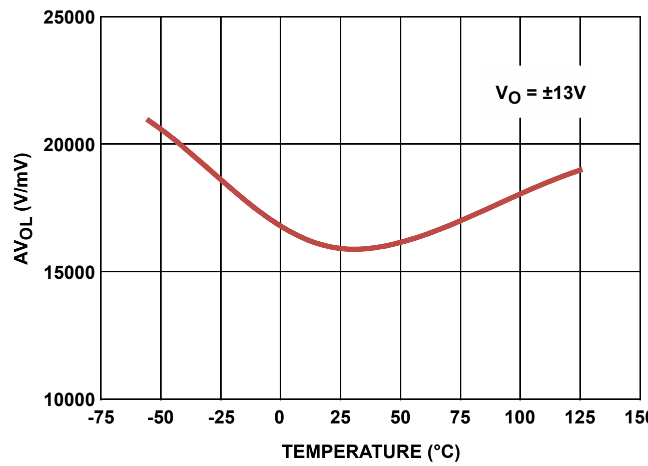



FIGURE 12. $AV_{OL}$ vs TEMPERATURE

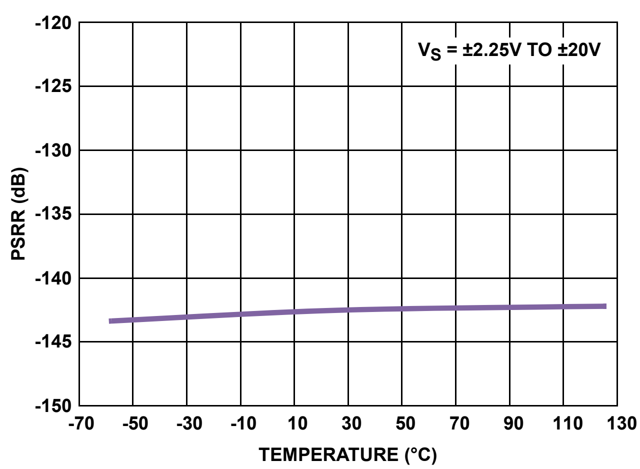



FIGURE 13. PSRR vs TEMPERATURE

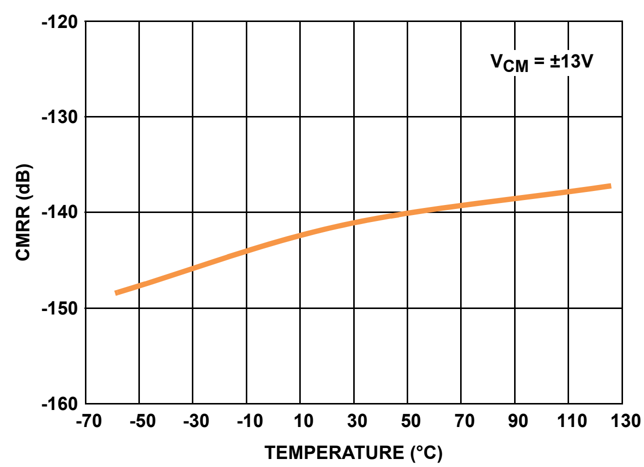



FIGURE 14. CMRR vs TEMPERATURE

## Typical Performance Curves $V_S$ = ±15V, $V_{CM}$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise specified. **(Continued)**

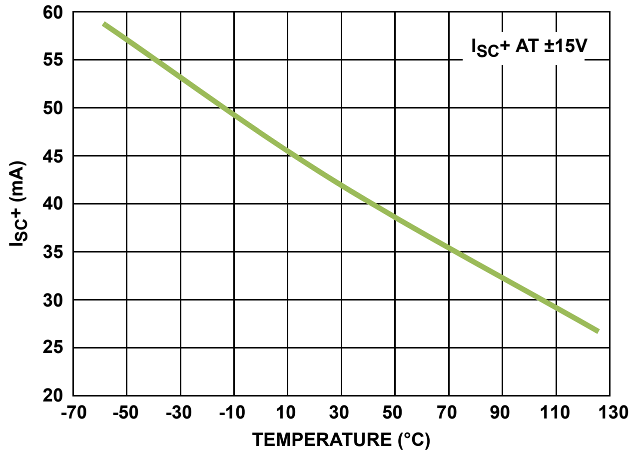



FIGURE 15. SHORT CIRCUIT CURRENT vs TEMPERATURE

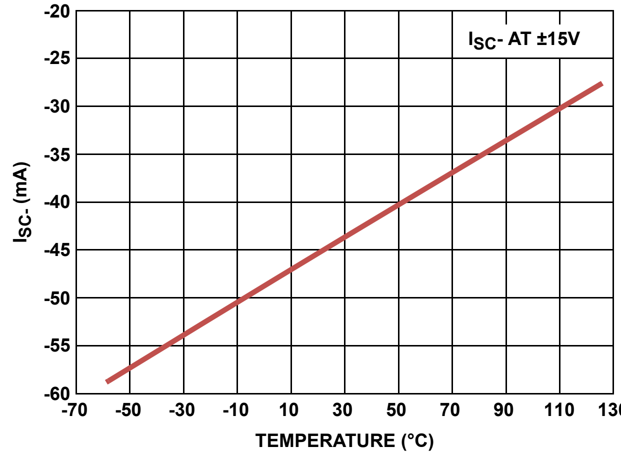



FIGURE 16. SHORT CIRCUIT CURRENT vs TEMPERATURE

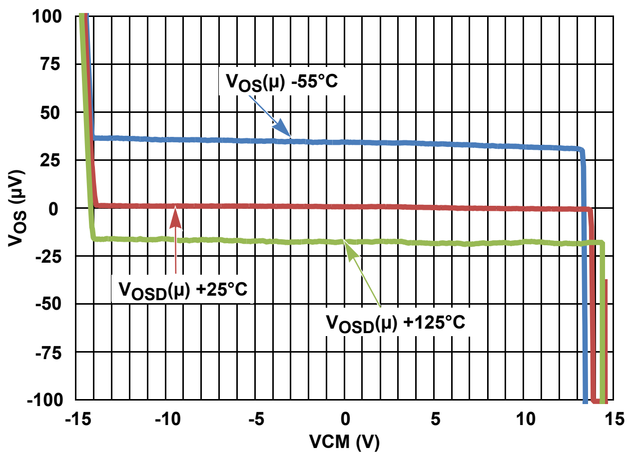



FIGURE 17. INPUT $V_{OS}$ vs INPUT COMMON MODE VOLTAGE, $V_S$ = ±15

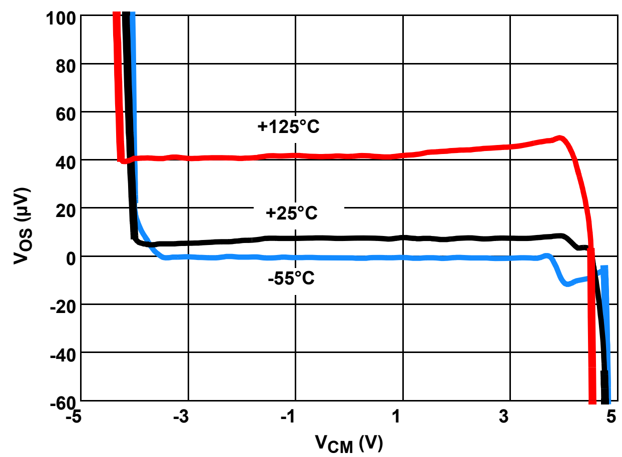



FIGURE 18. INPUT $V_{OS}$ vs INPUT COMMON MODE VOLTAGE, $V_S$ = ±5V

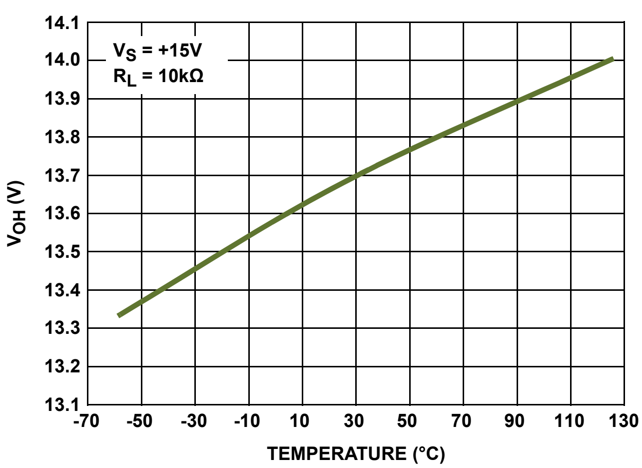



FIGURE 19. $V_{OUT}$ vs TEMPERATURE

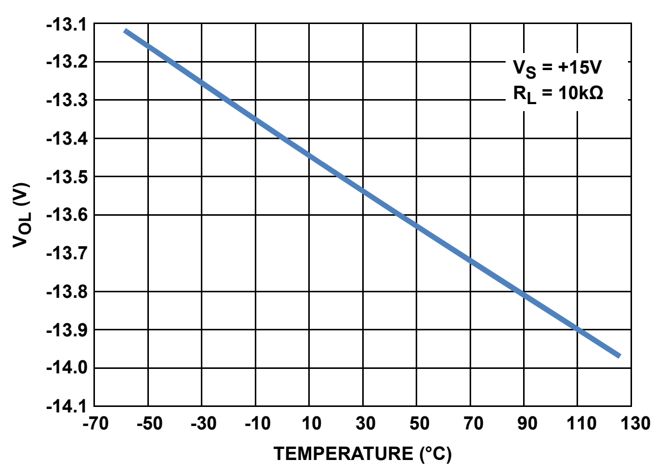



FIGURE 20. $V_{OUT}$ vs TEMPERATURE

## Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, $R_L$ = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

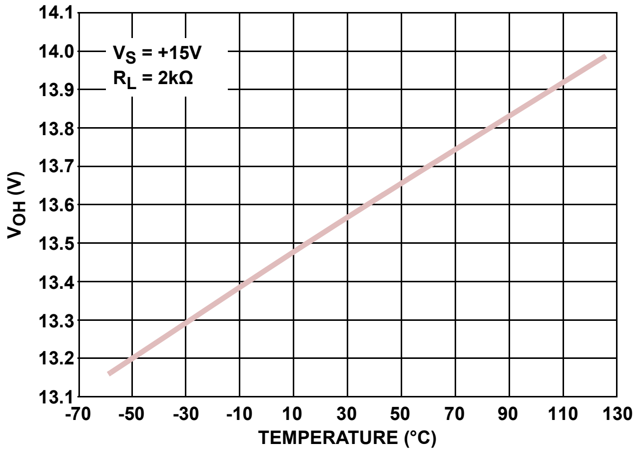



FIGURE 21. $V_{OUT}$ vs TEMPERATURE

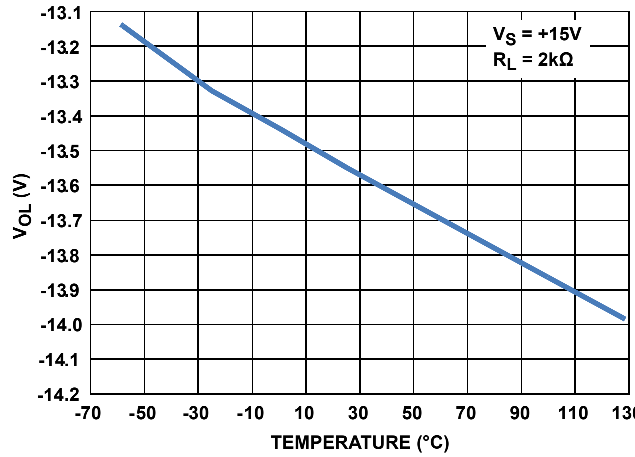



FIGURE 22. $V_{OUT}$ vs TEMPERATURE

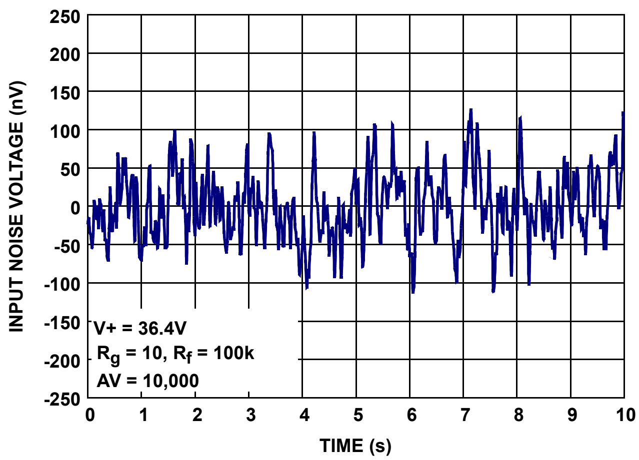



FIGURE 23. INPUT NOISE VOLTAGE 0.1Hz to 10Hz

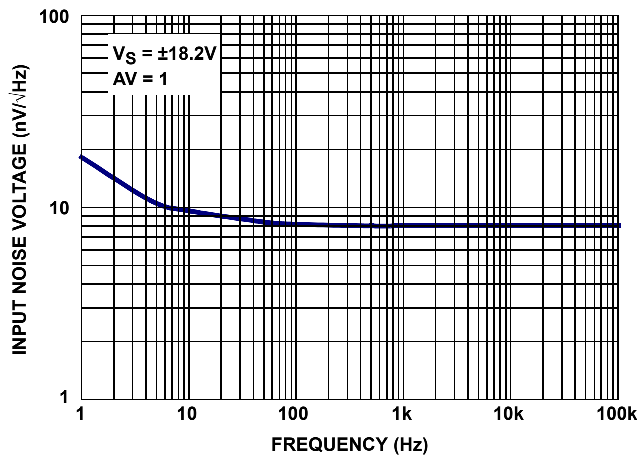



FIGURE 24. INPUT NOISE VOLTAGE SPECTRAL DENSITY

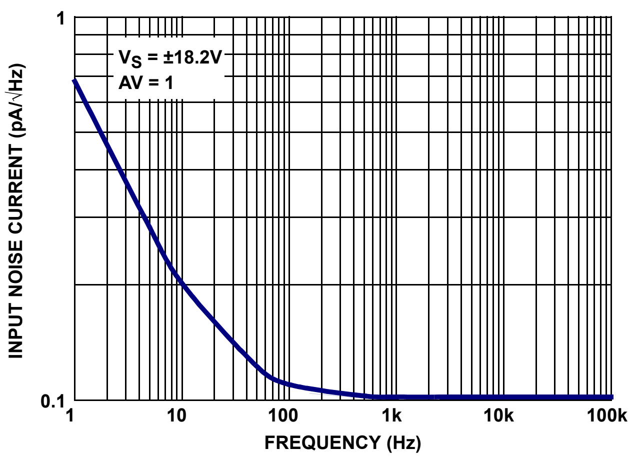



FIGURE 25. INPUT NOISE CURRENT SPECTRAL DENSITY

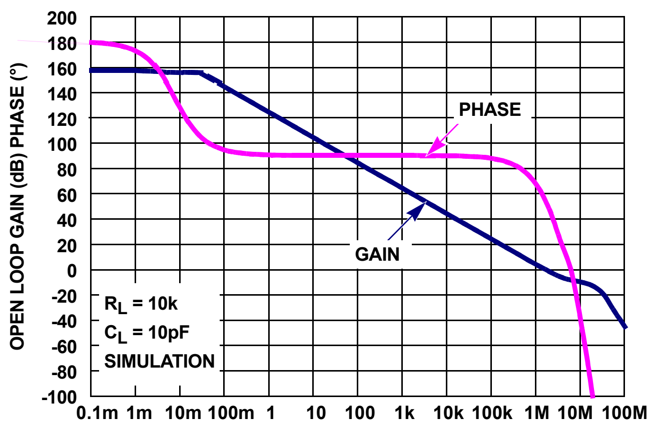



FIGURE 26. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L$ = 10kΩ, $C_L$ = 10pF

## Typical Performance Curves $V_S$ = ±15V, $V_{CM}$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise specified. **(Continued)**

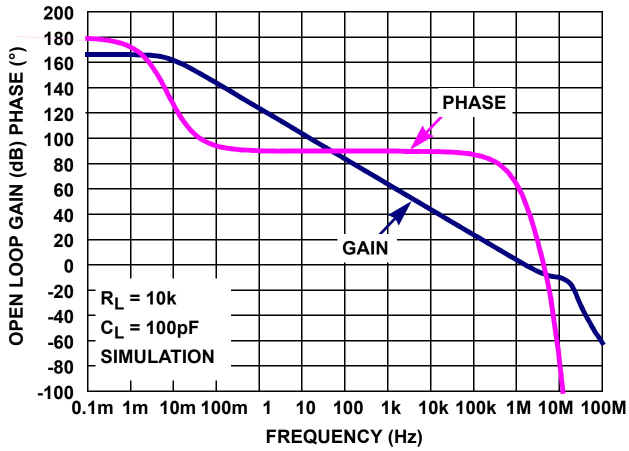



FIGURE 27. OPEN-LOOP GAIN, PHASE vs FREQUENCY, $R_L$ = 10kΩ, $C_L$ = 100pF

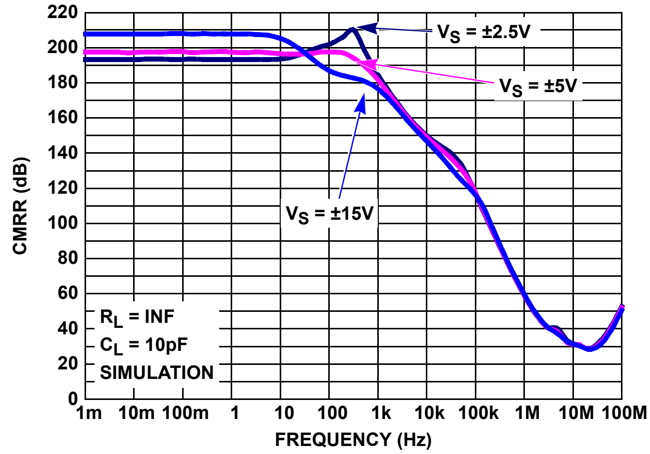



FIGURE 28. CMRR vs FREQUENCY, $V_S$ = ±2.25, ±5V, ±15V

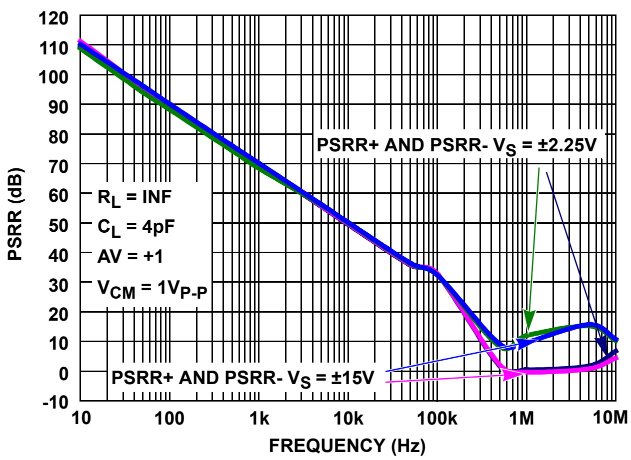



FIGURE 29. PSRR vs FREQUENCY, $V_S$ = ±5V, ±15V

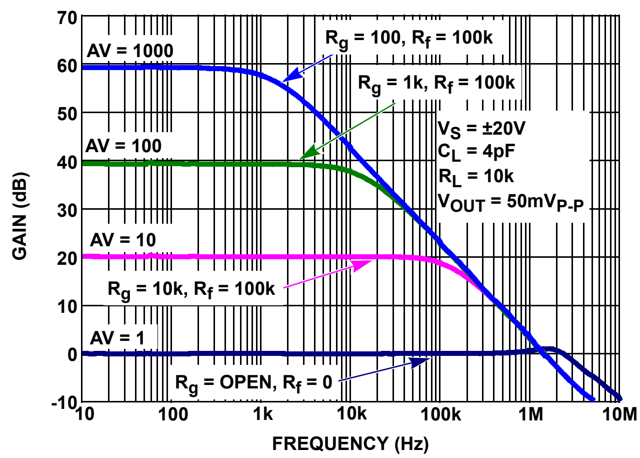



FIGURE 30. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

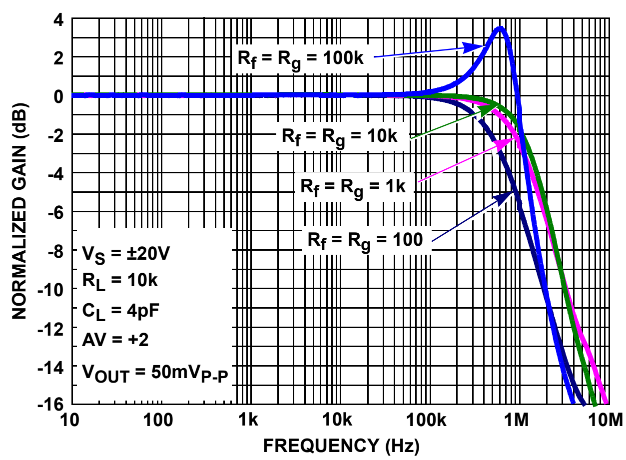



FIGURE 31. FREQUENCY RESPONSE vs FEEDBACK RESISTANCE $R_f/R_g$

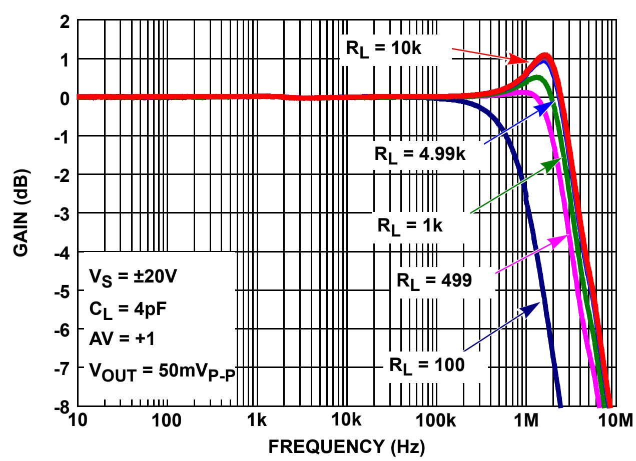



FIGURE 32. GAIN vs FREQUENCY vs $R_L$

## Typical Performance Curves $V_S$ = ±15V, $V_{CM}$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise specified. **(Continued)**

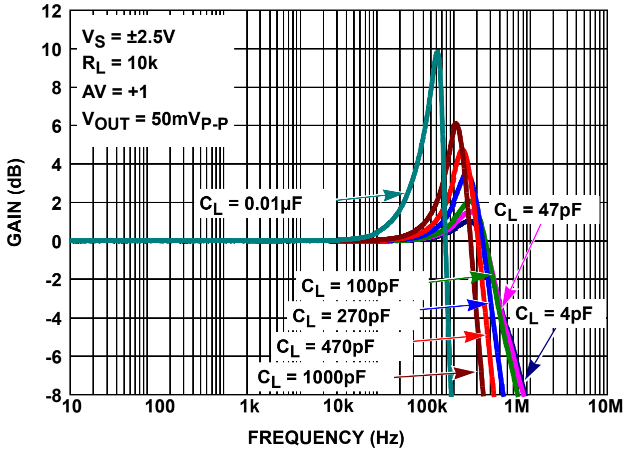



FIGURE 33. GAIN vs FREQUENCY vs $C_L$

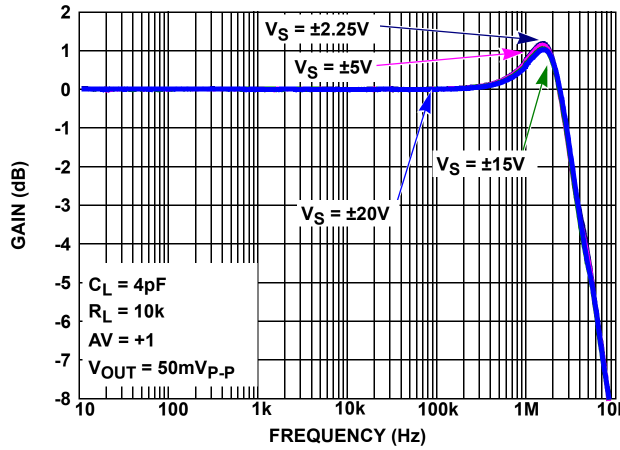



FIGURE 34. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

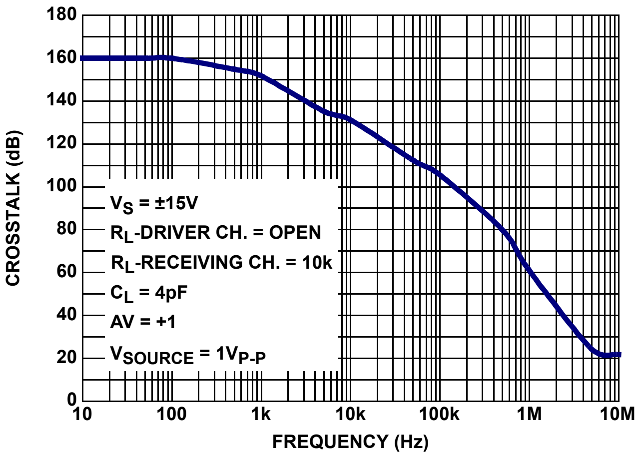



FIGURE 35. CROSSTALK, $V_S$ = ±15V

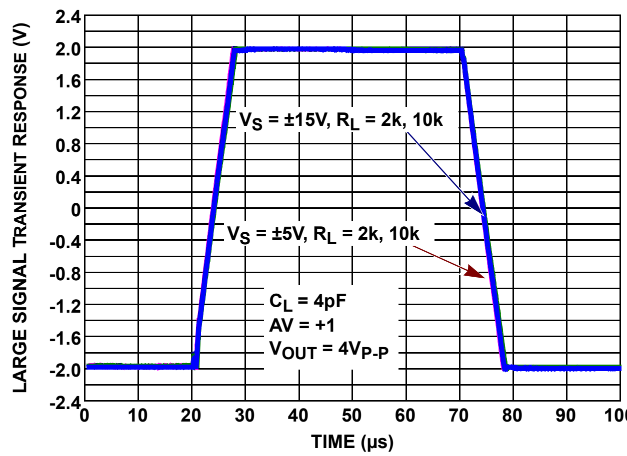



FIGURE 36. LARGE SIGNAL TRANSIENT RESPONSE vs $R_L$ $V_S$ = ±5V, ±15V

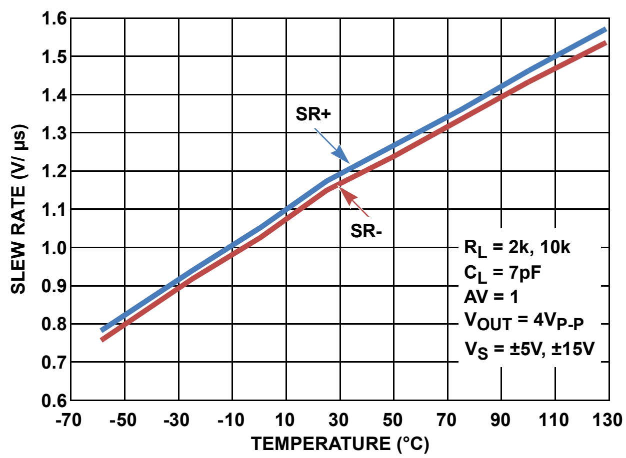



FIGURE 37. SLEW RATE vs TEMPERATURE $V_S$ = ±5V, ±15V

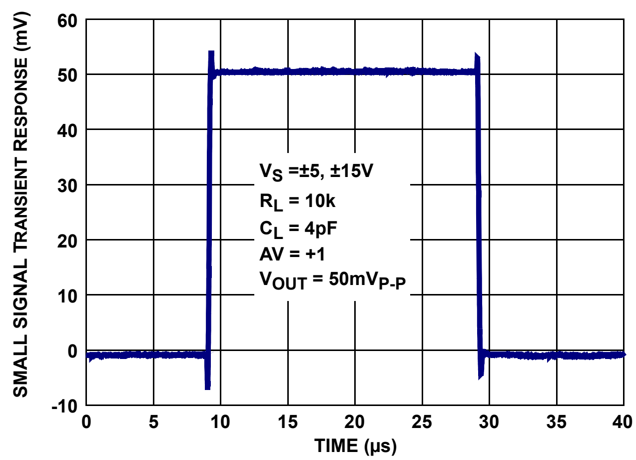



FIGURE 38. SMALL SIGNAL TRANSIENT RESPONSE, $V_S$ = ±5V, ±15V

## Typical Performance Curves
$V_S$ = ±15V, $V_{CM}$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise specified. **(Continued)**

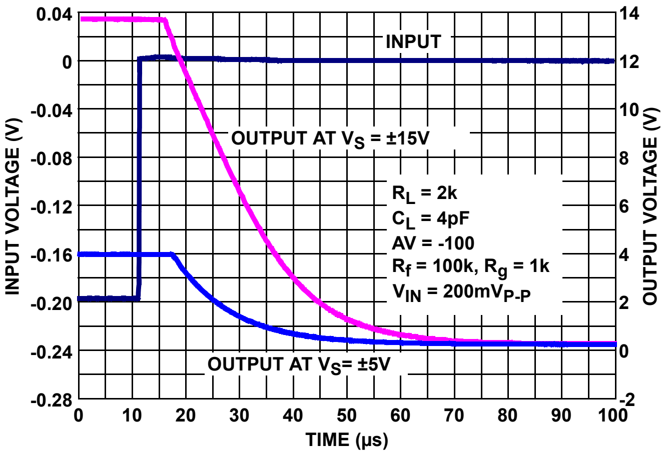



**FIGURE 39. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S$ = ±5V, ±15V**

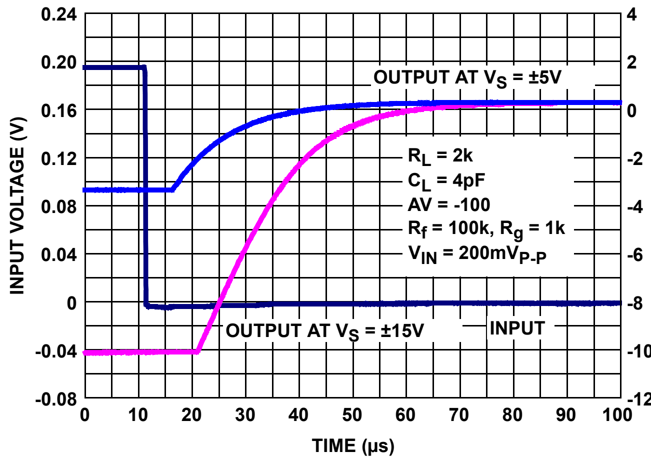



**FIGURE 40. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, $V_S$ = ±5V, ±15V**

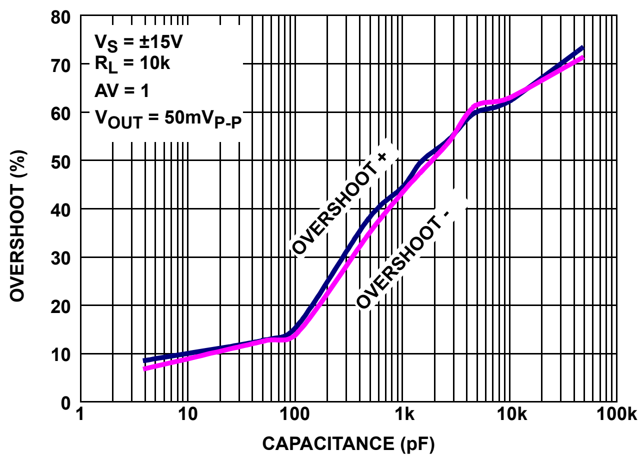



**FIGURE 41. % OVERSHOOT vs LOAD CAPACITANCE, $V_S$ = ±15V**

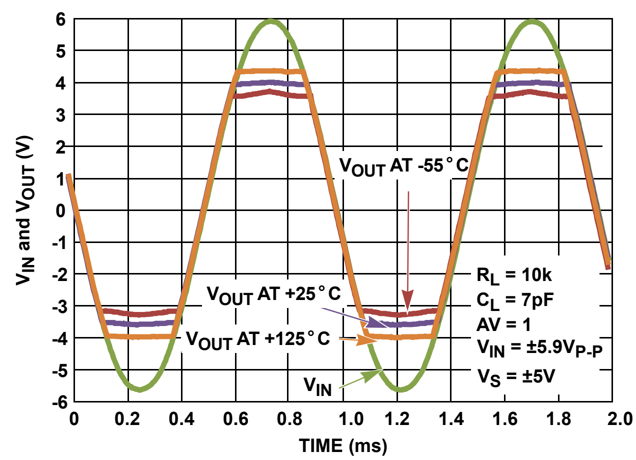



**FIGURE 42. OUTPUT PHASE REVERSAL RESPONSE vs TEMPERATURE**

**Post High Dose Radiation Characteristics** Unless otherwise specified, $V_S \pm 15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a high dose rate of 50 - 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

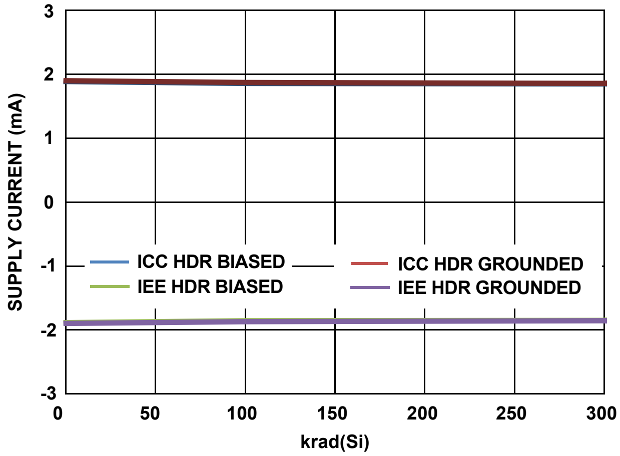



FIGURE 43. SUPPLY CURRENT vs HIGH DOSE RATE RADIATION

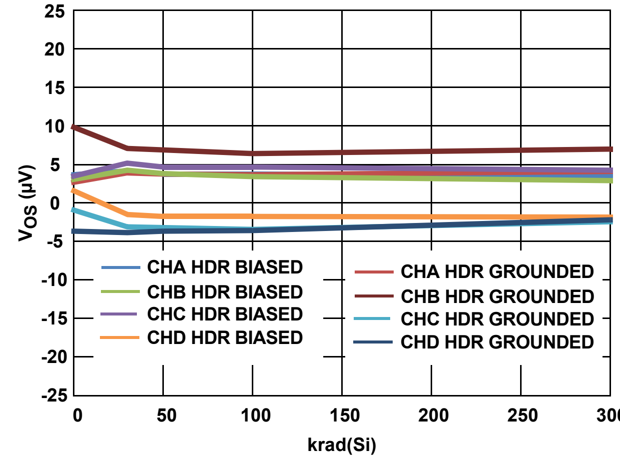



FIGURE 44. $V_{OS}$ vs HIGH DOSE RATE RADIATION

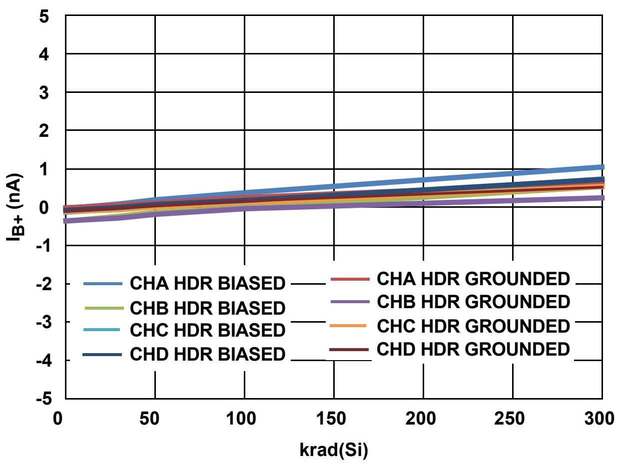



FIGURE 45. $I_B$+ vs HIGH DOSE RATE RADIATION

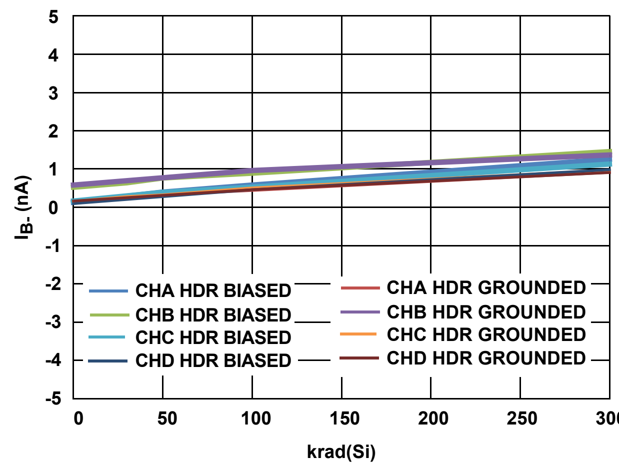



FIGURE 46. $I_B$- vs HIGH DOSE RATE RADIATION

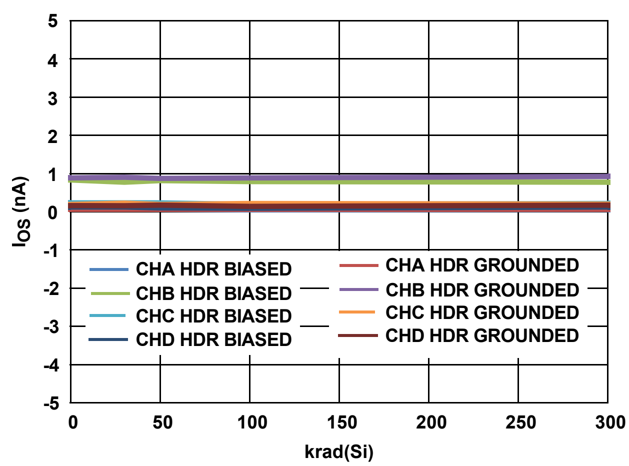



FIGURE 47. $I_{OS}$vs HIGH DOSE RATE RADIATION

**Post Low Dose Radiation Characteristics** Unless otherwise specified, $V_S$ ± 15V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed**

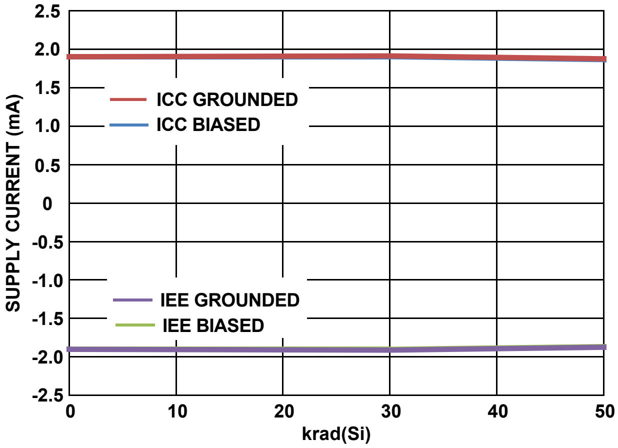



FIGURE 48. SUPPLY CURRENT vs LOW DOSE RATE RADIATION

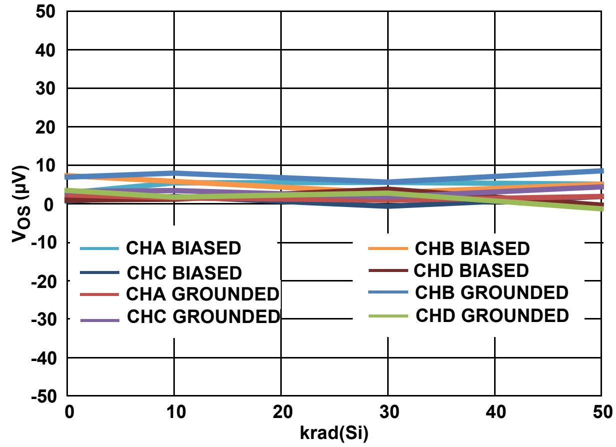



FIGURE 49. $V_{OS}$ vs LOW DOSE RATE RADIATION

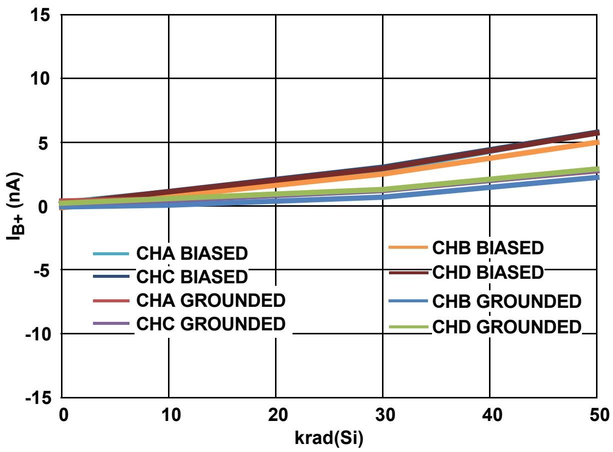



FIGURE 50. $I_{B+}$ vs LOW DOSE RATE RADIATION

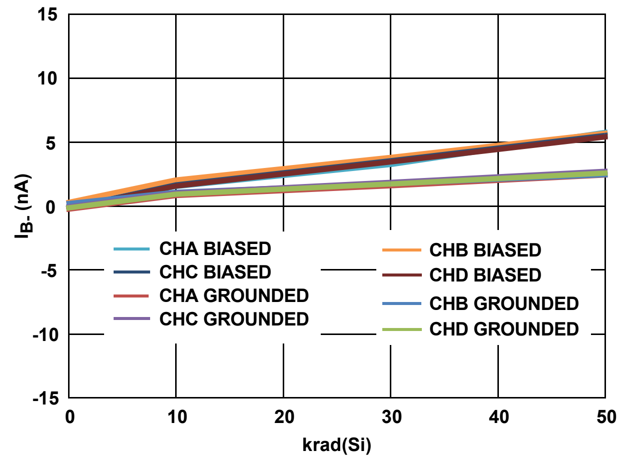



FIGURE 51. $I_{B-}$ vs LOW DOSE RATE RADIATION

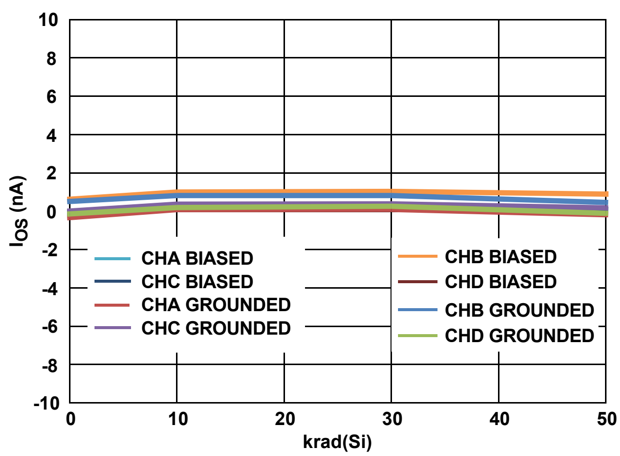



FIGURE 52. $I_{OS}$ vs LOW DOSE RATE RADIATION

# Applications Information

## Functional Description

The ISL70419SEH contains four low noise precision operational amplifiers (op amps). This device is fabricated in a precision 40V complementary bipolar DI process. A super-beta NPN input stage with input bias current cancellation provides low input bias current (180pA typical), low input offset voltage (13µV typical), low input noise voltage (8nV/√Hz), and low 1/f noise corner frequency (~8Hz). The ISL70419SEH also features high open-loop gain (14kV/mV) for excellent CMRR (145dB) and THD+N performance (0.0005% at $3.5V_{RMS}$, 1kHz into 2kΩ). A complementary bipolar output stage enables high capacitive load drive without external compensation.

## Operating Voltage Range

The device is designed to operate over the 4.5V (±2.25V) to 36V (±18V) voltage range and is fully characterized at 10V (±5V) and 30V (±15V). The Power Supply Rejection Ratio typically exceeds 140dB across the full operating voltage range and 120dB minimum across the -55°C to +125°C temperature range. The worst case common-mode input voltage range over-temperature is 2V to each rail. With ±15V supplies, Common-Mode Rejection Ratio (CMRR) performance is typically >130dB over-temperature. The minimum CMRR performance across the -55°C to +125°C temperature range is >120dB for power supply voltages from ±5V (10V) to ±15V (30V).

## Input Performance

The super-beta NPN input pair provides excellent frequency response while maintaining high input precision. High NPN beta (>1000) reduces input bias current while maintaining good frequency response, low input bias current, and low noise. Input bias cancellation circuits provide additional bias current reduction to <5nA and excellent temperature stabilization. Figures 6 through 8 show the high degree of bias current stability at ±5V and ±15V supplies that is maintained across the -55°C to +125°C temperature range. The low bias current TC also produces very low input offset current TC, which reduces DC input offset errors in precision high impedance amplifiers.

The +25°C maximum input offset voltage ($V_{OS}$) is 75µV at ±15V supplies. The input offset voltage temperature coefficient ($V_{OS}TC$) is a maximum of ±1.0µV/°C. The $V_{OS}$ temperature behavior is smooth (Figures 3 through 4), maintaining constant TC across the entire temperature range.

## Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors, and an anti-parallel diode pair across the inputs (Figure 53).

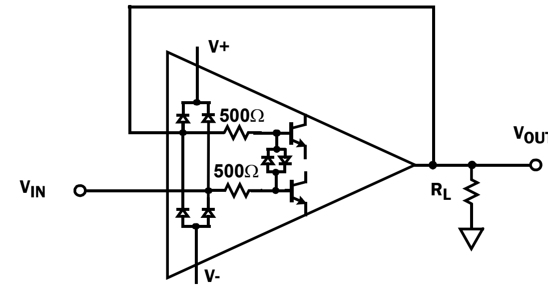



FIGURE 53. INPUT ESD DIODE CURRENT LIMITING- UNITY GAIN

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dV/dT exceeds the 0.5V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes, causing current to flow to the output resulting in severe distortion and possible diode failure.

Figure 36 provides an example of distortion free large signal response using a $4V_{P-P}$ input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (36V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA maximum.

## Output Current Limiting

The output current is internally limited to approximately ±45mA at +25°C and can withstand a short-circuit to either rail if the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the quad operational amplifier. Continuous operation under these conditions may degrade long term reliability. Figures 15 and 16 on page 10 show the current limit variation with temperature.

## Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL70419SEH is immune to output phase reversal, even when the input voltage is 1V beyond the supplies.

## Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)
- $PD_{MAX}$ for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- $T_{MAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of one amplifier
- $V_S$ = Total supply voltage
- $I_{qMAX}$ = Maximum quiescent supply current of one amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application

## Package Characteristics

### Weight of Packaged Device

0.6043 grams (Typical)

### Lid Characteristics

Finish: Gold
Potential: Unbiased; tied to EPAD
Case Isolation to Any Lead: 20 x $10^9$ Ω (min)

## Die Characteristics

### Die Dimensions

2406µm x 2935µm (95mils x 116mils)
Thickness: 483µm ±25µm (19mils ±1 mil)

### Interface Materials

#### GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

#### TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

#### BACKSIDE FINISH

Silicon

#### PROCESS

Dielectrically Isolated Complementary Bipolar - PR40

### ASSEMBLY RELATED INFORMATION

#### SUBSTRATE POTENTIAL

Floating

### ADDITIONAL INFORMATION

#### WORST CASE CURRENT DENSITY

< 2 x $10^5$ A/cm$^2$

## Metallization Mask Layout

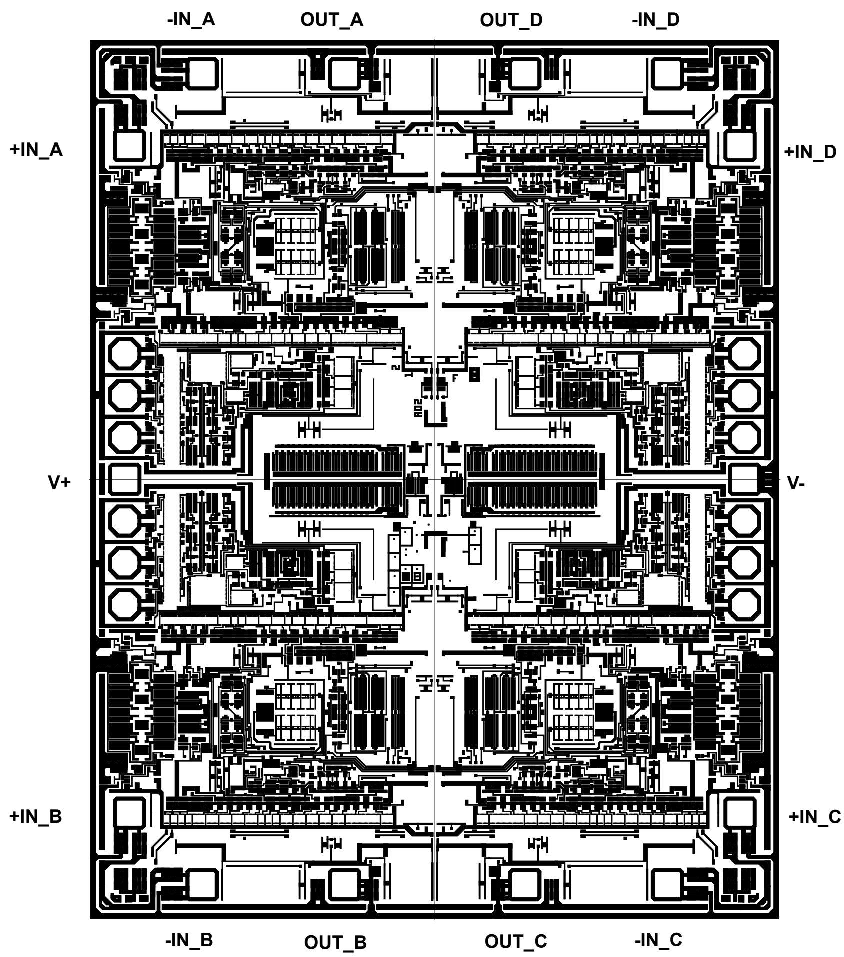


TABLE 1. DIE LAYOUT X-Y COORDINATES

| PAD NAME | PAD NUMBER | X (µm) | Y (µm) | dX (µm) | dY (µm) | BOND WIRES PER PAD |
|---|---|---|---|---|---|---|
| OUT_A | 3 | -445.5 | 1308.5 | 70 | 70 | 1 |
| -IN_A | 4 | -815 | 1308.5 | 70 | 70 | 1 |
| +IN_A | 5 | -1040.5 | 1092 | 70 | 70 | 1 |
| V+ | 9 | -1044 | 0 | 70 | 70 | 1 |
| +IN_B | 13 | -1040.5 | -1092 | 70 | 70 | 1 |
| -IN_B | 14 | -815 | -1308.5 | 70 | 70 | 1 |
| OUT_B | 15 | -445.5 | -1308.5 | 70 | 70 | 1 |
| OUT_C | 16 | 445.5 | -1308.5 | 70 | 70 | 1 |
| -IN_C | 17 | 815 | -1308.5 | 70 | 70 | 1 |
| +IN_C | 18 | 1040.5 | -1092 | 70 | 70 | 1 |
| V- | 22 | 1044 | 0 | 70 | 70 | 1 |
| +IN_D | 26 | 1040.5 | 1092 | 70 | 70 | 1 |
| -IN_D | 1 | 815 | 1308.5 | 70 | 70 | 1 |
| OUT_D | 2 | 445.5 | 1308.5 | 70 | 70 | 1 |

NOTE:

8. Origin of coordinates is the center of die.

## Revision History

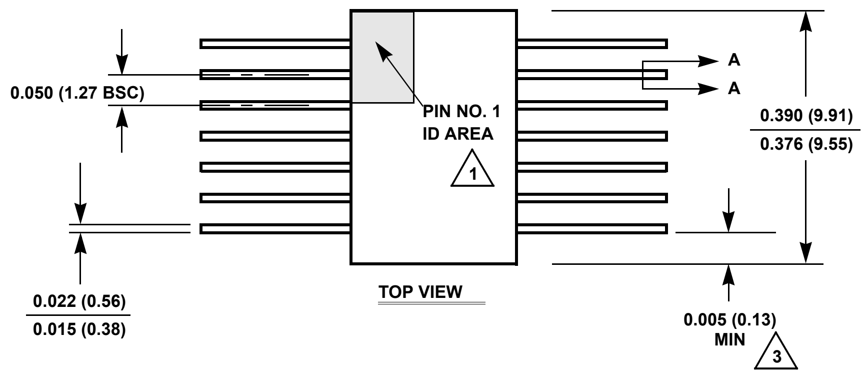
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

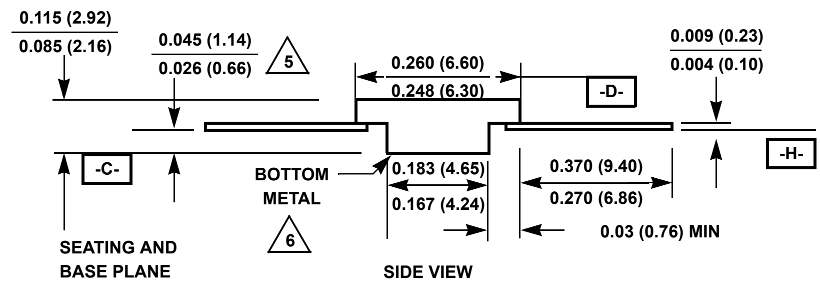
| DATE | REVISION | CHANGE |
|---|---|---|
| Oct 15, 2018 | FN8653.2 | Updated Related Literature section.<br>Updated Ordering Information table.<br>Added Notes 3 and 4.<br>Removed Pb-Free Reflow reference as it is not applicable to this type of package.<br>Removed About Intersil section.<br>Updated disclaimer and moved to end of document. |
| Jul 11, 2014 | FN8653.1 | Modified in Features on page 1<br>SEL/SEB $LET_{TH}$ (VS = ±36V). . . . . . . . . 86.4 MeV•$cm^2$/mg<br>to<br>SEB $LET_{TH}$ (VS = ±18V). . . . . . . . . 86.4 MeV•$cm^2$/mg<br><br>Added in Features on page 1<br>"SEL Immune (SOI Process)"<br>under in the radiation environment section |
| Jun 24, 2014 | FN8653.0 | Initial Release |

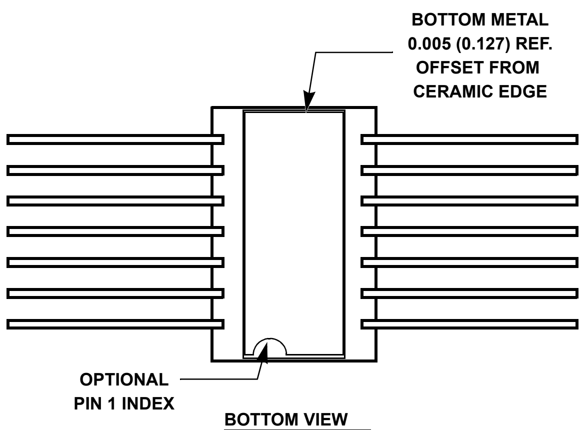
# Package Outline Drawing

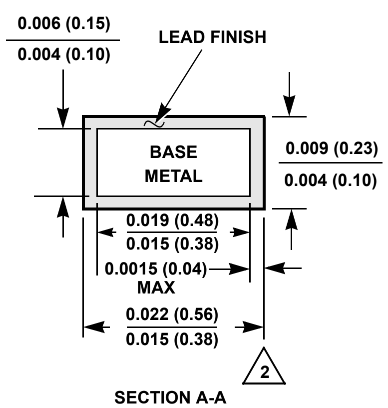
For the most recent package outline drawing, see K14.C.

K14.C
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 0, 9/12




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Measure dimension at all four corners.
4. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
5. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
6. The bottom of the package is a solderable metal surface.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: INCH (mm). Controlling dimension: INCH.

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