ISL71091SEH10

10V Radiation Hardened Ultra Low Noise, Precision Voltage Reference

FN8633
Rev 2.00
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The ISL71091SEH10 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 12V to 30V. It uses Intersil's advanced bipolar technology to achieve 14.8µV_{P-P} 0.1Hz to 10Hz noise with an initial voltage accuracy of 0.05%.

The ISL71091SEH10 offers a 10.0V output voltage option with 6ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld flatpack package.

The ISL71091SEH10 is ideal for high-end instrumentation, data acquisition and processing applications requiring high DC precision where low noise performance is critical.

Applications

- Precision voltage sources for data acquisition system for space application
- Strain and pressure gauge for space applications
- Radiation hardened PWM requiring precision outputs

Related Literature

- AN1906, "ISL71091SEHXXEV1Z User's Guide"
- AN1938, "Single Event Effects (SEE) Testing of the ISL71091SEHxx Precision Voltage References Family"
- AN1939, "Total Dose Testing of the ISL71091SEHxx Precision Voltage Reference"

Features

- **Reference output voltage . . . . . 10.0V ±0.05%**
- **Accuracy over temperature . . . . . ±0.15%**
- **Accuracy over radiation . . . . . ±0.25%**
- **Output voltage noise . . . . . 14.8µV_{P-P} typical (0.1Hz to 10Hz)**
- Supply current . . . . . 300µA (typical)
- V_{OS} temperature coefficient . . . . . 6ppm/°C maximum
- Output current capability 10mA/-5mA
- Line regulation . . . . . 5ppm/V maximum
- Load regulation (sourcing) . . . . . 15ppm/mA maximum
- Operating temperature range. . . . . -55°C to +125°C
- **Radiation environment**
  - **High dose rate (50 to 300rad(Si)/s) . . . . . 100krad(Si)**
  - **Low dose rate (0.01rad(Si)/s) . . . . . 100krad(Si)***
  - **SEL/SEB free (V_{CC} = 36V) . . . . . 86MeV•cm^2/mg**

*Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

- Electrically screened to SMD 5962-14208

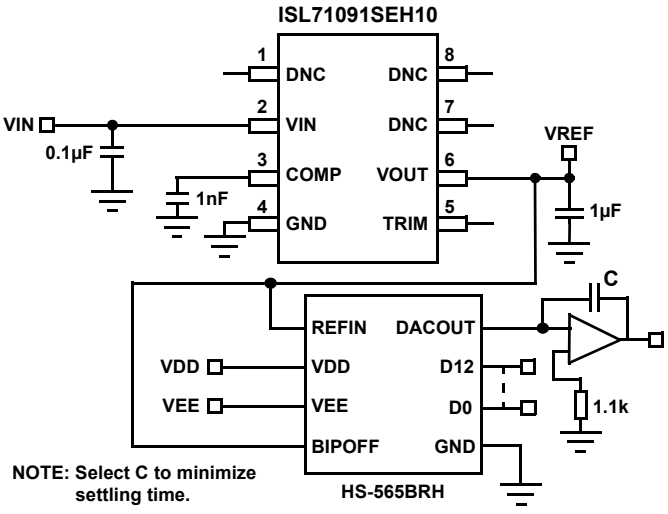


FIGURE 1. ISL71091SEH10 TYPICAL APPLICATION DIAGRAM

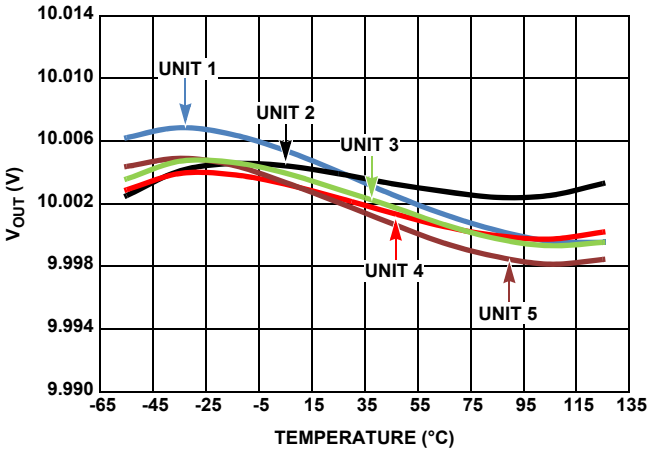


FIGURE 2. V_{OUT} vs TEMPERATURE

Ordering Information

ORDERING NUMBER (Notes 1, 2)	PART NUMBER	V_{OUT} OPTION (Note 3) (V)	GRADE (%)	TEMPCO (ppm/°C)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R1420804VXC	ISL71091SEHVF10	10	0.05	6	-55 to +125	8 Ld Flatpack	K8.A
5962R1420804V9A	ISL71091SEHVX10	10	0.05	6	-55 to +125	Die	
ISL71091SEHF10/PROTO	ISL71091SEHF10/PROTO	10	0.05	6	-55 to +125	8 Ld Flatpack	K8.A
ISL71091SEHX10SAMPLE	ISL71091SEHX10SAMPLE	10	0.05	6	-55 to +125	Die	
ISL71091SEH10EV1Z	Evaluation Board						

NOTES:

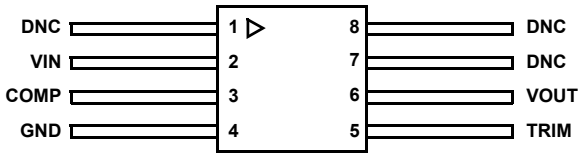
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.
3. For alternate V_{OUT} options, visit the ISL71090SEH and ISL71091SEH family pages.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART	V_{OUT} (V)	TEMPCO (ppm/°C)	OUTPUT VOLTAGE NOISE (μV_{P-P})	LOAD REGULATION (ppm/mA)
ISL71091SEH20	2.048	6	3.8	40
ISL71091SEH33	3.3	6	5.2	25
ISL71091SEH40	4.096	6	6.2	20
ISL71091SEH10	10	6	14.8	15

Pin Configuration

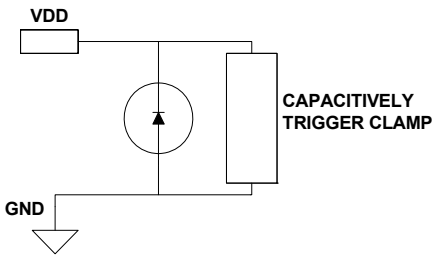
ISL71091SEH10
(8 LD FLATPACK)
TOP VIEW



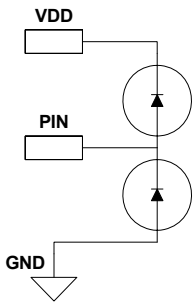
NOTE: The ESD triangular mark is indicative of pin #1. It is a part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

Pin Descriptions

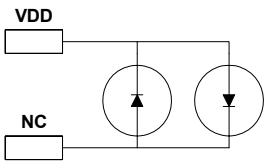
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection.
3	COMP	2	Compensation and noise reduction capacitor.
4	GND	1	Ground connection. Also connected to the lid.
5	TRIM	2	Voltage reference trim input.
6	VOUT	2	Voltage reference output.



ESD CIRCUIT 1



ESD CIRCUIT 2



ESD CIRCUIT 3

Functional Block Diagram

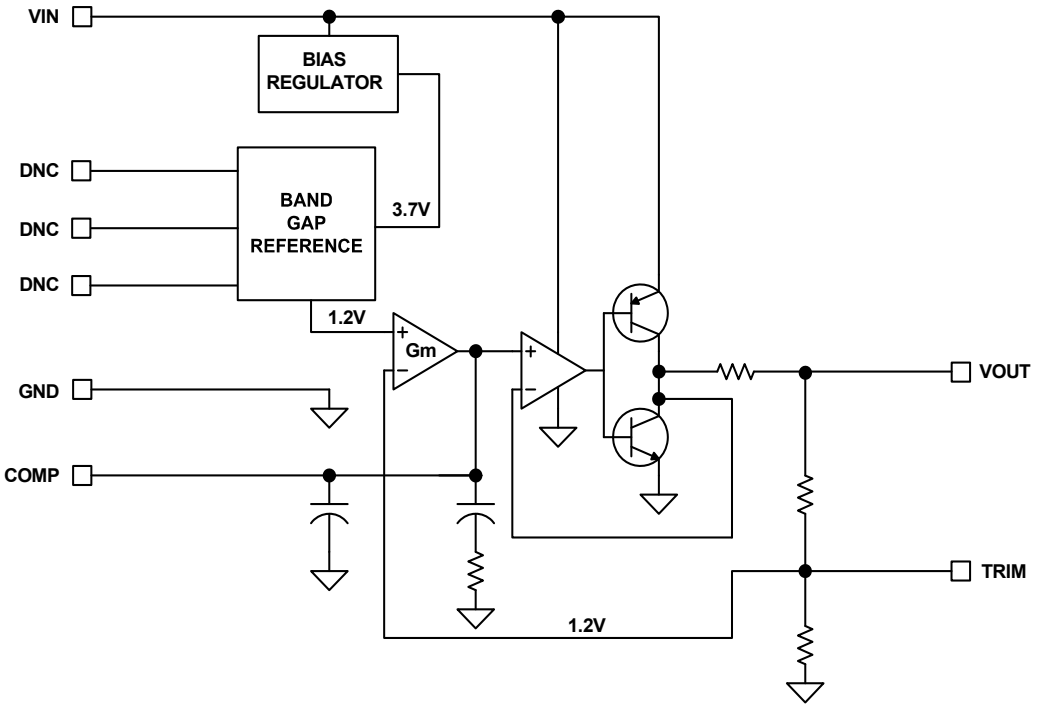


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Typical Trim Application Diagram

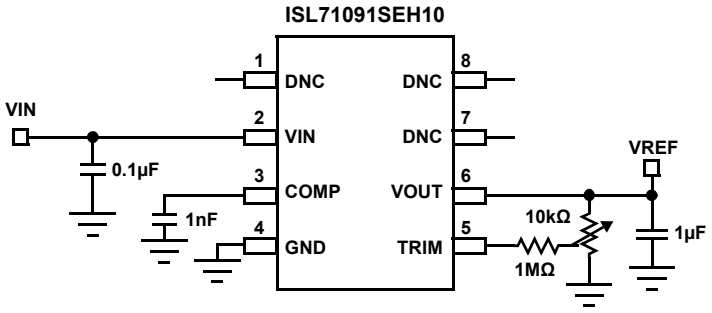


FIGURE 4. TYPICAL TRIM APPLICATION DIAGRAM

Absolute Maximum Ratings

Maximum Voltage
- VIN to GND ..... -0.5V to +40V
- VIN to GND at an LET = 86MeV • cm^2/mg ..... -0.5V to +36V
- VOUT to GND (10s) ..... -0.5V to V_{OUT} + 0.5V

Voltage on any Pin to Ground ..... -0.5V to +V_{OUT} + 0.5V
Voltage on DNC Pins ..... No connections permitted to these pins
ESD Ratings
- Human Body Model (Tested per MIL-PRF-883 3015.7) 2kV
- Machine Model (Tested per JESD22-A115-A) 200V
- Charged Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 4, 5)	135	11

Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) ..... +150°C

Recommended Operating Conditions

Input Voltage Range ..... +12V to +30V
Ambient Operating Temperature Range ..... -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.

Electrical Specifications for Flatpack

V_{IN} = 15V, I_{OUT} = 0mA, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OUT}	Output Voltage			10.0		V
V_{OA}	V_{OUT} Accuracy at T_A = +25°C	V_{OUT} = 10.0V, (Note 7)	-0.05		+0.05	%
V_{OA}	V_{OUT} Accuracy at T_A = -55°C to +125°C	V_{OUT} = 10.0V, (Note 7)	**-0.15**		**+0.15**	%
V_{OA}	V_{OUT} Accuracy at T_A = +25°C, Post Radiation	V_{OUT} = 10.0V, (Note 7)	-0.25		+0.25	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 8)				**6**	ppm/°C
V_{IN}	Input Voltage Range	V_{OUT} = 10.0V	**12**		**30**	V
I_{IN}	Supply Current			0.3	**0.5**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12V to 30V, V_{OUT} = 10.0V		0.3	**5**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 10mA		11	**15**	ppm/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA		25	**40**	ppm/mA
V_D	Dropout Voltage (Note 9)	I_{OUT} = 10mA		1.1	**1.6**	V
I_{SC+}	Short-Circuit Current	T_A = +25°C, V_{OUT} tied to GND		55		mA
I_{SC-}	Short-Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-61		mA
t_R	Turn-On Settling Time	90% of final value, C_L = 1.0µF, C_C = 1000pF		768		µs
PSRR	Ripple Rejection	f = 120Hz		80		dB
$e_N V_{P-P}$	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz, V_{OUT} = 10.0V		14.8		μV_{P-P}
$e_N V_{RMS}$	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz, V_{OUT} = 10.0V		14.7		μV_{RMS}
e_N	Noise Density	f = 1kHz, V_{OUT} = 10.0V		420		$nV/\sqrt{Hz}$
$\Delta V_{OUT}/\Delta t$	Long Term Stability	T_A = +25°C, 1000 hours		20		ppm

Electrical Specifications for Die

V_{IN} = 15V, I_{OUT} = 0, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. Specifications over temperature are guaranteed but not production tested on die.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OUT}	Output Voltage			10.0		V
V_{OA}	V_{OUT} Accuracy at T_A = +25°C	V_{OUT} = 10.0V (Note 10)	-0.05		+0.05	%
V_{OA}	V_{OUT} Accuracy at T_A = -55°C to +125°C	V_{OUT} = 10.0V (Note 10)	**-0.15**		**+0.15**	%
V_{OA}	V_{OUT} Accuracy at T_A = +25°C, Post Radiation	V_{OUT} = 10.0V (Note 10)	-0.25		+0.25	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 8)				**6**	ppm/°C
V_{IN}	Input Voltage Range	V_{OUT} = 10.0V	**12**		**30**	V
I_{IN}	Supply Current			0.3	**0.5**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12V to 30V		0.3	**5**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 10mA		11	**15**	ppm/mA
		Sinking: -5mA ≤ I_{OUT} ≤ 0mA		25	**40**	ppm/mA
V_D	Dropout Voltage (Note 9)	I_{OUT} = 10mA		1.1	**1.6**	V

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. Post-reflow drift for the ISL71091SEH10 devices can exceed 100µV based on experimental results with devices on FR4 double-sided boards. The engineer must take this into account when considering the reference voltage after assembly.
8. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in V_{OUT} is divided by the temperature range; in this case, -55°C to +125°C = +180°C.
9. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.
10. The V_{OUT} accuracy is based on die mount with Silver Glass die attach material such as “QMI 2569” or equivalent in a package with an Alumina ceramic substrate.

Total Dose Radiation Characteristics

This data is typical mean test data post total dose radiation exposure at both low dose rate (LDR) of <10mrad(Si)/s to 50krads and at a high dose rate (HDR) of 50 to 300rad(Si)/s to 150krads. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. LDR data to 150krads will be added when available. V_{IN} = 15V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF unless otherwise specified.

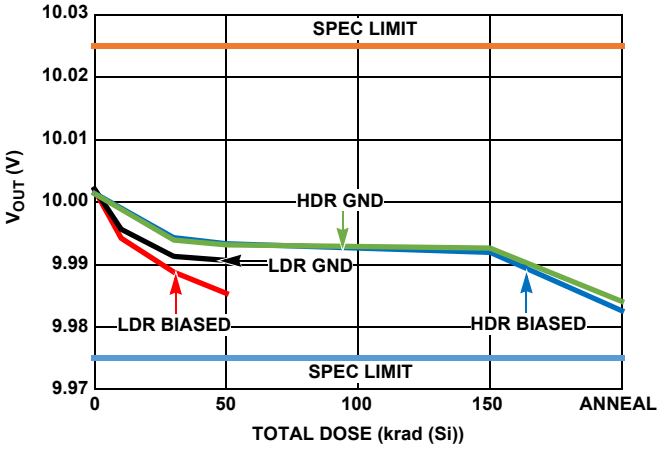


FIGURE 5. V_{OUT} ACCURACY SHIFT

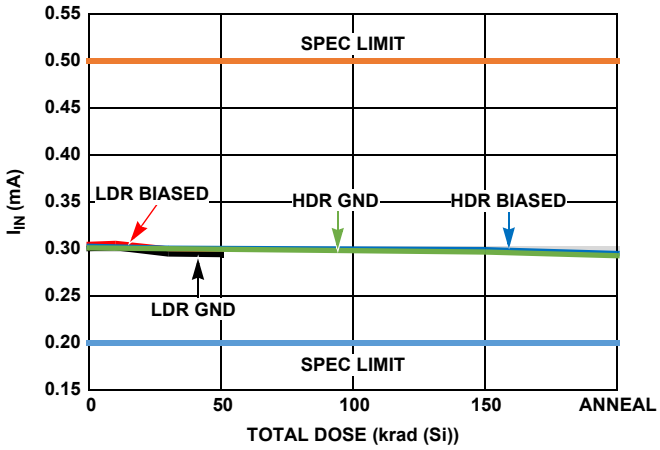


FIGURE 6. SUPPLY CURRENT SHIFT

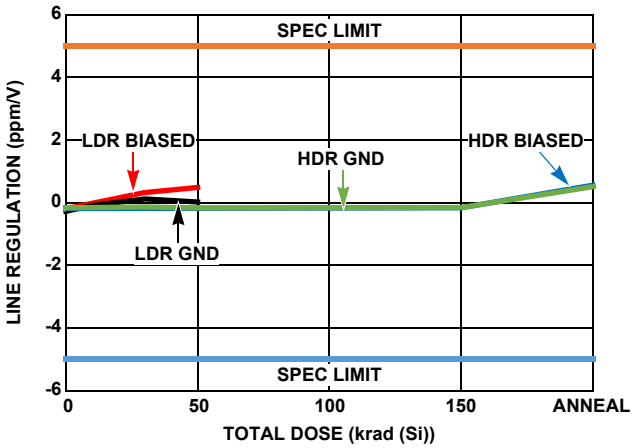


FIGURE 7. LINE REGULATION SHIFT

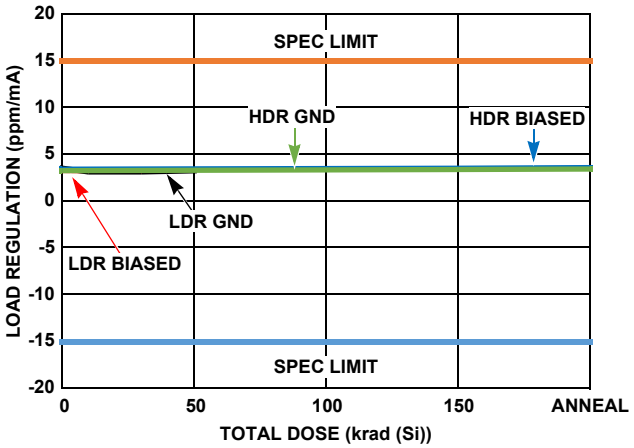


FIGURE 8. LOAD REGULATION (SOURCING) SHIFT

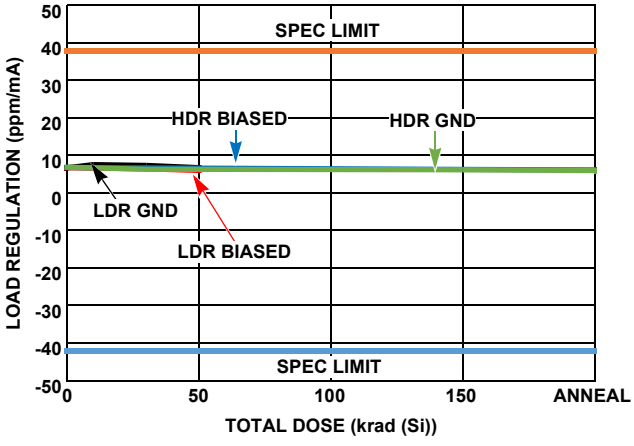


FIGURE 9. LOAD REGULATION (SINKING) SHIFT

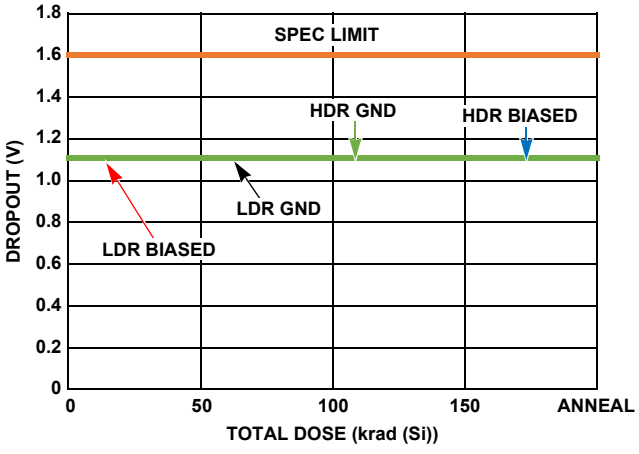


FIGURE 10. DROPOUT SHIFT

Typical Performance Curves

V_{IN} = 15V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified.

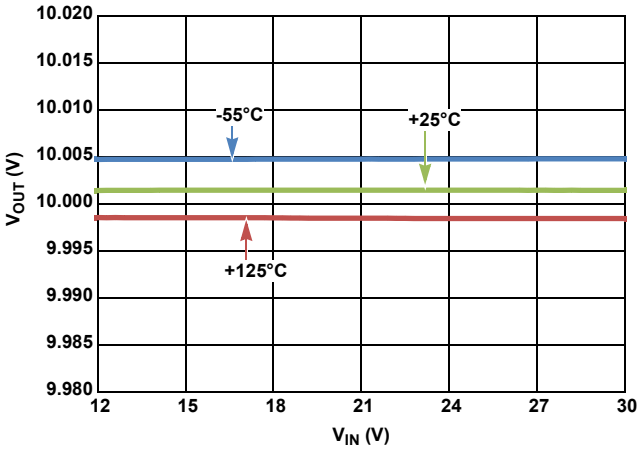


FIGURE 11. LINE REGULATION vs V_{OUT} (V) OVER TEMPERATURE

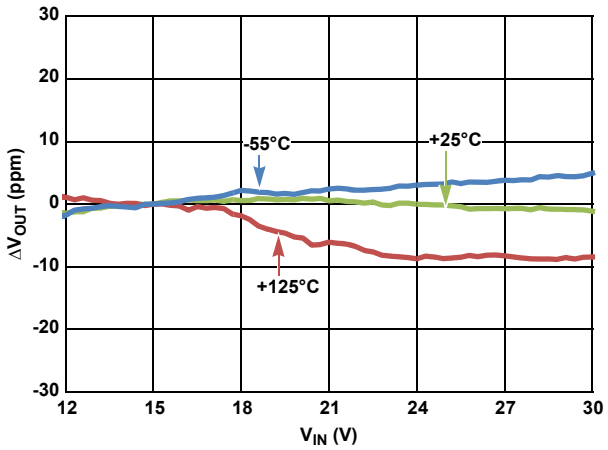


FIGURE 12. LINE REGULATION vs ΔV_{OUT} (ppm) OVER TEMPERATURE

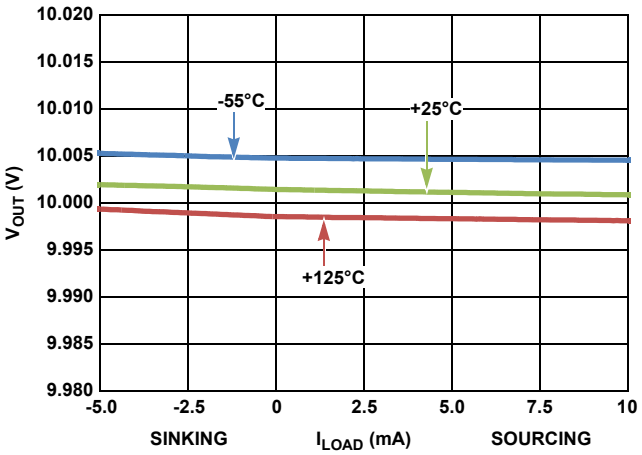


FIGURE 13. LOAD REGULATION vs V_{OUT} (V) OVER TEMPERATURE

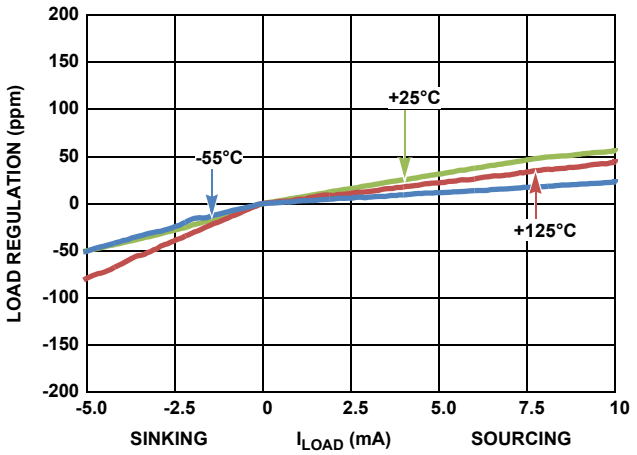


FIGURE 14. LOAD REGULATION vs V_{OUT} (PPM) OVER TEMPERATURE

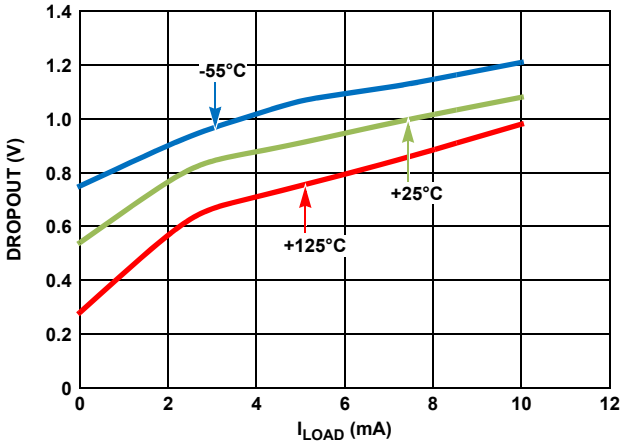


FIGURE 15. DROPOUT VOLTAGE vs OUTPUT CURRENT

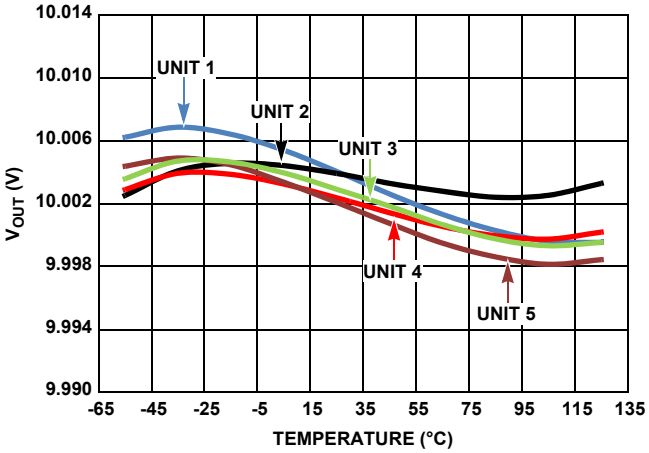


FIGURE 16. V_{OUT} vs TEMPERATURE

Typical Performance Curves

V_{IN} = 15V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified. **(Continued)**

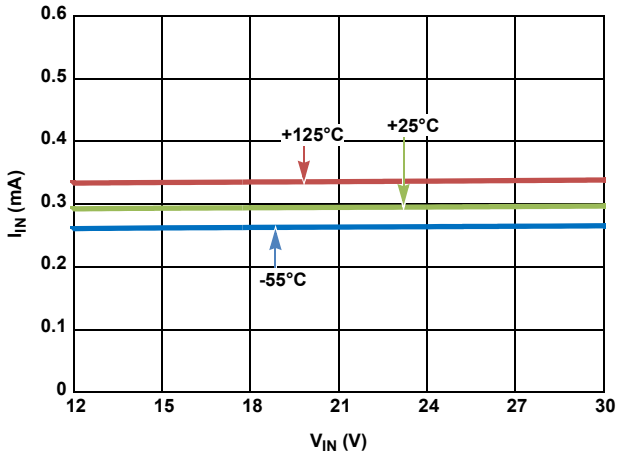


FIGURE 17. I_{IN} vs V_{IN} OVER TEMPERATURE

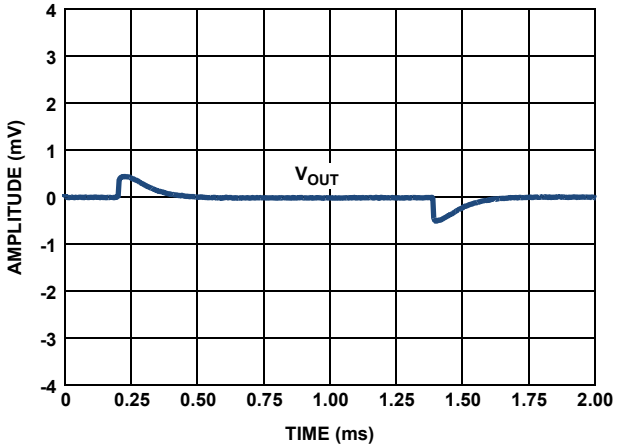


FIGURE 18. LINE TRANSIENT (ΔV_{IN} = 500mV)

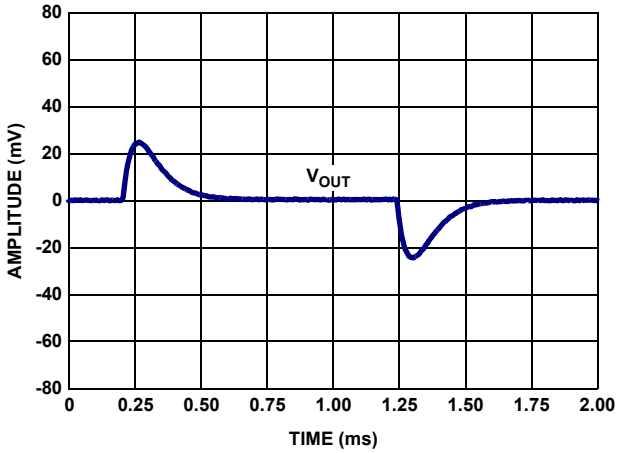


FIGURE 19. LOAD TRANSIENT (ΔI_L = 1mA)

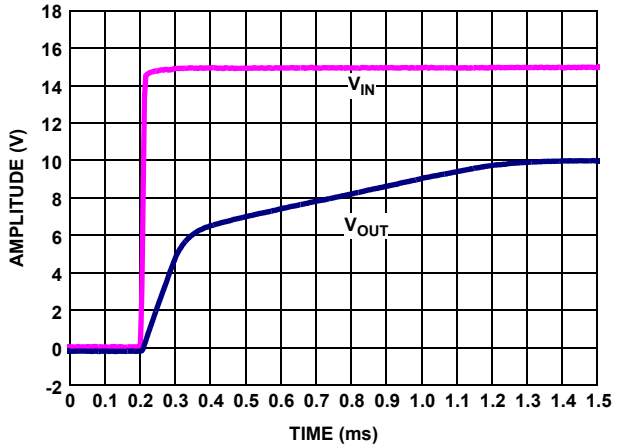


FIGURE 20. TURN-ON TIME

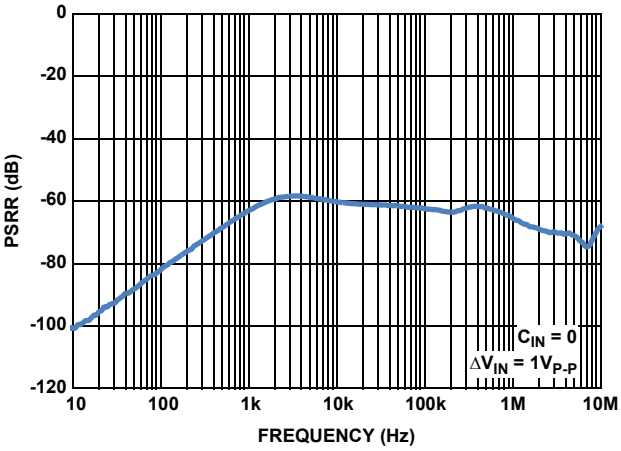


FIGURE 21. RIPPLE REJECTION vs FREQUENCY

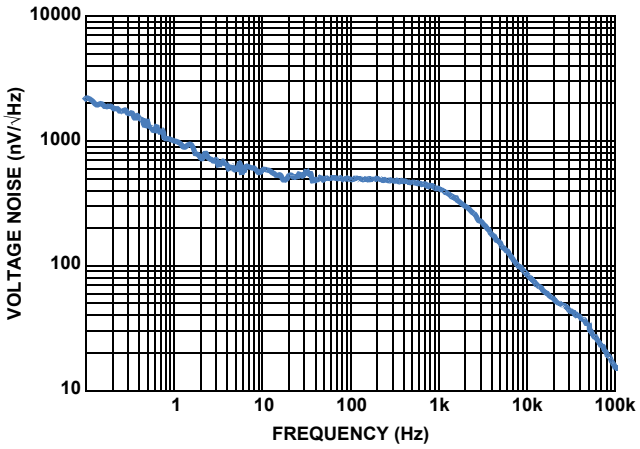


FIGURE 22. NOISE VOLTAGE DENSITY vs FREQUENCY

Typical Performance Curves

V_{IN} = 15V, T_A = +25°C, I_{OUT} = 0, C_{IN} = 0.1µF, C_L = 1µF and C_{COMP} = 0.001µF, unless otherwise specified. **(Continued)**

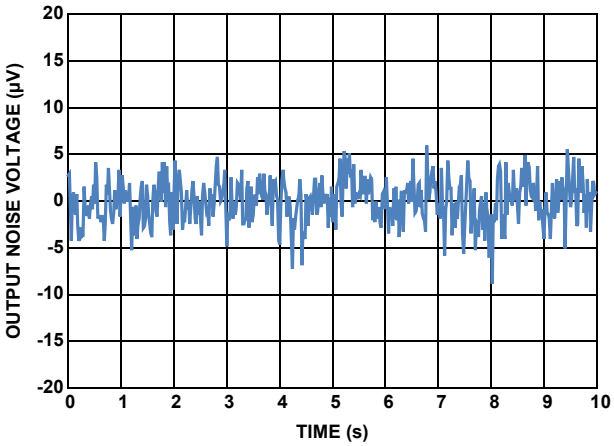


FIGURE 23. V_{OUT} vs NOISE, 0.1Hz TO 10Hz

Device Operation

Bandgap Precision References

The ISL71091SEH10 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

Applications Information

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally mild stresses to the die when the Printed Circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of 100µV to 500µV can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

Noise Performance and Reduction

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically 14.8µV_{P-P} (V_{OUT} = 10.0V). The noise measurement is made with a bandpass filter. The filter is made of a 1-pole high-pass filter, with a corner frequency at 0.1Hz, and a 2-pole low-pass filter, with a corner frequency (3dB) at 9.9Hz, to create a filter with a 9.9Hz bandwidth. Noise in the 10Hz to 1kHz bandwidth is approximately 14.7µV_{RMS} (V_{OUT} = 10.0V), with 0.1µF capacitance on the output. This noise measurement is made with a 2 decade bandpass filter. The filter is made of a 1-pole high-pass filter with a corner frequency at 10Hz of the center frequency, and 1-pole low-pass filter with a corner frequency at 1kHz. Load capacitance up to 10µF can be added but will result in only marginal improvements in output noise and transient response.

Turn-On Time

Normal turn-on time is typically 768µs, as shown in Figure 20 on page 9. The circuit designer must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, (V_{HIGH} – V_{LOW}), and divide by the temperature extremes of measurement (T_{HIGH} – T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The voltage at the trim pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference.

The suggested method to adjust the output is to connect a very high value external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a much lower total resistance and whose outer terminals connect to V_{OUT} and ground. It is important to minimize the capacitance on the trim terminal to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments, such as ±0.25%, will not disturb the factory-set temperature coefficient of the reference, but trimming by large amounts can.

Output Stage

The output stage of the device has a push-pull configuration with a high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 10mA and sink 5mA.

Use of COMP Capacitors

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from the COMP pin to GND. See Table 2 for recommended values of the COMP capacitor.

TABLE 2.

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

Data from SEE testing suggests the best option to use is 1µF for C_{OUT} and 1nF for C_{COMP}. Refer to the SEE report for more details.

DNC Pins

These pins are for trimming purposes and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

Simulation Model

A SPICE simulation model is available under the Documents tab of the ISL71091SEH10 landing page on the Intersil website. Figures 24 through 29 show a comparison of the characterized part performance and the simulated part performance.

Characterization vs Simulation Results

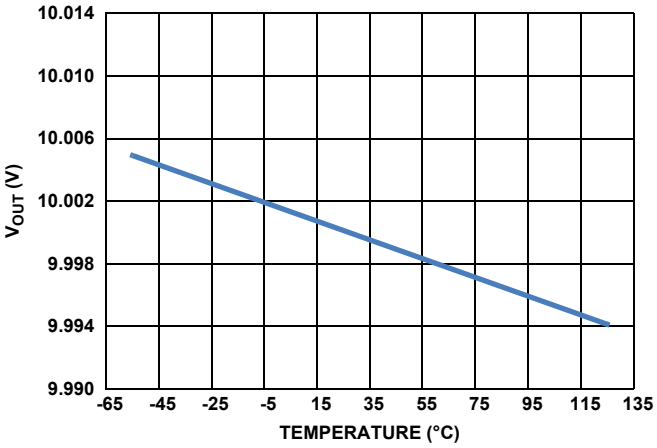


FIGURE 24. SIMULATED (WORSE CASE) V_{OUT} vs TEMPERATURE

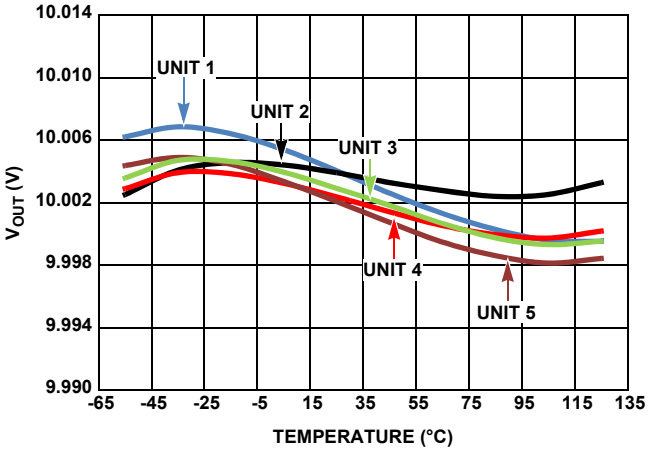


FIGURE 25. CHARACTERIZED V_{OUT} vs TEMPERATURE

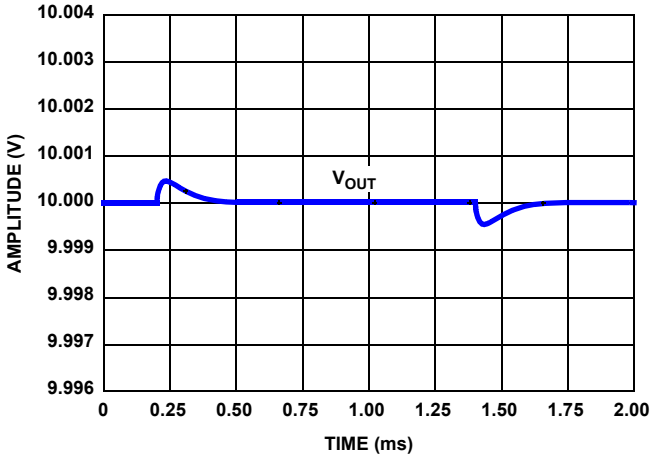


FIGURE 26. SIMULATED LINE TRANSIENT (ΔV_{IN} = 500mV)

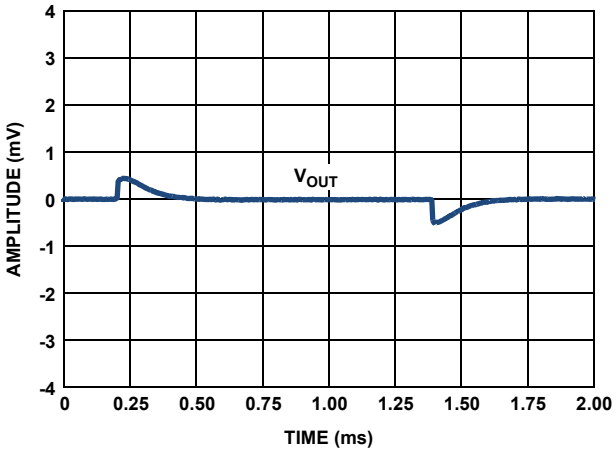


FIGURE 27. CHARACTERIZED LINE TRANSIENT (ΔV_{IN} = 500mV)

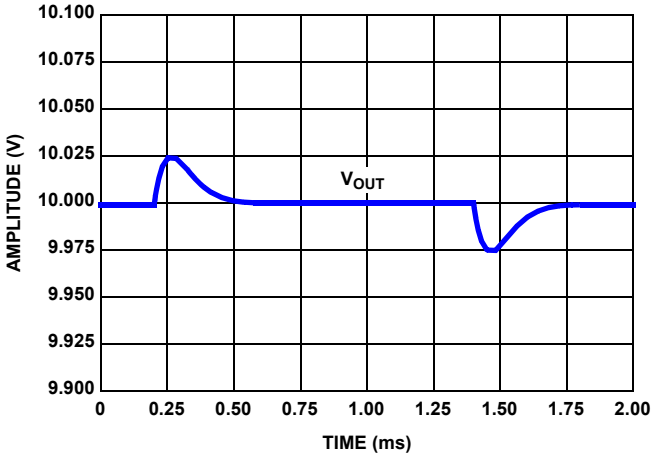


FIGURE 28. SIMULATED LOAD TRANSIENT (ΔI_L = 1mA)

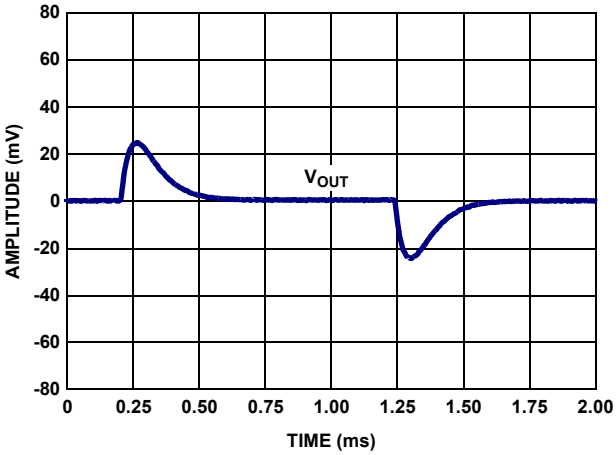


FIGURE 29. CHARACTERIZED LOAD TRANSIENT (ΔI_L = 1mA)

Package Characteristics

Weight of Packaged Device

0. 31 Grams (Typical)

Lid Characteristics

Finish: Gold
Potential: Connected to Pin #4 (GND)
Case Isolation to Any Lead: 20 x 10^9 Ω (minimum)

Die Characteristics

Die Dimensions

1990µm x 2380µm (78 mils x 94 mils)
Thickness: 483µm ± 25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

<2 x 10^5 A/cm^2

PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40

Metallization Mask Layout

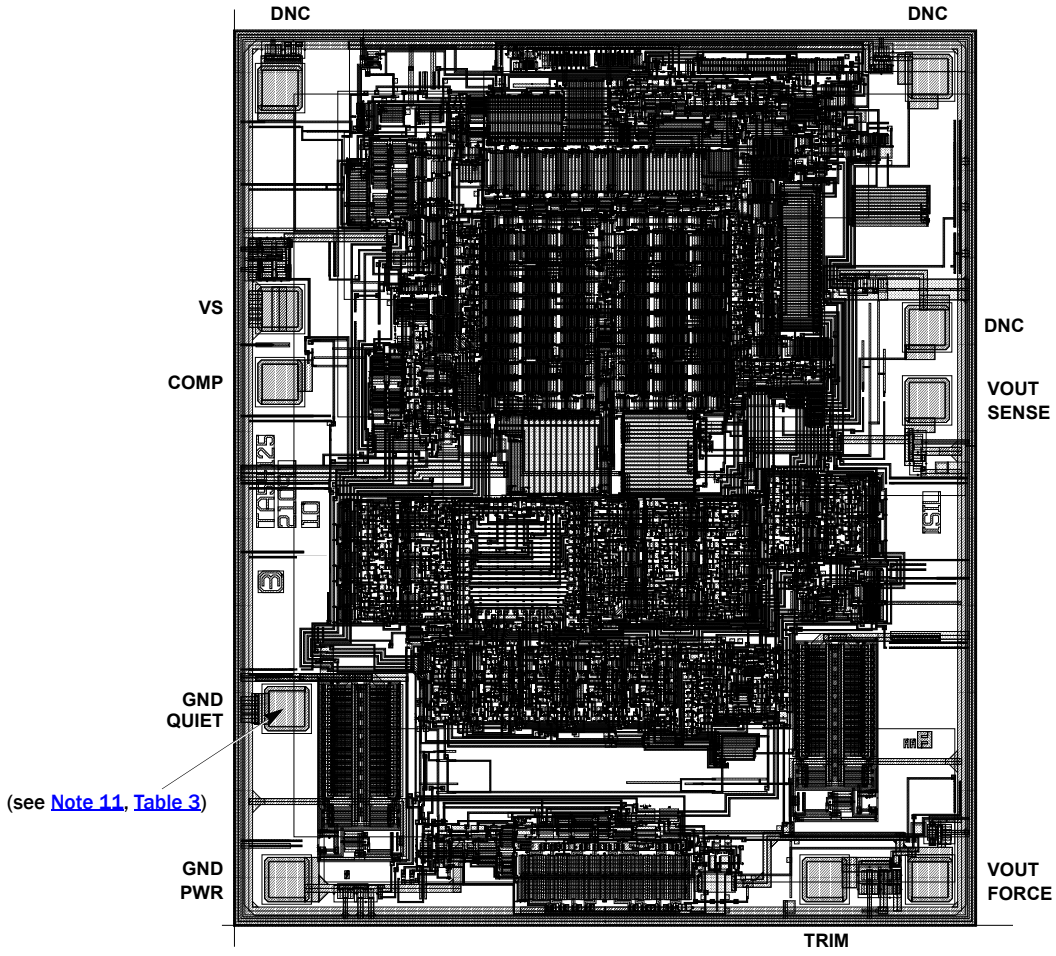


TABLE 3. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	BOND WIRES PER PAD (Note 12)
GND PWR	1	1	-436	1
GND QUIET	2	0	0	1
COMP	3	-15	831	1
VS	4	-17	1018	1
DNC	5			
DNC	6			
DNC	7			
VOUT SENSE	8	1633	786	1
VOUT FORCE	9	1640	-436	1
TRIM	10	1505	-436	1

NOTES:

11. Origin of coordinates is the centroid of GND QUIET.
12. Bond wire size is 1 mil.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 17, 2016	FN8633.2	-Updated Related Literature document titles to match titles on the actual documents. Added Table 1 on page 2. Added test information to ESD ratings in “Absolute Maximum Ratings” on page 5 On page 5: Changed Electrical Specification for Flatpack note From: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” To: “Boldface limits apply after radiation at +25°C or across the operating temperature range, -55°C to +125°C without radiation, unless other wise specified. For parameters V_{OA} (rows 2, 3, 4) on page 5 in Electrical Specifications for Flatpack table in the Conditions column changed From: “Note 10”, To: “Note 6” On page 6: Changed Electrical Specification For Die note From: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” To: “Boldface limits apply after radiation at +25°C or across the operating temperature range, -55°C to +125°C without radiation, unless other wise specified. For parameter V_{OA} Post Radiation (row 4) on page 6 in Electrical Specifications for Die table change description From: “V_{OUT} Accuracy at T_A = -55°C to +125°C, Post Rad”, To: “V_{OUT} Accuracy at T_A = +25°C, Post Radiation”. Updated POD K8.A to the latest revision changes are as follows: -Modified Note 2 by adding the words “...in addition to or instead of...”.
July 11, 2013	FN8633.1	Page 1 - changed title from: “Radiation Hardened Ultra Low Noise, Precision Voltage Reference” to: “10V Radiation Hardened Ultra Low Noise, Precision Voltage Reference”
May 28, 2014	FN8633.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

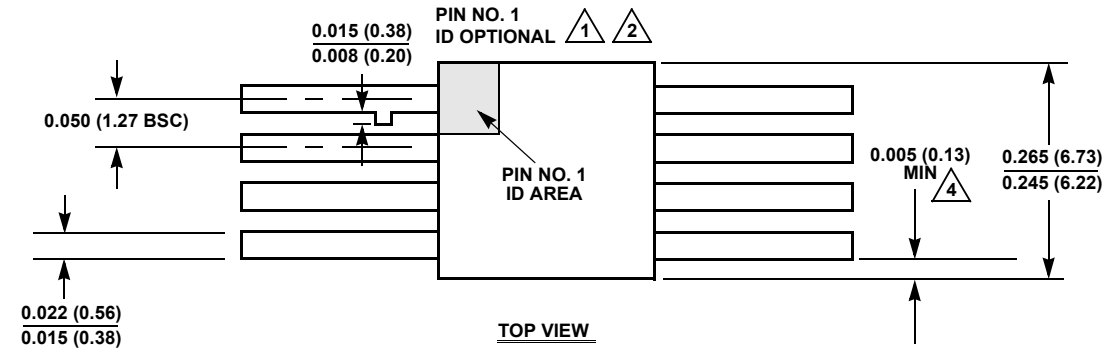
Reliability reports are also available from our website at www.intersil.com/support.

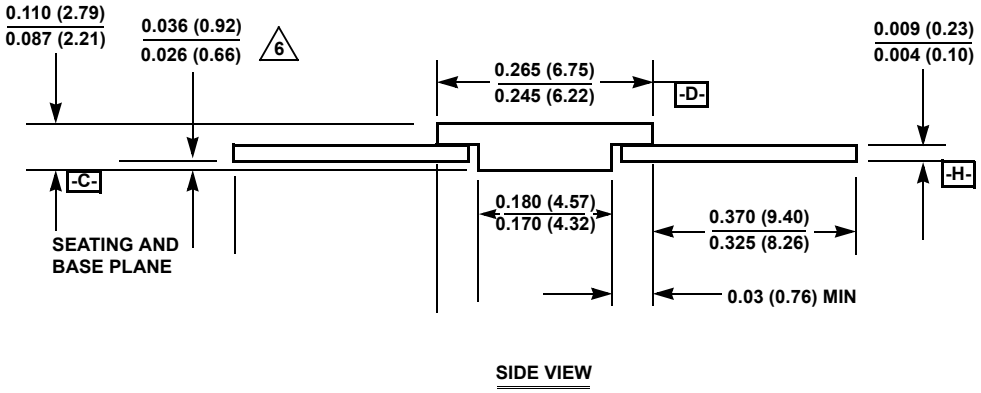
Package Outline Drawing

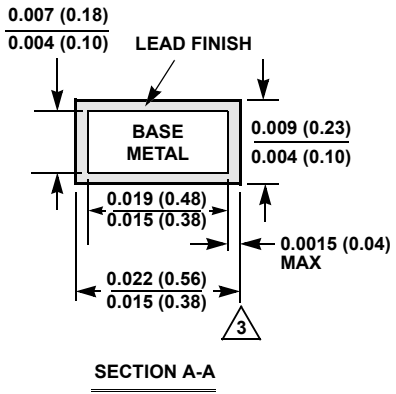
K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 4, 12/14







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.