ISL73841SEH

Radiation Tolerant 30V 32-Channel Analog Multiplexer

FN8846
Rev 3.00
Feb 23, 2018

The ISL73841SEH is a radiation tolerant, 32-channel high ESD protected multiplexer fabricated using the proprietary Renesas P6SOI (Silicon On Insulator) process technology. It operates with a dual supply voltage ranging from ±10.8V to ±16.5V. It has a 5-bit address plus an enable pin that can be driven with adjustable logic thresholds to conveniently select one of 32 available channels. An inactive channel is separated from an active channel by a high impedance, which inhibits any interaction between the channels.

The ISL73841SEH low r_{ON} allows for improved signal integrity and reduced power losses. The ISL73841SEH is also designed for cold sparing, making it excellent for high reliability applications that have redundancy requirements. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without loading signal sources. The ISL73841SEH also incorporates input analog overvoltage protection, which disables the switch to protect downstream devices.

The ISL73841SEH is available in a 48 Ld CQFP or die form and operates across the extended temperature range of -55°C to +125°C.

A 16-channel version in a 28 Ld CDFP is also available. Refer to the ISL73840SEH datasheet for more information. For a list of differences between the ISL73841SEH and ISL73840SEH, refer to Table 1 on page 3.

Related Literature

For a full list of related documents, visit our website

- ISL73841SEH product page

Features

- **DLA SMD #5962-15220**
- **Fabricated using P6SOI process technology**
- **ESD protection 8kV (HBM)**
- **Rail-to-rail operation**
- **Overvoltage protection**
- **Low r_{ON} . . . . . <500Ω (typical)**
- **Flexible split rail operation**
  - **Positive supply above GND (V^+) . . . . . +10.8V to +16.5V**
  - **Negative supply below GND (V^-) . . . . . -10.8V to -16.5V**
- **Adjustable logic threshold control with VREF pin**
- **Cold sparing capable (from ground) . . . . . ±25V**
- **Analog overvoltage range (from ground) . . . . . ±35V**
- **Off switch leakage . . . . . 100nA (maximum)**
- Transition times (t_R, t_F) . . . . . 500ns (typical)
- Break-before-make switching
- Grounded metal lid (internally connected)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si) (Note 1)
  - SEB LET_{TH} . . . . . 86.4MeV • cm^2/mg

NOTE:

1. Product capability established by initial characterization. All subsequent lots are assurance tested to 50krad (0.01rad(Si)/s) wafer-by-wafer.

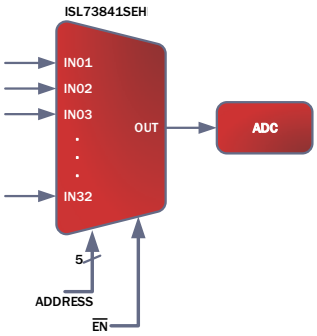

FIGURE 1. TYPICAL APPLICATION

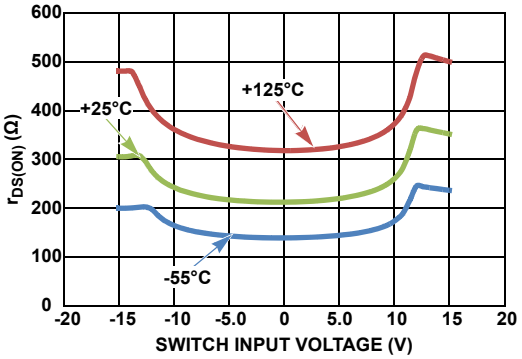

FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY ACROSS SWITCH INPUT COMMON-MODE VOLTAGE AT +25°C

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Ordering Information

ORDERING NUMBER (Note 3)	PART NUMBER (Note 2)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962L1522002VXC	ISL73841SEHVF	-55 to +125	48 LD CQFP	R48.A
N/A	ISL73841SEHF/PROTO (Note 4)	-55 to +125	48 LD CQFP	R48.A
5962L1522002V9A	ISL73841SEHVX	-55 to +125	DIE	N/A
N/A	ISL73841SEHX/SAMPLE (Note 4)	-55 to +125	DIE	N/A

NOTES:

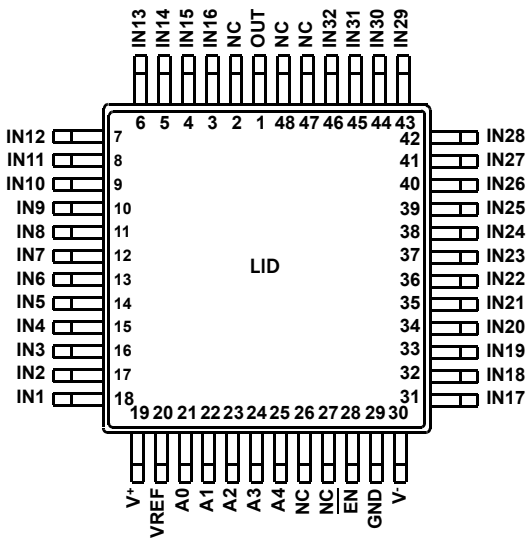
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

TABLE 1. TABLE OF DIFFERENCES

SPECIFICATION	ISL73841SEH	ISL73840SEH
Number of Channels	32	16
Supply Current (I+/I-)	400µA (maximum)	350µA (maximum)
Output Leakage (+125°C)	120nA (maximum)	60nA (maximum)

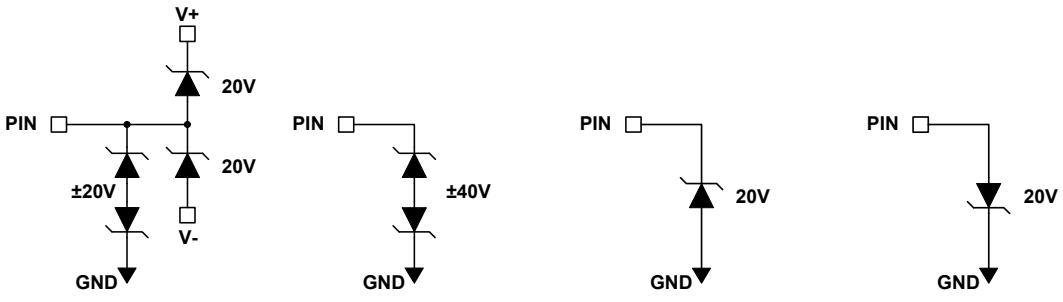
Pin Configuration

ISL73841SEH
(48 LD CQFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
NC	2, 26, 27, 47, 48	Not connected, no internal connection.
OUT	1	Output for multiplexer (see Circuit 1 in Figure 3)
V^+	19	Positive power supply (see Circuit 3 in Figure 3)
V^-	30	Negative power supply (see Circuit 4 in Figure 3)
INx	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46	Inputs for multiplexer (see Circuit 2 in Figure 3)
Ax	21, 22, 23, 24, 25	Address lines for multiplexer (see Circuit 3 in Figure 3)
$\overline{EN}$	28	Enable control for multiplexer (active low, see Circuit 3 in Figure 3)
VREF	20	Reference voltage used to set logic thresholds (see Circuit 3 in Figure 3)
GND	29	Ground
LID	-	Package Lid is internally connected to GND (Pin 29)



Circuit 1 Circuit 2 Circuit 3 Circuit 4

FIGURE 3. ESD Circuits

Absolute Maximum Ratings

Positive Supply Voltage above GND (V^+) (Note 7) . . . . . +20V
Negative Supply Voltage below GND (V^-) (Note 7) . . . . . -20V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 7) 40V
Analog Input Voltage (INx)
From GND (Note 7) . . . . . ±35V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . . GND to V^+
VREF to GND (Note 7) 16.5V
ESD Tolerance
Human Body Model (Tested per MIL-STD-883 TM 3015) 8kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A) 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld CQFP (Notes 5, 6)	50	2

Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Positive Supply Voltage Above GND (V^+) . . . . . +10.8V to +16.5V
Negative Supply Voltage Below GND (V^-) . . . . . -10.8V to -16.5V
Supply Voltage Differential (V^+ to V^-) . . . . . 21.6V to 33V
VREF to GND . . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the package underside.
7. Tested in a heavy ion environment at LET = 86.3MeV • cm^2/mg at +125°C.

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Analog Input Signal Range	V_S		V^-	-	V^+	V
Channel ON-Resistance	r_{ON}	V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±15.0V, ±16.5V I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
r_{ON} Match Between Channels	Δr_{ON}	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
ON-Resistance Flatness	$R_{FLAT(ON)}$	V_{IN} = +5V, -5V	-	-	**25**	Ω
Switch Off Leakage	$I_{S(OFF)}$	V_{IN} = V^+ - 5V, V± = ±16.5V All unused inputs are tied to V^- + 5V	**-10**	-	**10**	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V^- + 5V, V± = ±16.5V All other inputs = V^+ - 5V T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-100	-	100	nA
Switch Off Leakage with Device Powered Off	$I_{S(OFF)\ POWER\ OFF}$	V_{IN} = +25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total Ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Switch Off Leakage with Device Powered Off	$I_{S(OFF)\ POWER\ OFF}$	V_{IN} = +25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, $V_{\overline{EN}}/V_A/V_{REF}$ = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA
Switch On Leakage Current into the Source (overvoltage)	$I_{S(ON)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-500	-	500	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-500	-	500	nA
Switch Off Leakage Current into the Source (overvoltage)	$I_{S(OFF)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-750	-	750	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-750	-	750	nA
Switch Off Leakage	$I_{D(OFF)}$	V_{OUT} = V^+ - 5V, all inputs = V^- + 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-80	-	80	nA
		V_{OUT} = V^- + 5V, all inputs = V^+ - 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-80	-	80	nA
Switch Off Leakage Current into the Drain (overvoltage)	$I_{D(OFF)\ OVERVOLT}$	V_{OUT} = 0V, V_{IN} = +35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA
		V_{OUT} = 0V, V_{IN} = -35V, V± = ±16.5V All unused inputs are tied to GND	**-10**	-	**10**	nA
		Post radiation	-500	-	500	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Switch On Leakage Current into the Source/Drain	$I_{D(ON)}$	V_{IN} = V_{OUT} = V^+ - 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V_{OUT} = V^- + 5V, T_A = +25°C, -55°C All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-100	-	100	nA
Logic Input High/Low Voltage	$V_{AH/L}$, $V_{ENH/L}$	V_{REF} = 5.0V	**1.2**	-	**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V_A = $V_{\overline{EN}}$ = 4.0V V^+= 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V_A = $V_{\overline{EN}}$ = 0.8V V+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Quiescent Supply Current	I+	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
Quiescent Supply Current	I-	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**-400**	-		µA
Standby Supply Current	I+	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
Standby Supply Current	I-	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**-400**	-		µA
Supply Current into V_{REF}	I_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**10**	-	**35**	µA
	DYNAMIC					
Transition Time	t_{ALH}	Figures 5, 6	-	0.5	**800**	ns
Transition Time	t_{AHL}	Figures 5, 6	-	0.5	**800**	ns
Break-Before-Make Delay	t_{BBM}	Figures 9, 10	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
Enable Turn-On Time	t_{ENABLE}	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
Disable Turn-Off Time	$t_{DISABLE}$	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, (Figure 7)	-	2	5	pC
Off Isolation	V_{ISO}	$V_{\overline{EN}}$ = 4V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	75	-	-	dB
Crosstalk	V_{CT}	$V_{\overline{EN}}$ = 0.8V, R_L = 1kΩ, f = 200kHz, C_L = 7pF, V_{RMS} = 3V	47	-	-	dB
Digital Input Capacitance	C_A	f = 1MHz, V^+ = V^- = 0V	-	-	**7**	pF
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz, V^+ = V^- = 0V	-	-	**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz, V^+ = V^- = 0V	-	-	**50**	pF

Electrical Specifications (±12V)

V^+ = 12V, V^- = -12V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
V_S	Analog Input Signal Range		V^-		V^+	V
r_{ON}	Channel ON-Resistance	V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±10.8V, ±13.2V I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
Δr_{ON}	r_{ON} Match Between Channels	V_{IN} = +5V, -5V; I_{OUT} = -1mA	-	10	**20**	Ω
$R_{FLAT(ON)}$	ON-Resistance Flatness	V_{IN} = +5V, -5V, V± = ±13.2V	-	-	**25**	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, T_A = +25°C, -55°C, +125°C	-	-	30	Ω
		V_{IN} = +5V, -5V, V± = ±10.8V, post radiation			**40**	Ω
I+	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	-	-	**400**	µA
I-	Quiescent Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-400**	-	**-**	µA
I+	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	-	-	**400**	µA
I-	Standby Supply Current	V_{IN} = V_A = $V_{\overline{EN}}$ = 4.0V, V± = ±10.8V, ±13.2V	**-400**	-	**-**	µA
I_{REF}	Supply Current Into V_{REF}	V_{REF} = 5.5V, V_{IN} = V_A = $V_{\overline{EN}}$ = 0.8V, V± = ±10.8V, ±13.2V	**-**	-	**35**	µA
DYNAMIC						
t_{ALH}	Transition Time	Figures 5, 6	-	0.5	**800**	ns
t_{AHL}	Transition Time	Figures 5, 6	-	0.5	**800**	ns
t_{BBM}	Break-Before-Make Delay	Figures 9, 10	**5**	50	**200**	ns
		Post radiation	**5**	-	**400**	ns
t_{ENABLE}	Enable Turn-On Time	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns
$t_{DISABLE}$	Disable Turn-Off Time	Figures 7, 8	-	0.5	**600**	ns
		Post radiation	-	-	**800**	ns

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

TABLE 2. TRUTH TABLE

A4	A3	A2	A1	A0	EN	"ON"-CHANNEL
X	X	X	X	X	1	None
0	0	0	0	0	0	1
0	0	0	0	1	0	2
0	0	0	1	0	0	3
0	0	0	1	1	0	4
0	0	1	0	0	0	5
0	0	1	0	1	0	6
0	0	1	1	0	0	7
0	0	1	1	1	0	8
0	1	0	0	0	0	9
0	1	0	0	1	0	10
0	1	0	1	0	0	11
0	1	0	1	1	0	12
0	1	1	0	0	0	13
0	1	1	0	1	0	14
0	1	1	1	0	0	15
0	1	1	1	1	0	16
1	0	0	0	0	0	17
1	0	0	0	1	0	18
1	0	0	1	0	0	19
1	0	0	1	1	0	20
1	0	1	0	0	0	21
1	0	1	0	1	0	22
1	0	1	1	0	0	23
1	0	1	1	1	0	24
1	1	0	0	0	0	25
1	1	0	0	1	0	26
1	1	0	1	0	0	27
1	1	0	1	1	0	28
1	1	1	0	0	0	29
1	1	1	0	1	0	30
1	1	1	1	0	0	31
1	1	1	1	1	0	32

NOTE: X = Don't care, "1" = Logic High, "0" = Logic Low

Block Diagram

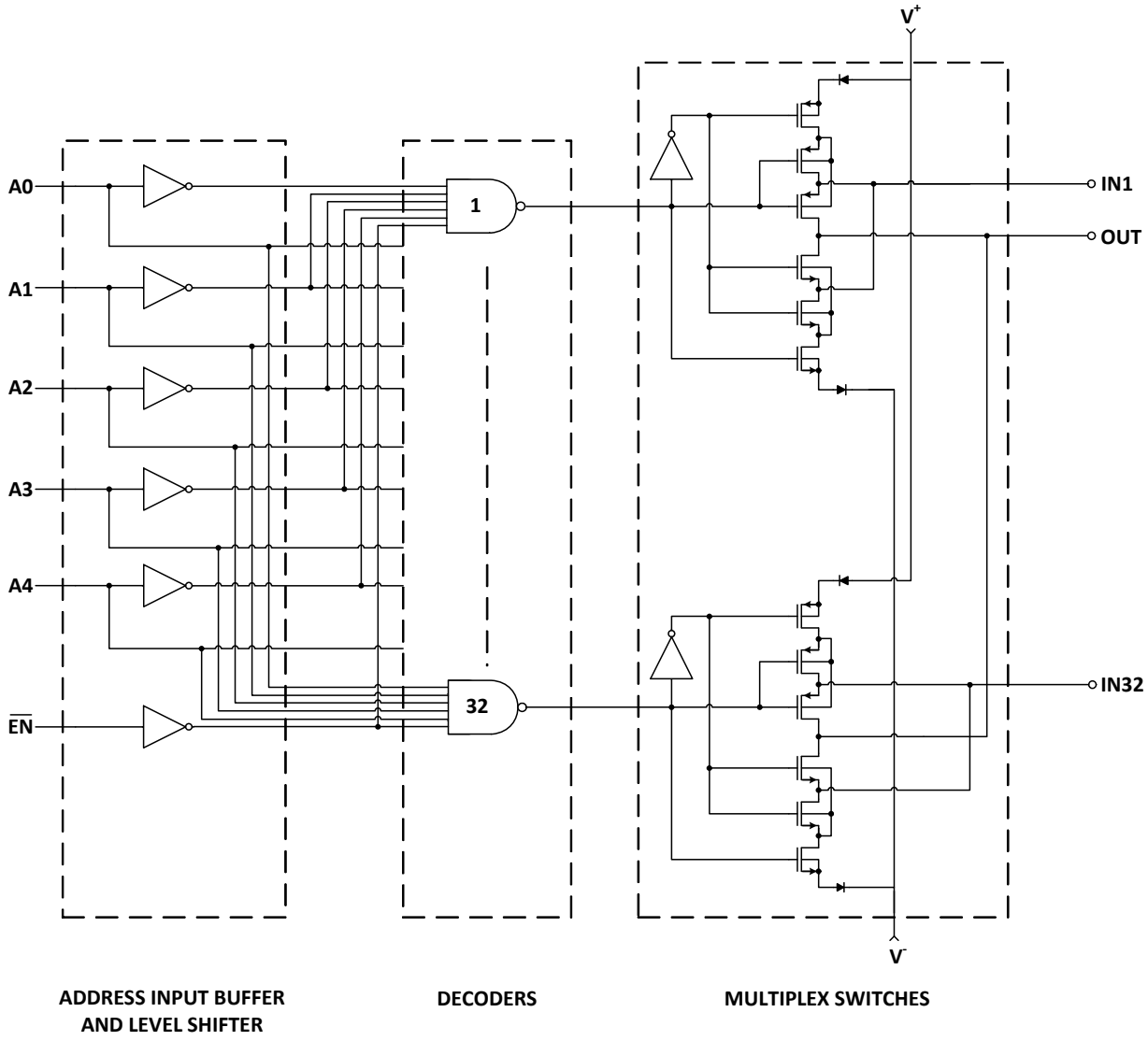


FIGURE 4. BLOCK DIAGRAM

Timing Diagrams

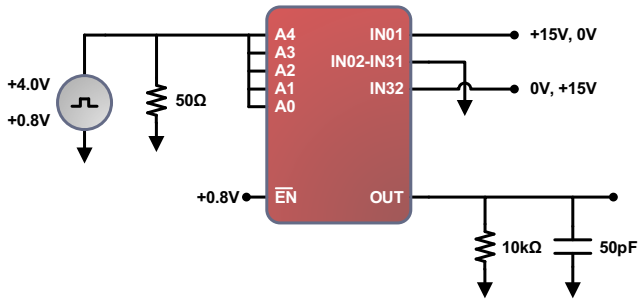


FIGURE 5. ADDRESS TIME TO OUTPUT TEST CIRCUIT

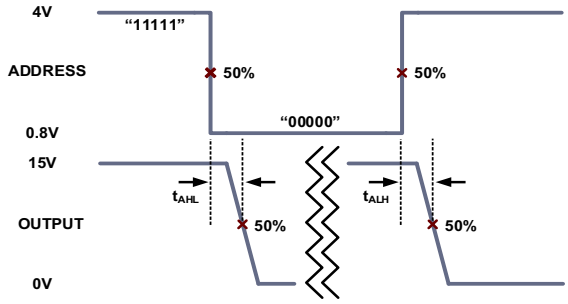


FIGURE 6. ADDRESS TIME TO OUTPUT DIAGRAM

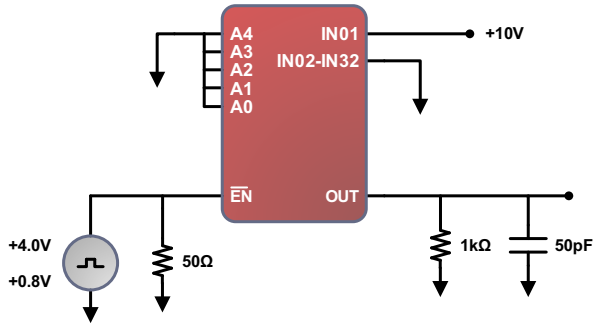


FIGURE 7. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

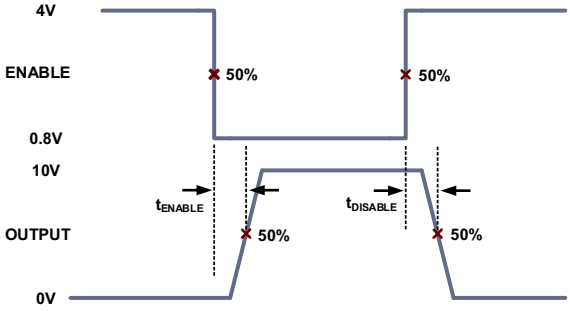


FIGURE 8. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

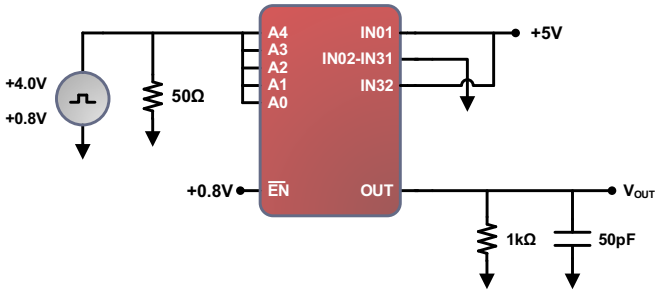


FIGURE 9. BREAK-BEFORE-MAKE TEST CIRCUIT

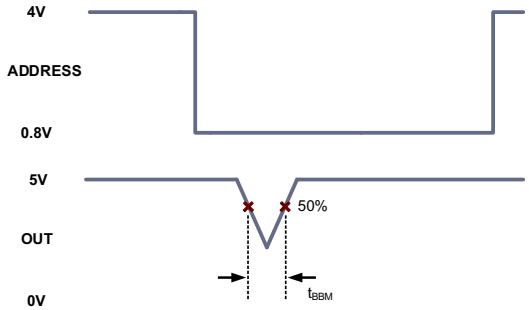


FIGURE 10. BREAK-BEFORE-MAKE DIAGRAM

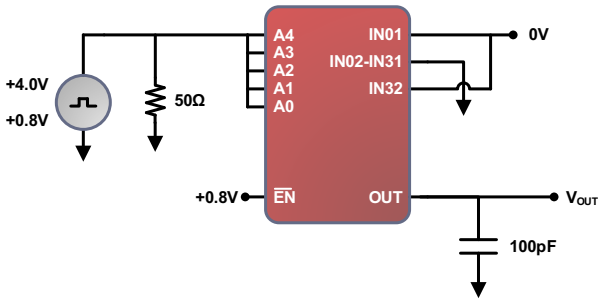


FIGURE 11. CHARGE INJECTION TEST CIRCUIT

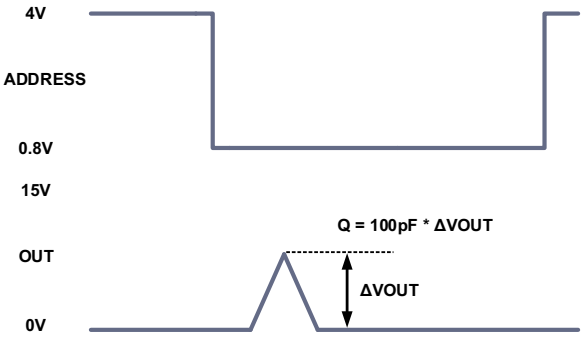


FIGURE 12. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified.

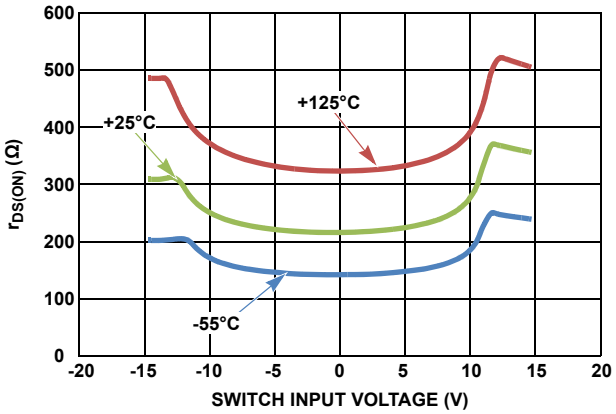


FIGURE 13. $r_{DS(ON)}$ vs VCM (V± = 14.5V)

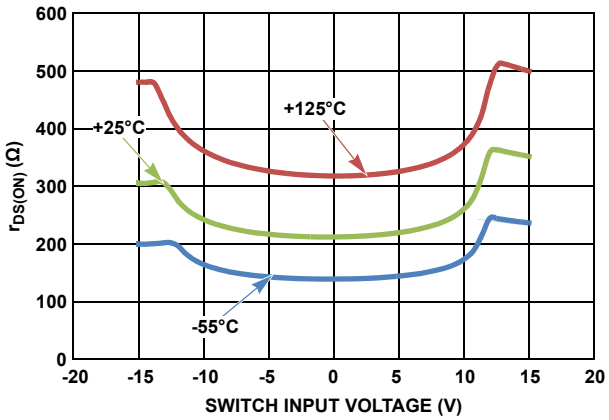


FIGURE 14. $r_{DS(ON)}$ vs VCM (V± = 15.0V)

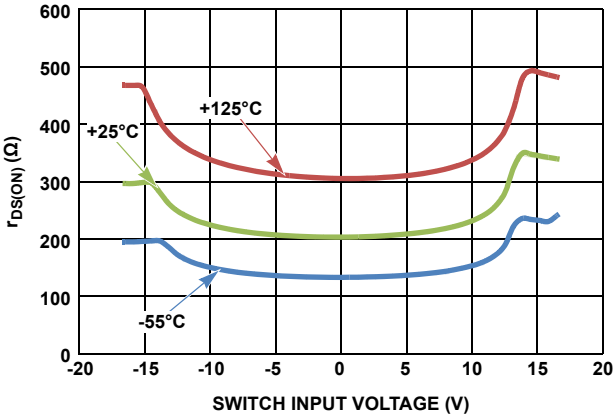


FIGURE 15. $r_{DS(ON)}$ vs VCM (V± = 16.5V)

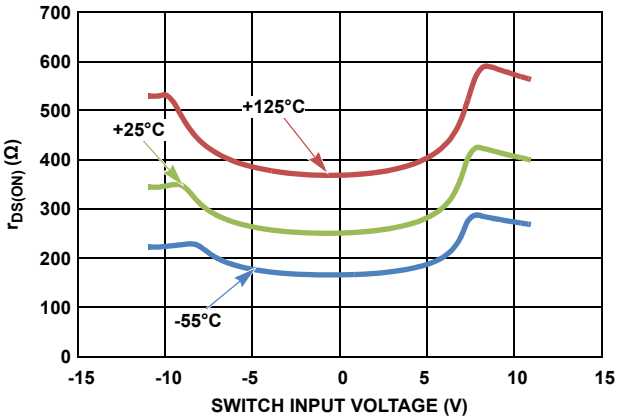


FIGURE 16. $r_{DS(ON)}$ vs VCM (V± = 10.8V)

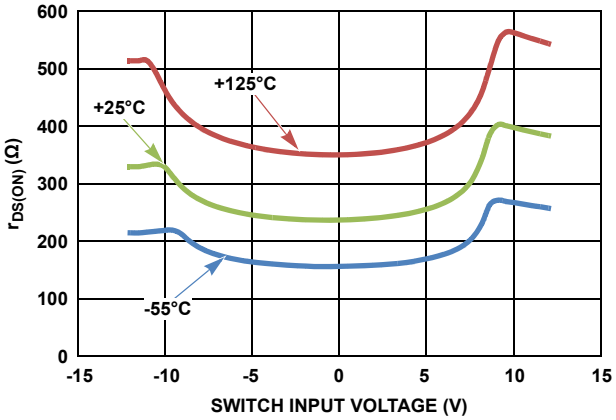


FIGURE 17. $r_{DS(ON)}$ vs VCM (V± = 12.0V)

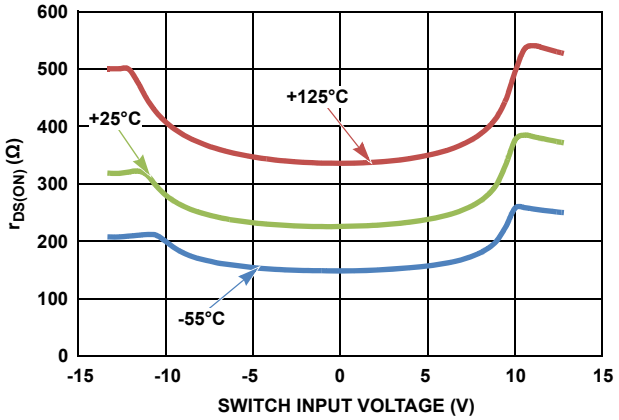


FIGURE 18. $r_{DS(ON)}$ vs VCM (V± = 13.2V)

Typical Performance Curves

$V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

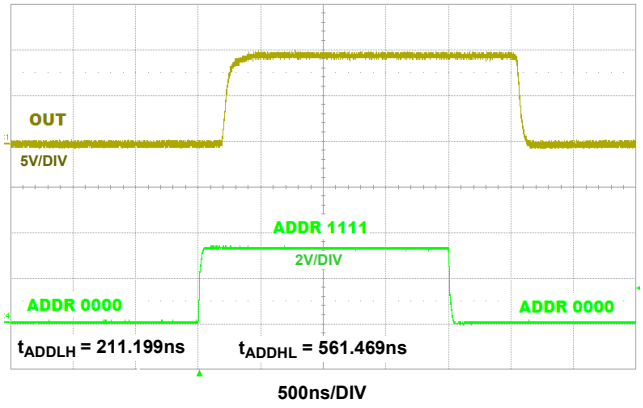


FIGURE 19. TYPICAL ADDRESS TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

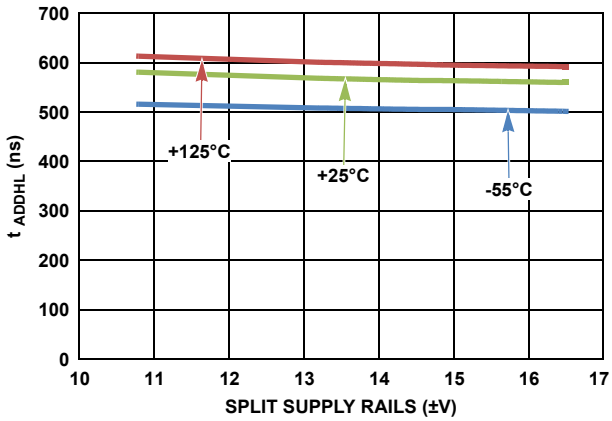


FIGURE 20. ADDRESS TO OUTPUT DELAY (HIGH TO LOW)

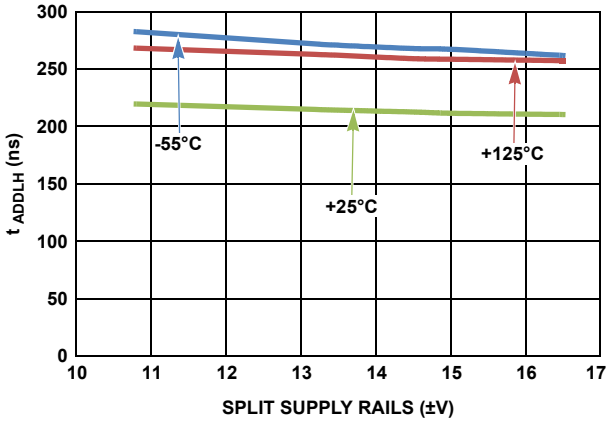


FIGURE 21. ADDRESS TO OUTPUT DELAY (LOW TO HIGH)

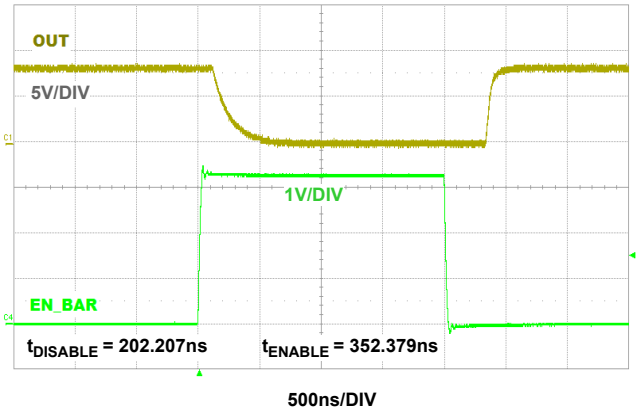


FIGURE 22. TYPICAL ENABLE TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

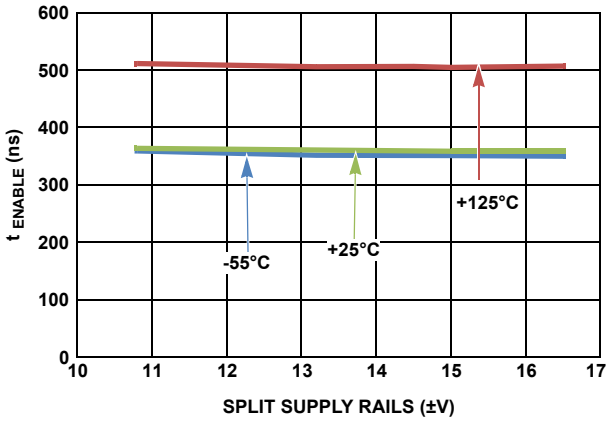


FIGURE 23. ENABLE TO OUTPUT DELAY (LOW TO HIGH)

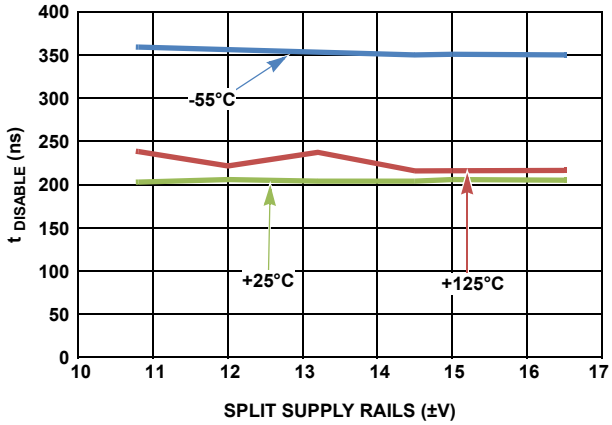


FIGURE 24. DISABLE TO OUTPUT DELAY (LOW TO HIGH)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Continued)

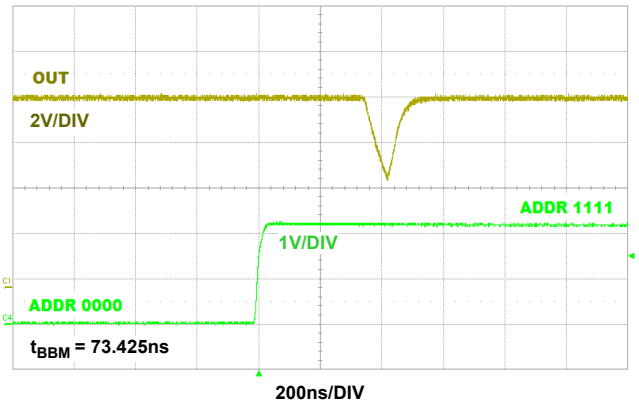


FIGURE 25. TYPICAL BREAK-BEFORE-MAKE DELAY (V± = 15V, +25°C)

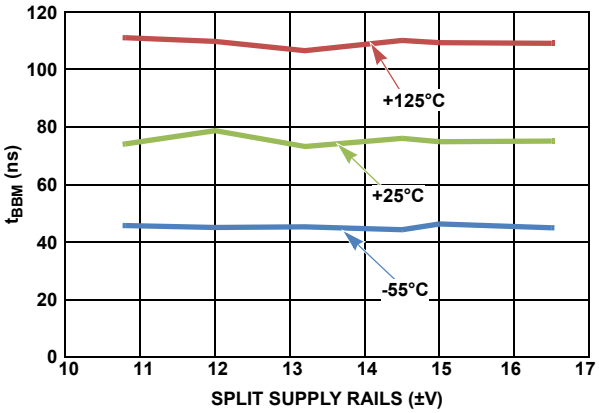


FIGURE 26. BREAK-BEFORE-MAKE DELAY

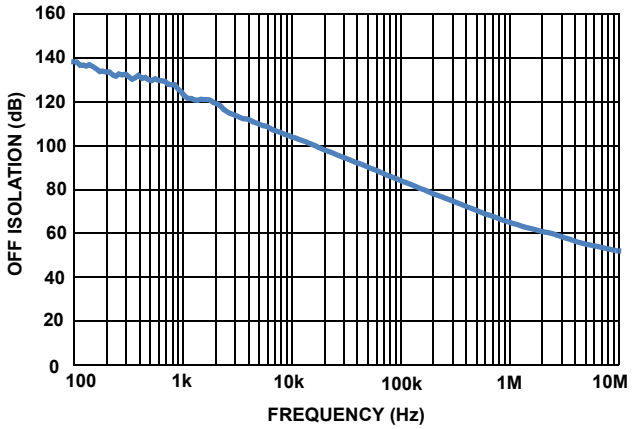


FIGURE 27. OFF ISOLATION (V± = ±15V, R_L = 1kΩ, +25°C)

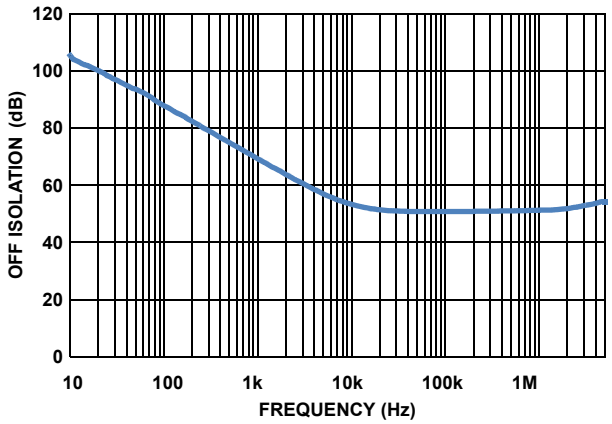


FIGURE 28. OFF ISOLATION (V± = ±15V, R_L = OPEN, +25°C)

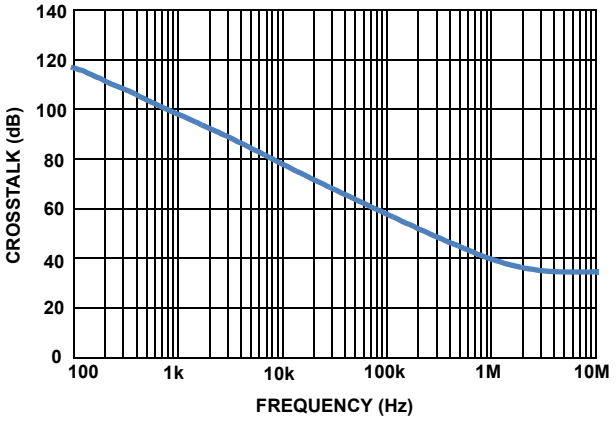


FIGURE 29. CROSSTALK (V± = ±15V, R_L = 1kΩ, +25°C)

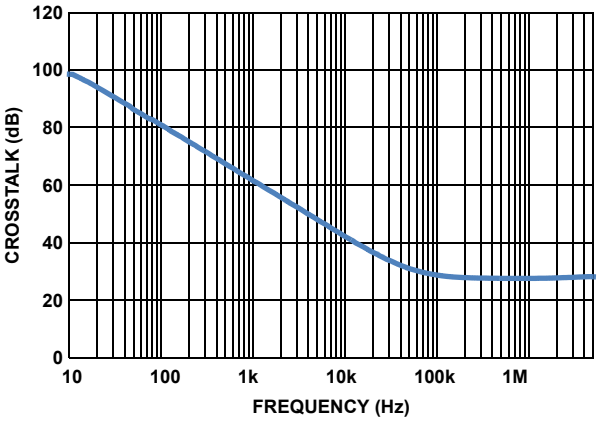


FIGURE 30. CROSSTALK (V± = ±15V, R_L = OPEN, +25°C)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

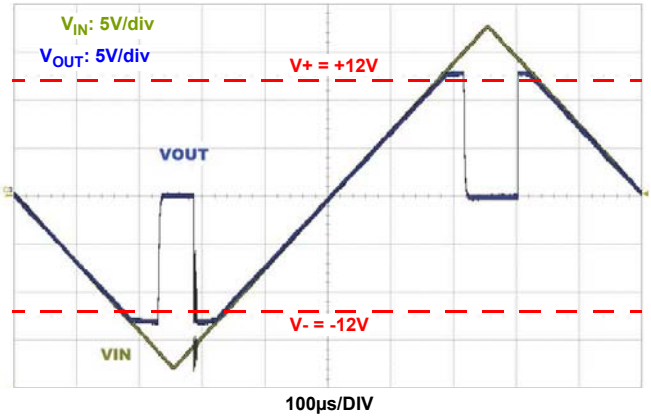


FIGURE 31. OVERVOLTAGE/UNDERVOLTAGE PROTECTION (+25°C)

Post Low Dose Rate Radiation Characteristics ($V\pm = \pm15V$)

Unless otherwise specified, $V\pm = \pm15V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

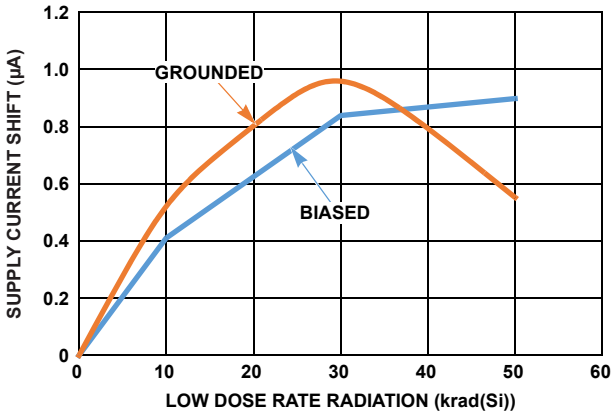


FIGURE 32. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

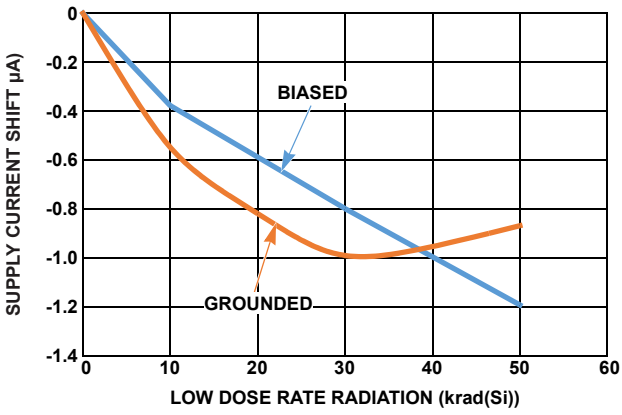


FIGURE 33. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

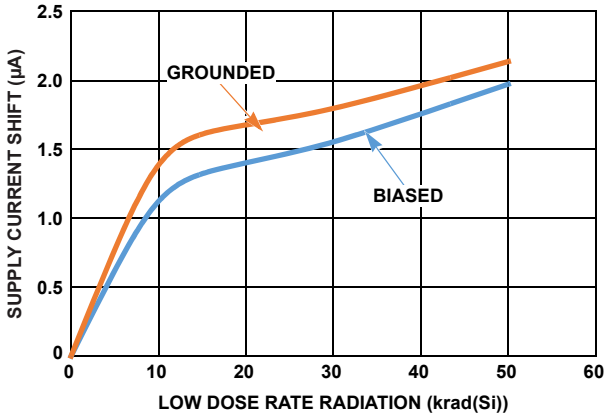


FIGURE 34. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

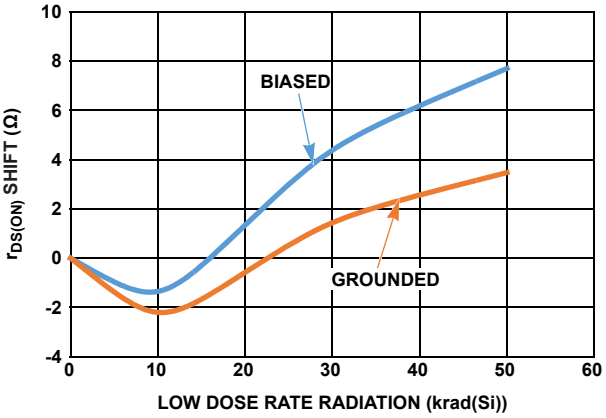


FIGURE 35. $r_{DS(ON)}$ SHIFT ($V_{IN} = +5V$) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

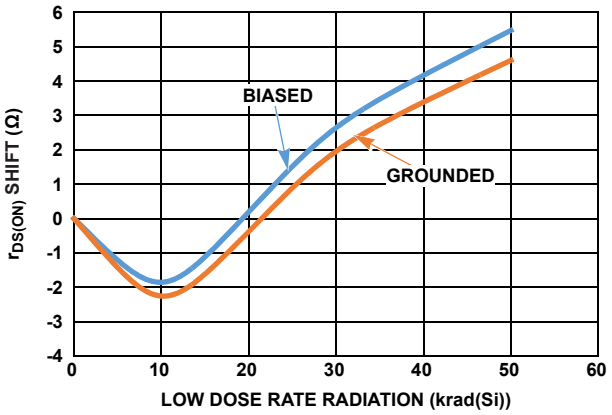


FIGURE 36. $r_{DS(ON)}$ Shift (V_{IN} = -5V) vs LDR RADIATION

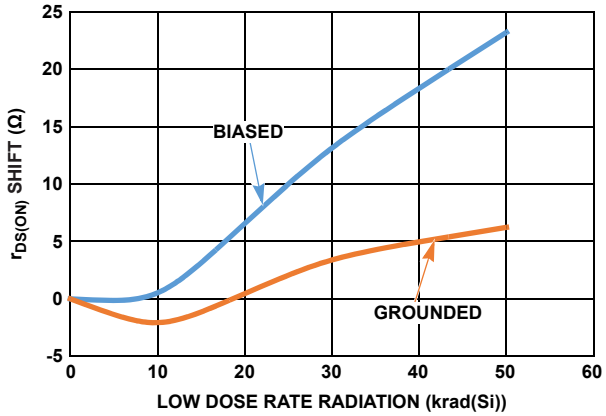


FIGURE 37. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

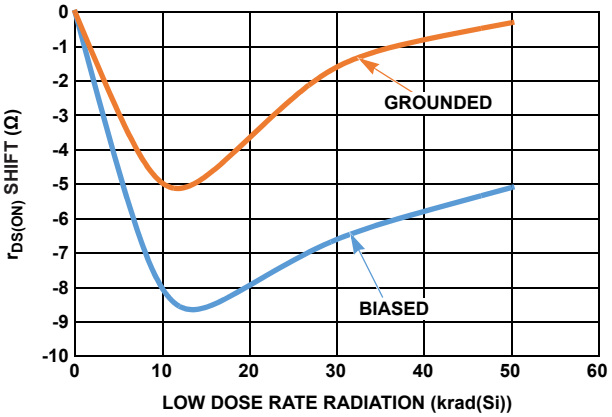


FIGURE 38. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

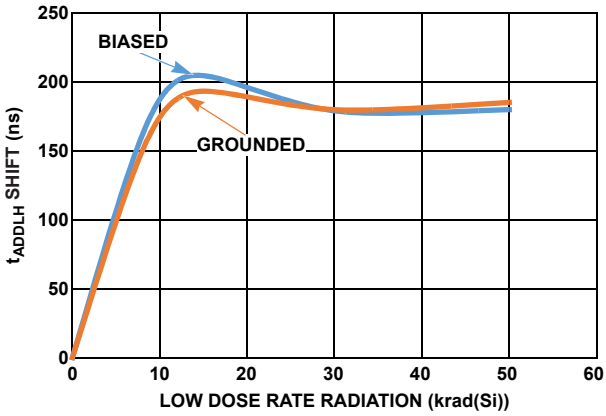


FIGURE 39. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

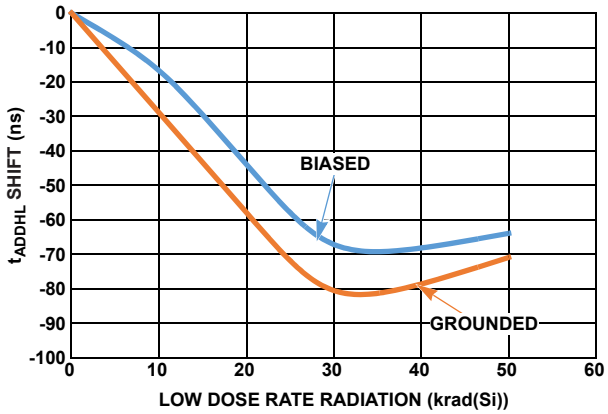


FIGURE 40. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

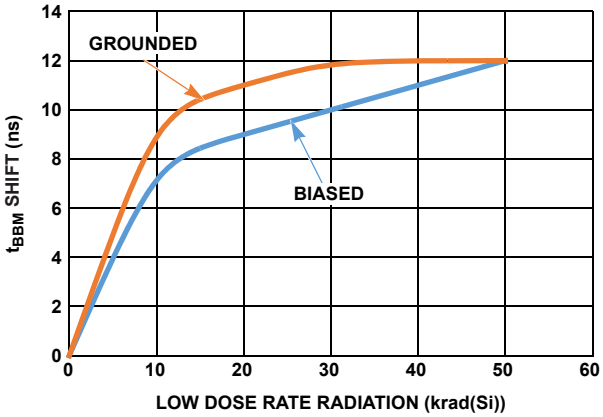


FIGURE 41. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

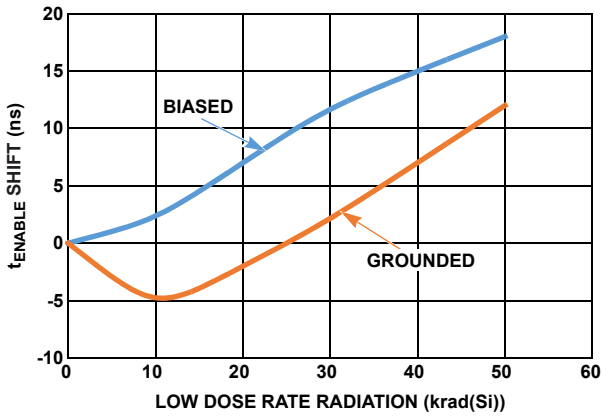


FIGURE 42. t_{ENABLE} SHIFT vs LDR RADIATION

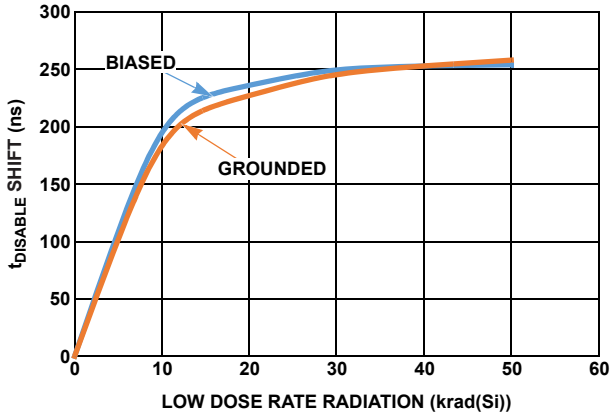


FIGURE 43. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

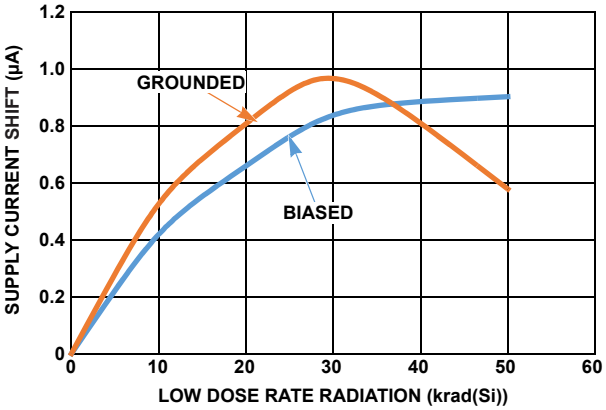


FIGURE 44. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

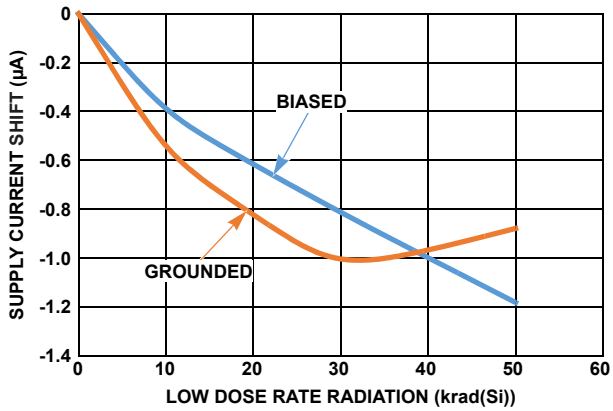


FIGURE 45. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

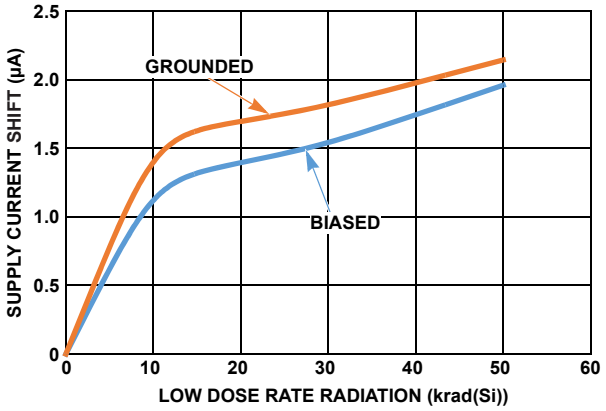


FIGURE 46. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

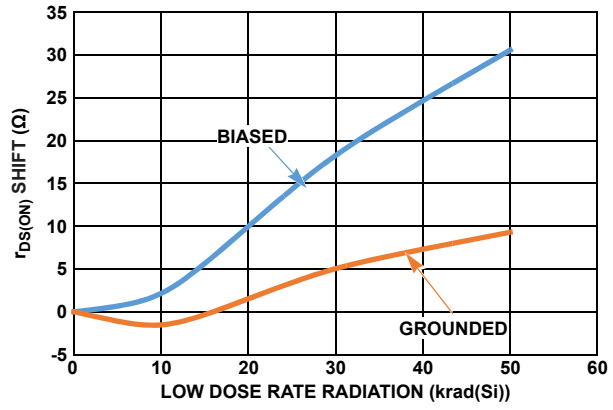


FIGURE 47. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

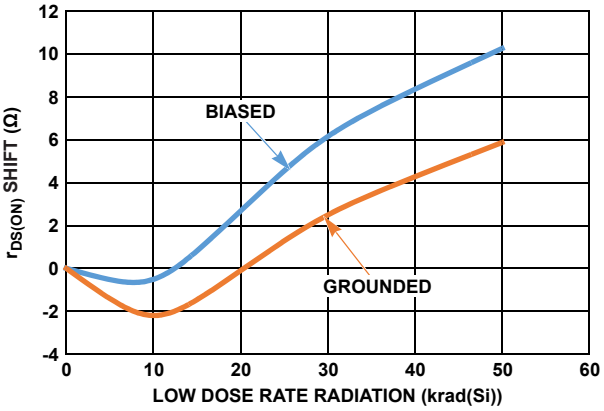


FIGURE 48. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

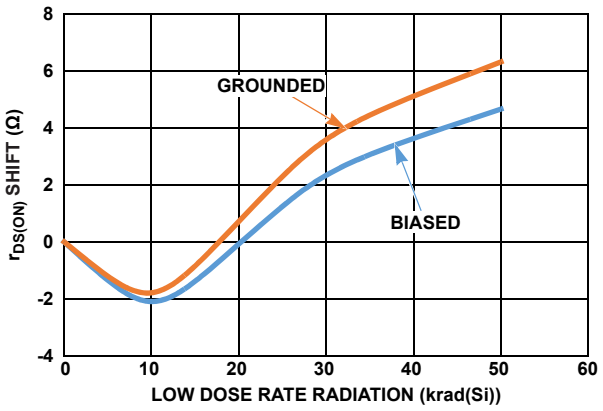


FIGURE 49. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

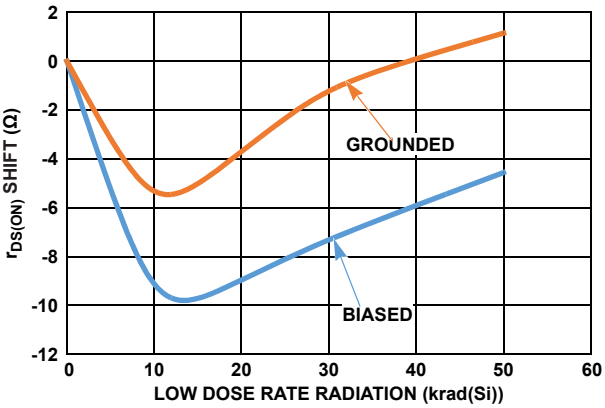


FIGURE 50. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

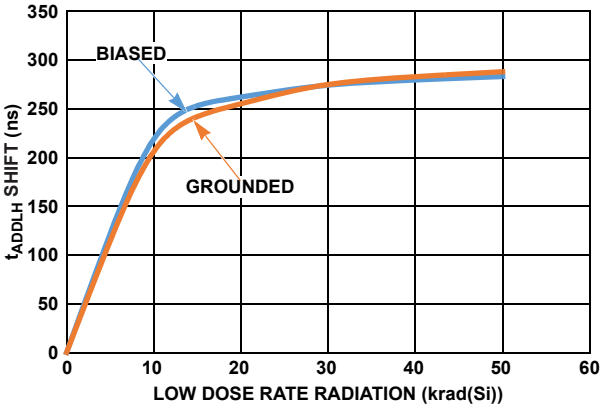


FIGURE 51. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

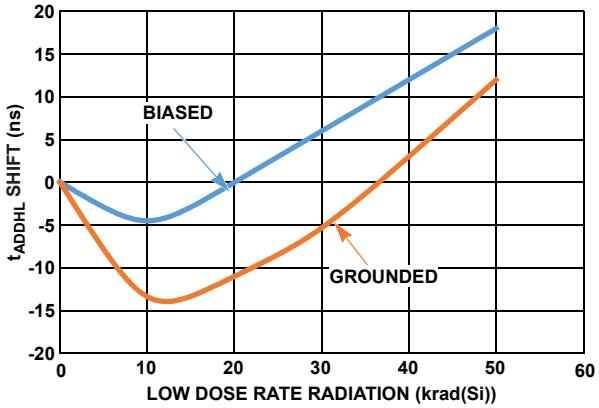


FIGURE 52. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

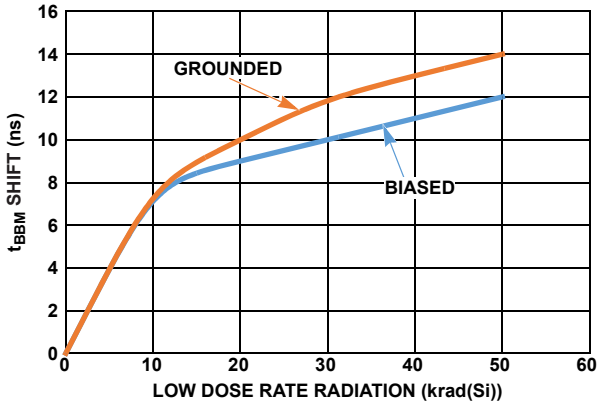


FIGURE 53. t_{BBM} SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

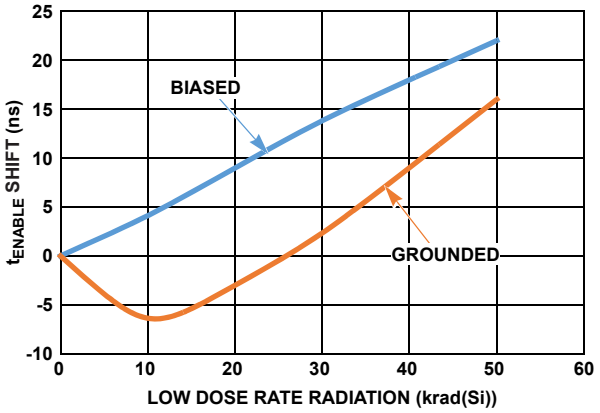


FIGURE 54. t_{ENABLE} SHIFT vs LDR RADIATION

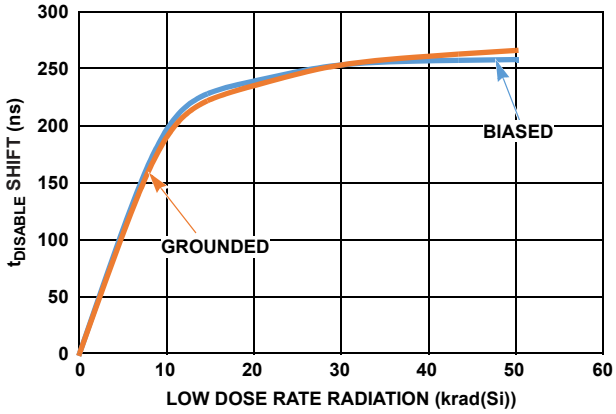


FIGURE 55. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+, V^-, and VREF; however, it is recommended that all supplies power-up relatively close to each other.

Overvoltage Protection

The ISL73841SEH has overvoltage protection on both the input and the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition (3V to 4V past the rail), the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL73841SEH. The range for VREF is between 4.5V and 5.5V with a nominal voltage of 5V. The address pins and enable are compared against roughly 30% of V_{REF} voltage (refer to Figure 56). With 5.0V on V_{REF}, the switching point is set to around 1.4V. This switching point allows for both 5V and 3.3V logic control.

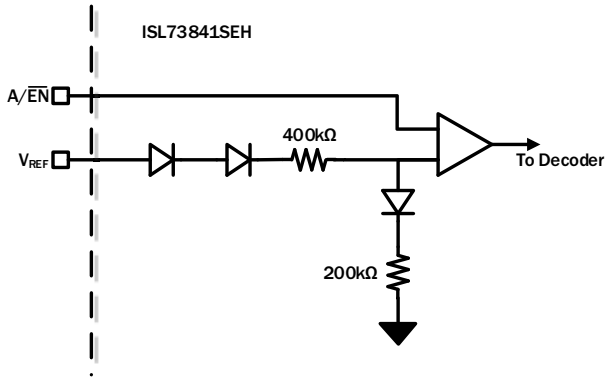


FIGURE 56. SIMPLIFIED V_{REF} CIRCUITRY

Considerations for Redundant Applications

When using the ISL73841SEH in a cold sparing application, it is recommended to keep the ground pin connected to system ground at all times. All supply pins (V^+, V^-, and VREF) should either be grounded or floating together.

If the supply pins are floating, it is recommended to place a high value bleed resistor (~1MΩ) in parallel with the decoupling caps on each supply pin to ensure that the supply voltage is discharged in a predictable manner. Figures 57 and 58 illustrate the recommended cold sparing setup for both shorted and floating supplies.

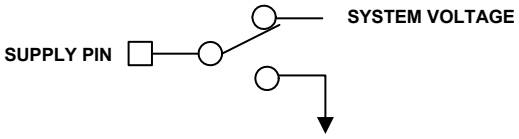


FIGURE 57. COLD SPARING SETUP WITH SUPPLIES SHORTED

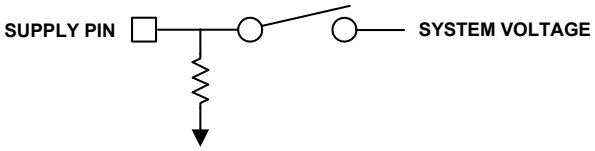


FIGURE 58. COLD SPARING SETUP WITH SUPPLIES FLOATING

ISL73841SEH vs ISL73840SEH

The ISL73840SEH, a 16-channel version of the ISL73841SEH, is available in a 28 Ld CDFP. The parts' performance specifications are very similar. Apart from the apparent increase in channel density, the ISL73841SEH has slightly higher output leakage compared to the ISL73840SEH because it has more channels connected to the output. The supply current for the ISL73841SEH is also slightly higher compared to the ISL73840SE. Refer to Table 1 on page 3 for a comparison of the two devices.

Die Characteristics

Die Dimensions

5000µm x 4080µm (197 mils x 161 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6×10^5 A/cm^2

TRANSISTOR COUNT

10752

Weight of Packaged Device

1.54 grams (typical)

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package Pin 29

Metalization Mask Layout

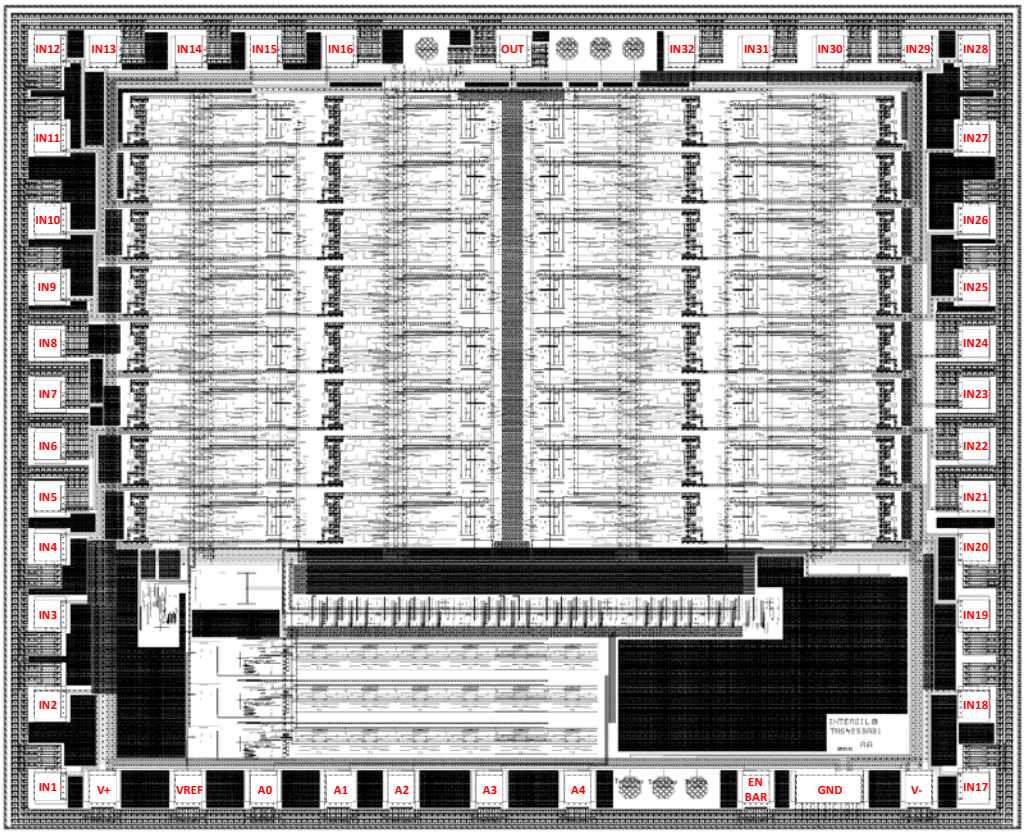


TABLE 3. ISL73841SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN28	P42	122	122	2232.2	1776.05
2	IN29	P43	122	122	1956.5	1772.2
3	IN30	P44	122	122	1529.15	1772.2
4	IN31	P45	122	122	1171.85	1772.2
5	IN32	P46	122	122	816.35	1772.2
9	OUT	P1	122	122	7.2	1773.25
11	IN16	P3	122	122.05	-829.525	1772.2
12	IN15	P4	122	122	-1192.2	1772.2
13	IN14	P5	122	122	-1553.65	1772.2
14	IN13	P6	122	122	-1965.35	1772.2
15	IN12	P7	122	122	-2232.2	1775.55
16	IN11	P8	122	122	-2232.2	1343.55
17	IN10	P9	122	122	-2232.2	944.5
18	IN9	P10	122	122	-2232.2	626.15
19	IN8	P11	122	122	-2232.2	354.4
20	IN7	P12	122	122.05	-2232.2	108.275
21	IN6	P13	122	122	-2232.2	-138.75
22	IN5	P14	122	122	-2232.2	-391.8
23	IN4	P15	122	122	-2232.2	-622.95
24	IN3	P16	122	122	-2232.2	-948.55
25	IN2	P17	122	122	-2232.2	-1379.95
26	IN1	P18	122	122	-2232.2	-1775.95
27	V^+	P19	122	122	-1970.75	-1789.2
28	VREF	P20	122	122	-1558.65	-1789.2
29	A0	P21	122	122	-1196.8	-1789.2
30	A1	P22	122	122	-835.6	-1789.2
31	A2	P23	122	122	-533	-1789.2
32	A3	P24	122	122	-109.45	-1789.2
33	A4	P25	122	122	313.95	-1789.2
37	EN_B	P28	122	122	1171.9	-1789.2
38	GND	P29, P29	320	122	1525.85	-1789.1
39	V^-	P30	122	122	1955.7	-1789.2
40	IN17	P31	122	122	2232.2	-1774.95
41	IN18	P32	122	122	2232.2	-1380.25
42	IN19	P33	122	122	2232.2	-947.45
43	IN20	P34	122	122	2232.2	-624.75
44	IN21	P35	122	122	2232.2	-391.95
45	IN22	P36	122	122	2232.2	-139.05
46	IN23	P37	122	122.05	2232.2	107.525

TABLE 3. ISL73841SEH DIE LAYOUT X-Y COORDINATES (Continued)

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
47	IN24	P38	122	122	2232.2	353.6
48	IN25	P39	122	122	2232.2	626.9
49	IN26	P40	122	122	2232.2	943.9
50	IN27	P41	122	122	2232.2	1342.7

NOTE: Origin of coordinates is the center of the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Feb 23, 2018	FN8846.3	Added “Considerations for Redundant Applications” section on page 19. Removed About Intersil section and added Renesas disclaimer.
Dec 7, 2017	FN8846.2	Added Related Literature section on page 1 Added Note 4 to Ordering Information on page 3 Added ESD circuit images in Figure 3 on page 4
May 31, 2016	FN8846.1	Added SMD in Features Updated Ordering Information table on page 3 Updated header in 1st and 2nd columns of “Electrical Specifications (±15V)” on page 5 and “Electrical Specifications (±12V)” on page 8 from “Parameter” and “Description” to “Symbol” and “Parameter”
May 13, 2016	FN8846.0	Initial release

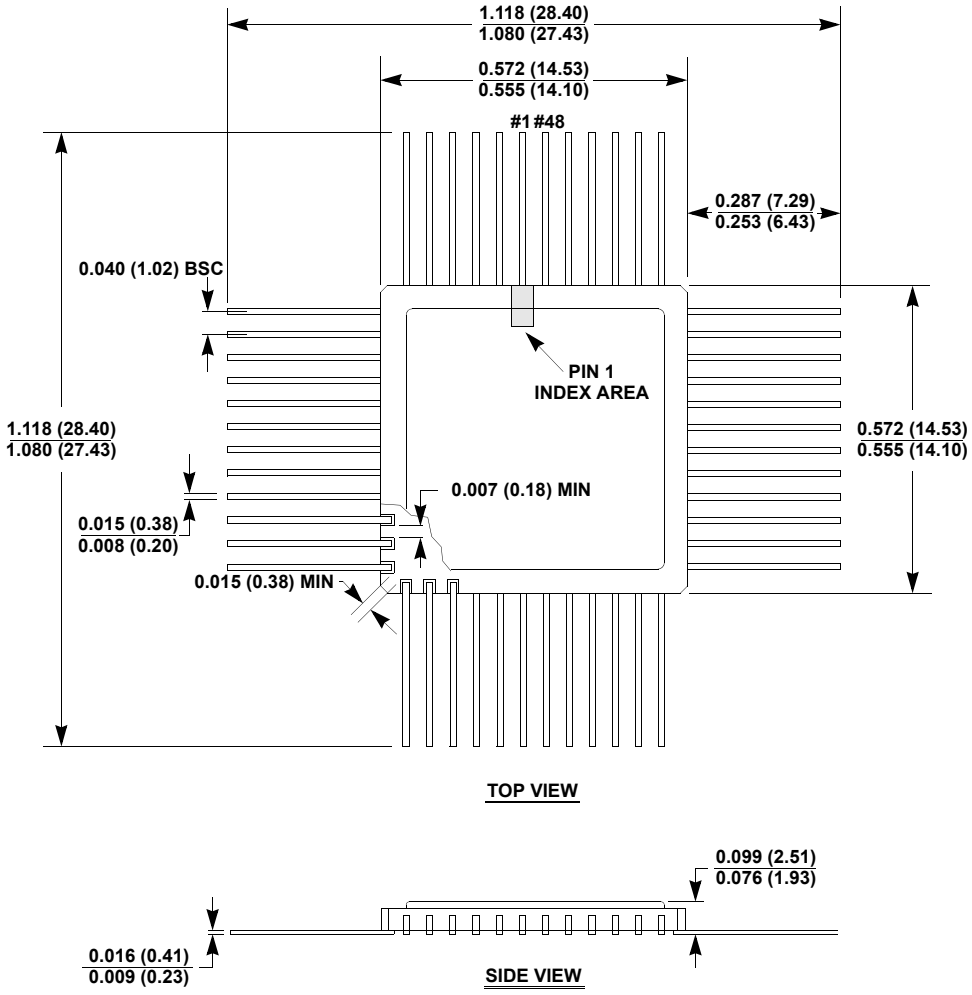
Package Outline Drawing

For the most recent package outline drawing, see R48.A.

R48.A

48 CERAMIC QUAD FLATPACK PACKAGE (CQFP)

Rev 3, 10/12



NOTE:

1. **All dimensions are in inches (millimeters).**

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(Rev.4.0-1 November 2017)

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