ISL78113A

Low Input Voltage and High Efficiency Synchronous Boost Converter with 1.3A Switch

FN8638
Rev 0.00
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The ISL78113A provides a tiny and convenient boost power supply solution to generate a regulated output up to 500mA from any sub-5V secondary rail found in an automotive electrical system, including battery powered applications (NiCd, NiMH, or one-cell Li-Ion/Li-Polymer). It offers an adjustable output (3.0V to 5.2V) supporting USB-OTG or HDMI applications. The device is able to supply 500mA from a 3V input and 5V output, and has a typical 1.3A peak current limit.

The ISL78113A is a fully integrated, internally compensated, synchronous converter optimized to maximize efficiency and reduce the overall solution size and bill of materials. Its high 2MHz switching frequency allows the use of tiny, low-profile inductors and chip capacitors. It also eliminates potential interference within the AM radio band and the external EMI filtering needed for converters switching at lower rates. To minimize power consumption while off, the device features an ultra-low current shutdown mode dropping quiescent current to 50nA typical.

ISL78113A is supplied in an 8 Ld DFN package. The device is rated to operate over the temperature range of -40°C to +105°C.

Features

- Output disconnect during shutdown preventing output precharging and uncontrolled short-circuit current
- Input voltage range: 0.8V to 4.7V
- Output current: Up to 500mA (V_{BAT} = 3V, V_{OUT} = 5V)
- Logic control shutdown (I_Q < 1µA)
- 2MHz switching frequency
- Up to 95% efficiency at typical operating conditions
- Fault protection: OVP, OCP, OTP, UVLO
- 2mmx2mm 8 Ld DFN package
- Qualified for automotive operations

Applications

- Automotive head units and infotainment systems: especially those including portable HDMI and USB-OTG connectivity
- Automotive camera systems

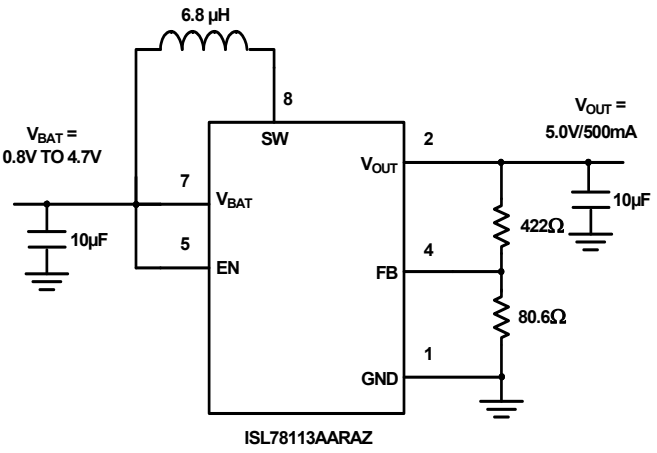


FIGURE 1. TYPICAL APPLICATION

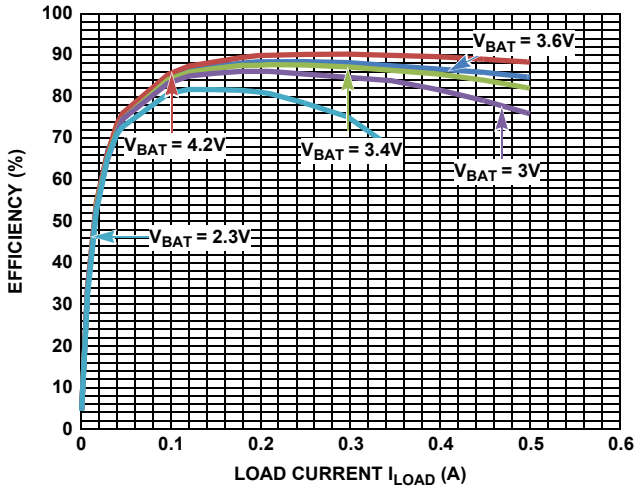
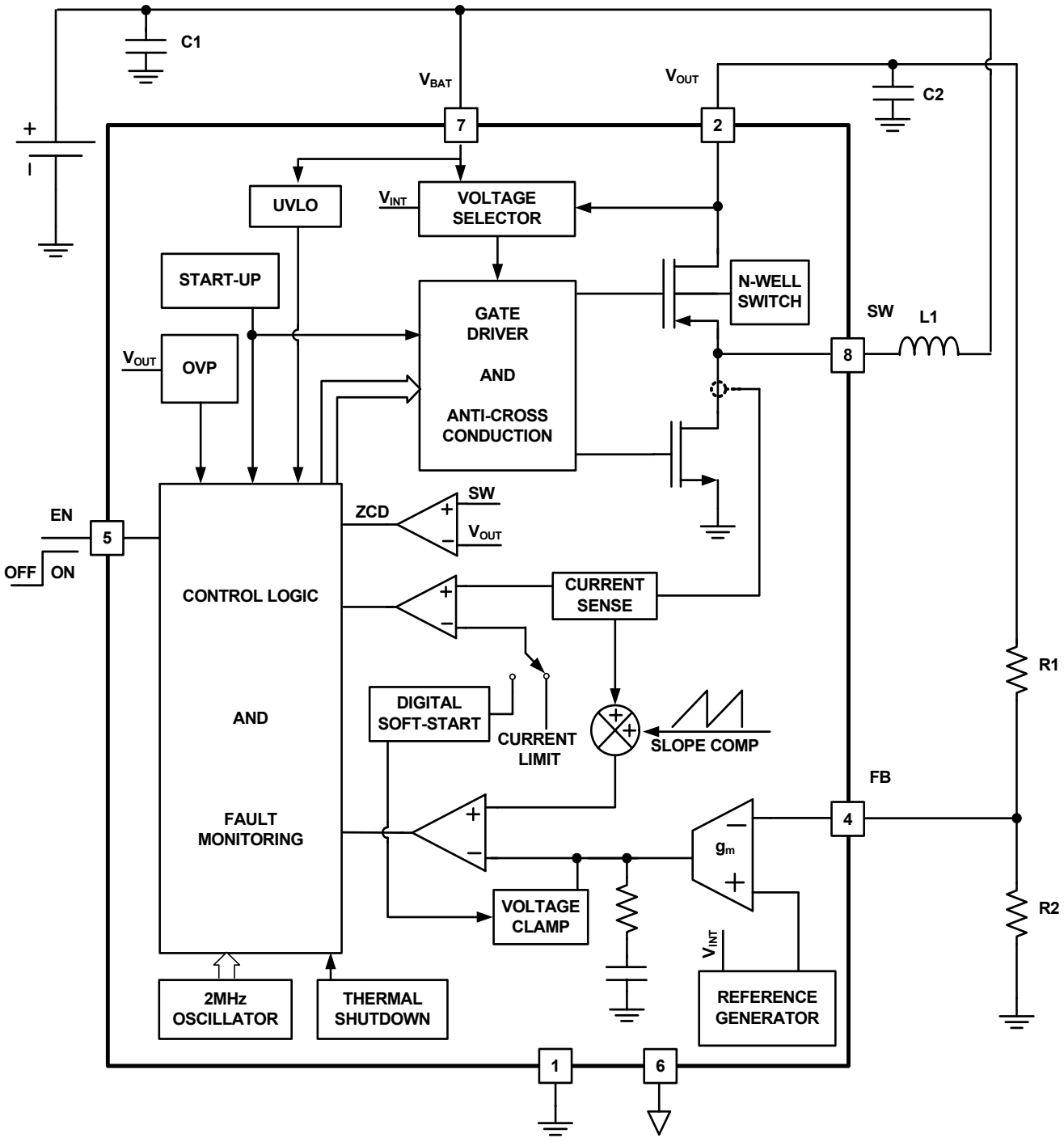


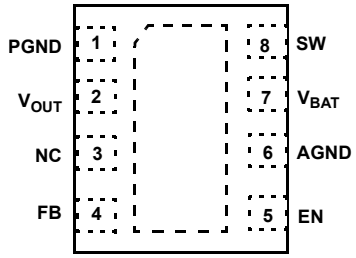
FIGURE 2. EFFICIENCY vs LOAD CURRENT

Block Diagram



Pin Configuration

ISL78113A
ADJUSTABLE OUTPUT
(8 LD DFN)
TOP VIEW



Pin Descriptions

PIN NUMBERS	SYMBOL	PIN DESCRIPTION
1	PGND	Power ground.
2	V_{OUT}	Device output.
3	NC	No connection.
4	FB	Feedback pin of the converter. Connect voltage divider resistors between V_{OUT}, FB and GND for desired output.
5	EN	The EN pin is an active-HIGH logic input for enabling the device. When asserted HIGH, the boost function begins. When driven LOW, the device is completely disabled, and current is blocked from flowing from the SW pin to the output and vice versa. This pin may be tied either HIGH to enable the device or LOW to disable.
6	AGND	Analog ground.
7	V_{BAT}	Device input supply from a battery. Connect a 10µF ceramic capacitor from VBAT to power ground.
8	SW	The SW pin is the switching node of the power converter. Connect one terminal of the inductor to the SW pin and the other to power input.
	EPAD	The exposed pad must be connected to PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the system GND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{OUT} (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL78113AARAZ-T	AAR	Adjustable	-40 to +105	8 Ld DFN	L8.2x2D

NOTES:

1. Use “-T7A” suffix for 250 pieces tape and reel. Please refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78113A. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

V_{BAT}, EN, V_{OUT} . . . . . -0.3V to 6.5V
SW Voltage
DC . . . . . -0.5V to 6.5V
Pulse <10ns . . . . . -0.5V to 8.0V
ESD Ratings
Human Body Model (Tested per AEC-Q100-002) 4kV
Machine Model (Tested per AEC-Q100-003) 300V
Charged Device Model (Tested per AEC-Q100-011) 2.2kV
Latch Up (Tested per AEC-Q100-004; Class II, Level A) 15mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld DFN Package (Notes 4, 5)	80	15

Maximum Junction Temperature (plastic package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile TB493

Recommended Operating Conditions

V_{BAT} (after start-up) . . . . . 0.8V to 4.7V
V_{OUT} . . . . . (V_{BAT} + 0.2V) to 5.2V
Operating Junction Temperature Range . . . . . -40°C to +125°C
Ambient Temperature Range . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC} the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{BAT} = 3.0V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Start-up Voltage	V_{MIN}	V_{EN} = 1.2V, R_{LOAD} = 50Ω	**0.6**	0.75	**0.9**	V
Input Undervoltage Lockout	V_{UVLO}	V_{EN} = V_{BAT}, R_{LOAD} = 50Ω	**0.66**	0.70	**0.76**	V
Feedback Voltage	V_{FB}		**784**	800	**816**	mV
Output Voltage		V_{BAT} = 2V	**3.0**		**5.2**	V
Feedback Pin Input Current			**-100**		**100**	nA
Quiescent Current from V_{OUT}	I_{Q1}	V_{BAT} = V_{EN} = 1.2V, no load (Note 7)		5.5	**10**	mA
Shutdown Current from V_{BAT}	I_{SD}	V_{EN} = 0V, V_{BAT} = 1.2V, V_O = 0		0.05	**2.8**	µA
Leakage Current at SW Pin		V_{EN} = 0V, V_{BAT} = 4.7V, V_O = 0			**15**	µA
N-Channel MOSFET ON-resistance				0.20		Ω
P-Channel MOSFET ON-resistance				0.35		Ω
N-Channel MOSFET Peak Current Limit	I_{PK}		**1**	1.3	**1.6**	A
Maximum Duty Cycle	D_{MAX}		**82**	87.5		%
PWM Switching Frequency	F_{OSC}		**1.73**	2	**2.23**	MHz
EN Logic High		2.5V < V_{BAT} < 4.7V	**1.2**			V
		V_{BAT} < 2.5V	**0.48*V_{BAT}**			V
EN Logic Low		2.5V < V_{BAT} < 4.7V			**0.35**	V
		V_{BAT} < 2.5V			**0.14*V_{BAT}**	V
Soft Start-up Time		C_{OUT} = 4.7µF, L = 4.7µH		0.2	**1**	ms
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	I_{LOAD} = 1 to 50mA	**-0.5**	±0.01	**0.5**	%
Line Regulation		V_{BAT} = 3.0V to 3.6V, I_{LOAD} = 1mA	**-0.5**	±0.03	**0.5**	%
Minimum SW Low in PWM Mode	$t_{MIN(ON)}$			42	**49**	ns
Output Overvoltage Protection Threshold				5.9		V
Thermal Shutdown	T_{SD}			150		°C
Thermal Shutdown Hysteresis				25		°C

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. I_{Q1} is measured at V_{OUT} and multiplied by V_{OUT}/V_{BAT}; thus, the equivalent input quiescent current is calculated.

Detailed Description

Current Mode PWM Operation

The control scheme of the device is based on the peak current mode control and the control loop is compensated internally. The peak current of the N-channel MOSFET switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical current limit is set to 1.3A.

The control circuit includes a current ramp generator, slope compensator, error amplifier and a PWM comparator (see the "Block Diagram" on page 2). The ramp signal is derived from the inductor current. This ramp signal is then compared to the error amplifier output to generate the PWM gating signals for driving both N-channel and P-channel MOSFETs. The PWM operation is initialized by the clock from the internal oscillator (typical 2MHz). The N-channel MOSFET is turned ON at the beginning of a PWM cycle, the P-channel MOSFET remains OFF, and the current starts ramping up. When the sum of the ramp and the slope compensator output reaches the error amplifier output voltage, the PWM comparator outputs a signal to turn OFF the N-channel MOSFET. Here, both MOSFETs remain OFF during the dead-time interval. Next, the P-channel MOSFET is turned ON and remains ON until the end of this PWM cycle. During this time, the inductor current ramps down until the next clock. At this point, following a short dead time, the N-channel MOSFET is again turned ON, repeating as previously described.

Synchronous Rectifier

The ISL78113A integrates one N-channel MOSFET and one P-channel MOSFET to realize a synchronous boost converter. Because the commonly used discrete Schottky rectifier is replaced with the low $r_{DS(ON)}$ P-channel MOSFET, the power conversion efficiency reaches a value above 90%.

V_{OUT} Isolation

Since a typical step-up converter has a conduction path from the input to the output via the body diode of the P-channel MOSFET, a special circuit (see the "Block Diagram" on page 2) is used to reverse the polarity of the P-channel body diode when the device is shut down. Thus, this configuration completely disconnects the load from the input during shutdown of the converter. The benefit of this feature is that the battery will not be completely depleted during shutdown of the converter. No additional components are needed to disconnect the battery from the output of the converter.

Soft-Start

The soft start-up duration is the time between the device being enabled and V_{OUT} rising to within 3% of the target voltage. When the device is enabled, the start-up cycle starts with a linear operating phase. During the linear phase, the rectifying switch is turned ON in a current limited configuration, delivering about 350mA, until the output capacitor is charged to approximately 90% of the input voltage. At this point, PWM operation begins in boost mode. If the output voltage is below 2.3V, PWM switching is done at a fixed duty-cycle of 75% until the output voltage reaches 2.3V. When the output voltage exceeds 2.3V, the closed-loop current mode PWM loop overrides the duty cycle until the output voltage is regulated. Peak inductor current is ramped to the current limit value (typically 1.3A) during the soft-start period to limit in-rush current from the input source. Fault monitoring begins approximately 2ms after the device is enabled.

To start up with a slow V_{BAT} ramp-up rate is likely to cause the device to enter hiccup mode. This is a result of the input voltage dropping due to start-up current, which causes a fault of V_{OUT} out of regulation, especially at high load and cold temperature. Check the input ramp-up rate and a faster input slew rate would help to resolve this.

Over-temperature Protection (OTP)

The device offers over-temperature protection. A temperature sensor circuit is integrated and monitors the internal IC temperature. Once the temperature exceeds the preset threshold (typically +150°C), the IC shuts down immediately. The OTP has a typical hysteresis of +25°C. When the device temperature decreases by this, the device starts operating.

TABLE 1. FAULT DETECTION AND RESPONSE

FAULT CONDITION	DETECTION DETAILS	ACTION
Low Battery Voltage	V_{BAT} < 0.7V	Shutdown until V_{EN} or V_{BAT} is cycled.
V_{OUT} Out of Regulation	V_{OUT} is 10% below the target output voltage.	Shutdown only if V_{BAT} and V_{OUT} fall below 2.1V. Device automatically restarts after 200ms.
Short Circuit	V_{OUT} falls below V_{BAT}.	Shutdown immediately. Device automatically restarts after 200ms.
Over-temperature Protection	Die temperature is > +150°C.	Switching stops. Device automatically restarts when temperature decreases to +125°C.
Output Overvoltage Protection	V_{OUT} > 5.9V	Switching stops until EN pin is toggled or power is cycled.

Fault Monitoring

Fault monitoring starts 2ms after start-up. Table 1 shows the response to different detected faults.

Printed Circuit Board Layout Recommendations

The ISL78113A is a high frequency switching boost converter. Accordingly, the converter has fast voltage change and high switching current that may cause EMI and stability issues if the layout is not done properly. Therefore, careful layout is critical to minimize the trace inductance and reduce the area of the power loop.

Power components such as input capacitor, inductor, and the output capacitors should be placed as close to the device as possible. Board traces that carry high switching current should be routed wide and short. A solid power ground plane is important for EMI suppression.

The switching node (SW pin) of the converter and the traces connected to this pin are very noisy. Noise sensitive traces such as the FB trace should be kept away from the SW node. The voltage divider should be placed close to the FB pin to prevent noise pickup. Figure 3 shows the recommended PCB layout.

In the 8 Ld DFN package, the heat generated in the device is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. It is recommended to add at least 4 vias within the pad to the GND plane for the best thermal dissipation.

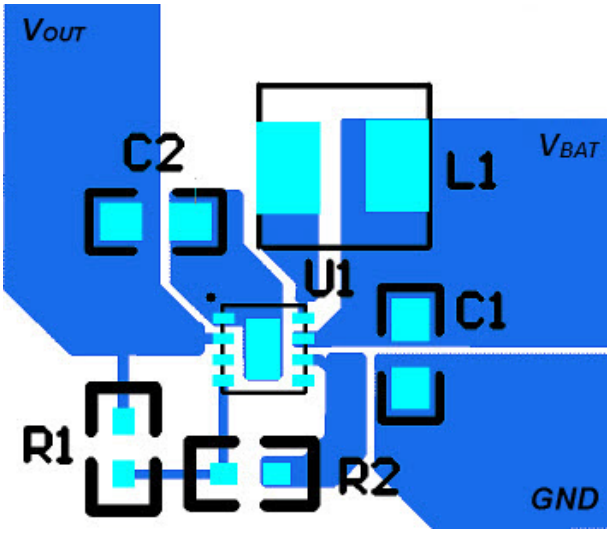


FIGURE 3. RECOMMENDED PCB LAYOUT

Output Voltage Setting Resistor Selection

For ISL78113A, resistors R_1 and R_2, shown in the “Block Diagram” on page 2, set the desired output voltage values. The output voltage can be calculated using Equation 1:

$$V_{OUT} = V_{FB} \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

where V_{FB} is the internal FB reference voltage (0.8V typical). The current flowing through the divider resistors is calculated as $V_{OUT}/(R_1 + R_2)$. The resistance is chosen based on the minimum expected load for V_{OUT} and the minimum PWM on time (PWM Low; 42ns typical). This will provide a small constant current that limits the V_{OUT} and voltage in light load conditions. R_1 and R_2 should be placed close to the FB pin of the device to prevent noise pickup.

Inductor Selection

An inductor with core material suitable for high frequency applications (e.g., ferrite) is desirable to minimize core loss and improve efficiency. The inductor should have a low DCR to reduce copper loss. Moreover, the inductor saturation current should be higher than the maximum peak current of the device; i.e., 1.6A.

The device is designed to operate with an inductor value of 2.2µH to 6.8µH to provide stable operation across the range of load, input and output voltages. Table 2 shows recommended inductors.

TABLE 2. INDUCTOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
Würth Elektronik	WE-TPC, Type S	www.we-online.com

Capacitor Selection

INPUT CAPACITOR

A minimum of a 10µF ceramic capacitor is recommended to provide stable operation under typical operating conditions. For input voltage less than 1.0V application, an additional 2.2µF ceramic capacitor is recommended for better noise filtering and EMI suppression. The input capacitor should be placed close to the input pin, GND pin, and the non-switching terminal of the inductor.

OUTPUT CAPACITOR

For the output capacitor, a ceramic capacitor with small ESR is recommended to minimize output voltage ripple. A typical 10µF should be used to provide stable operation at different typical operating conditions. The output capacitor should be placed close to the output pin and GND pin of the device. Table 3 shows the recommended capacitors.

TABLE 3. CAPACITOR VENDOR INFORMATION

MANUFACTURER	SERIES	WEBSITE
AVX	X7R	www.avx.com
Murata	X7R	www.murata.com
Taiyo Yuden	X7R	www.t-yuden.com
TDK	X7R	www.tdk.com

Forced PWM Operation

The part has forced PWM operation. During a no-load condition the low-side FET is forced ON for a short pulse with minimum ON-time (42ns typical) in every cycle and does not allow for pulse skipping. The part is also implemented with diode emulation mode to turn off the upper side MOSFET when inductor current drops to 0 and prevents any negative inductor current. Therefore in no load to light load (less than several mA) conditions, the output voltage is pushed higher than regulation point, which may be out of the user's output voltage specifications.

This issue can be resolved by adding a small load (several mA) to keep the output in regulation. The procedure to calculate the minimum load required due to these forced PWM pulses is elaborated in the following.

Figure 4 shows the inductor waveform in the forced PWM operation at no load. $t_{MIN(ON)\_LFET}$ is the time the low-side MOSFET is forced ON.

During $t_{MIN(ON)}$ time, inductor current is charged with slew rate of V_{IN}/L. The peak inductor current at the end of $t_{MIN(ON)}$ can be calculated in Equation 2.

$$IL_{peak} = \frac{V_{IN} \bullet t_{MIN(ON)}}{L} \quad \text{(EQ. 2)}$$

After $t_{MIN(ON)}$ time, low-side MOSFET is turned off, inductor current is free-wheeling through the high-side MOSFET from V_{IN} to V_{OUT} until the inductor current ramps down to 0 and the high-side MOSFET is turned off. The duration of this free-wheeling period (t_{FW}) can be calculated in Equation 3.

$$t_{FW} = \frac{IL_{peak} \bullet L}{V_{OUT} - V_{IN}} \quad \text{(EQ. 3)}$$

During this free-wheeling period, the charge to the output is shown as Q in Figure 4 on page 8, which can be calculated as shown by Equation 4.

$$Q = 0.5 \bullet IL_{peak} \bullet t_{FW} \quad \text{(EQ. 4)}$$

The ISL78113A outputs charge of Q to the output every switching cycle, therefore the average current to due to the $t_{MIN(ON)}$ pulses can be calculated as shown by Equation 5.

$$I_{OUT(AVG)} = Q \bullet F_{SW} \quad \text{(EQ. 5)}$$

where F_{SW} is the switching frequency.

Summarizing from Equations 2 through 5, the average current charged to the output due to the $t_{MIN(ON)}$ pulses can be calculated by Equation 6.

$$I_{OUT(AVG)} = \frac{0.5 \bullet F_{SW} \bullet (V_{IN} \bullet t_{MIN(ON)})^2}{L \bullet (V_{OUT} - V_{IN})} \quad \text{(EQ. 6)}$$

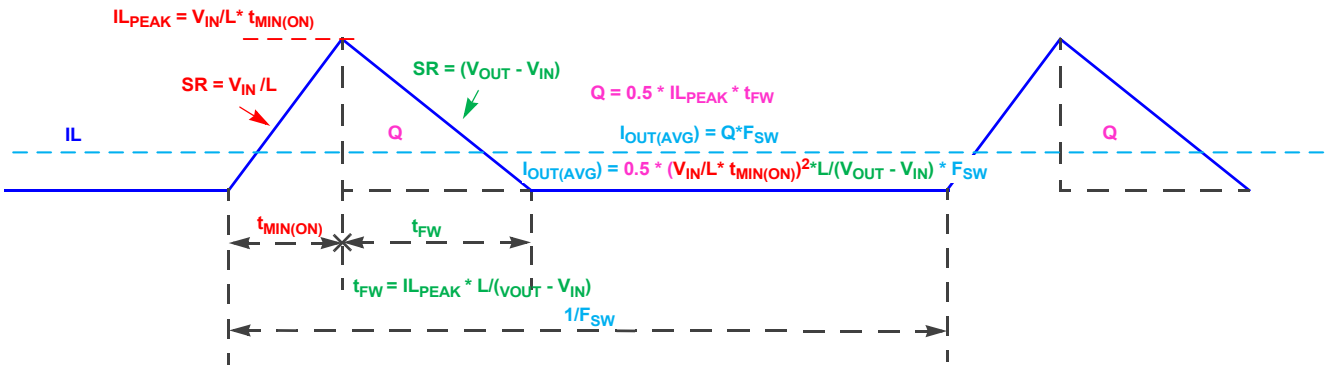


FIGURE 4. AVERAGE OUTPUT CURRENT DUE TO FORCED PWM PULSES AT NO LOAD CONDITION

Minimum Load Required in Forced PWM Mode

In a no load condition, in order to maintain the output voltage in regulation, a small load has to be added in the output to absorb the output current due to forced PWM pulses. Equation 6 can be used to calculate the minimum required load in worst cases.

The worst cases refer to F_{SW}, V_{IN}, $t_{MIN(ON)}$, L, V_{OUT} in Equation 6.

- Use the maximum V_{IN} for the worst case.
- Specify the allowed maximum Vout voltage $V_{IN(MAX)}$ and use it in the worst case calculation, basically the target is to have the minimum load keeping the V_{OUT} below the maximum acceptable voltage.
- Use the maximum switching frequency of 2.23MHz specified in the “Electrical Specifications” table on page 4. Maximum frequency is the worst case since it delivered most pulses with fixed charges to the output.
- Use the minimum inductor value considering inductance variations (normally -20% of nominal value). For the inductor selection, note the higher the inductance, the less the required minimum load.
- Use the maximum $t_{MIN(ON)}$ time of 49ns specified in the “Electrical Specifications” table on page 4. Maximum $t_{MIN(ON)}$ time is the worst case since it cause higher inductor peak current and higher charge to the output.

An example of the typical conditions are listed as follows:

- V_{IN} TYP = 3V
- V_{OUT} TYP = 5V
- F_{SW} TYP = 2MHz
- $L_{NOMINAL}$ = 6.8µH

To calculate the minimum required load, the worst conditions we can use are,

- $V_{IN(MAX)}$ = 3.6V (specified in customer system)
- $V_{OUT(MAX)}$ = 5.25V (specified in customer system)
- F_{SW} = 2.23MHz
- L_{MIN} = (-20%) $L_{NOMINAL}$ = 5.44µH

Using the above worst case parameters in Equation 6, the calculated output current ($I_{OUT(AVG)}$) is 3.87mA, which is the minimum required load to be added in the output to absorb the output current due to forced PWM pulses. Extra margin can be added depending on the system worst case condition.

Typical Characteristics

V_{IN} = 3.4V, V_{OUT} = 5V, L = 6.8µH, C_{OUT} = 10µF, R_1 = 422Ω, R_2 = 80.6Ω; unless otherwise noted.

Typical values are at T_A = +25°C.

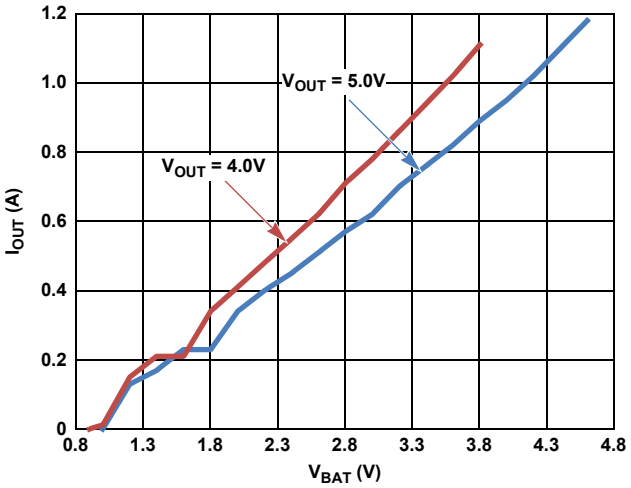


FIGURE 5. MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

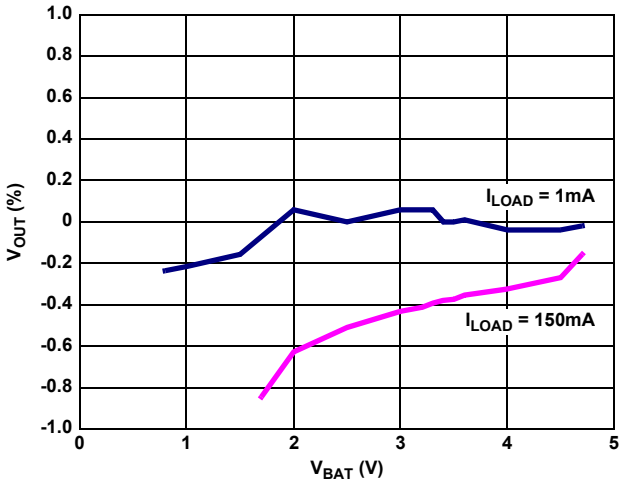


FIGURE 6. LINE REGULATION, V_{OUT} = 5V

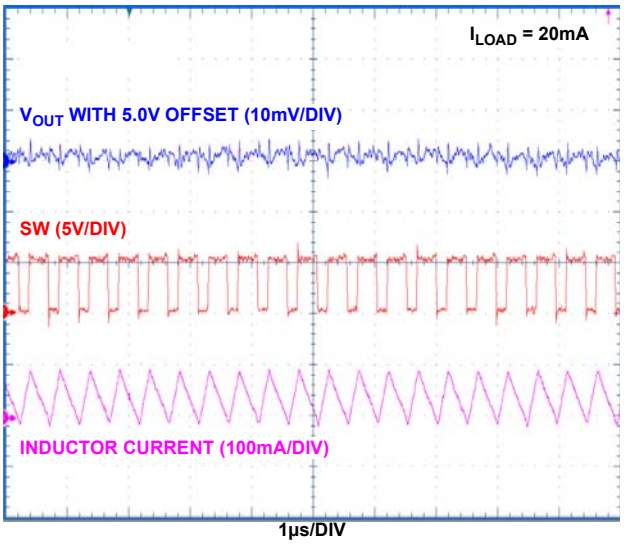


FIGURE 7. OUTPUT RIPPLE VOLTAGE (I_{LOAD} = 20mA)

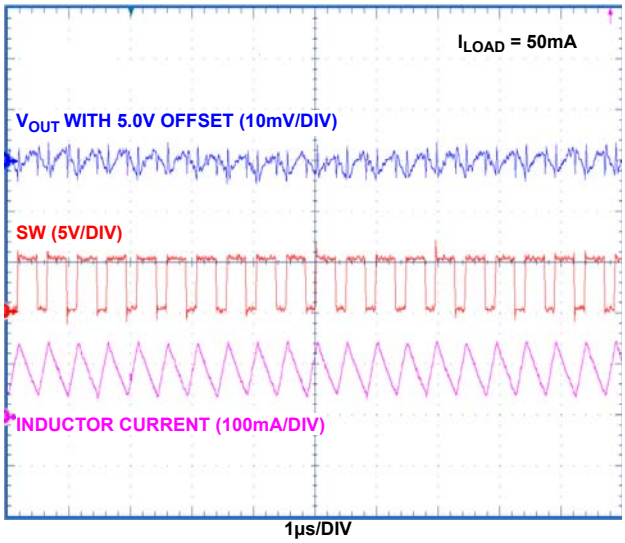


FIGURE 8. OUTPUT RIPPLE VOLTAGE (I_{LOAD} = 50mA)

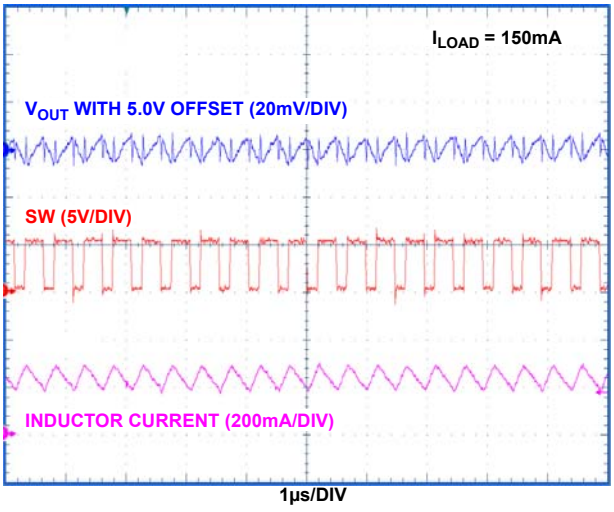


FIGURE 9. OUTPUT RIPPLE VOLTAGE (I_{LOAD} = 150mA)

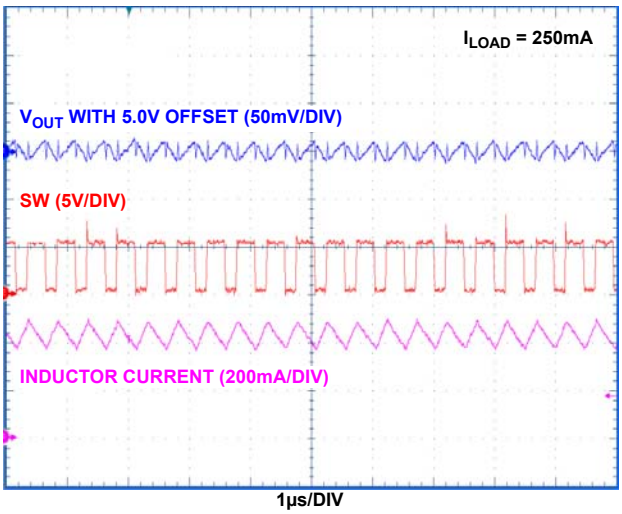


FIGURE 10. OUTPUT RIPPLE VOLTAGE (I_{LOAD} = 250mA)

Typical Characteristics

V_{IN} = 3.4V, V_{OUT} = 5V, L = 6.8µH, C_{OUT} = 10µF, R_1 = 422Ω, R_2 = 80.6Ω; unless otherwise noted.

Typical values are at T_A = +25°C. **(Continued)**

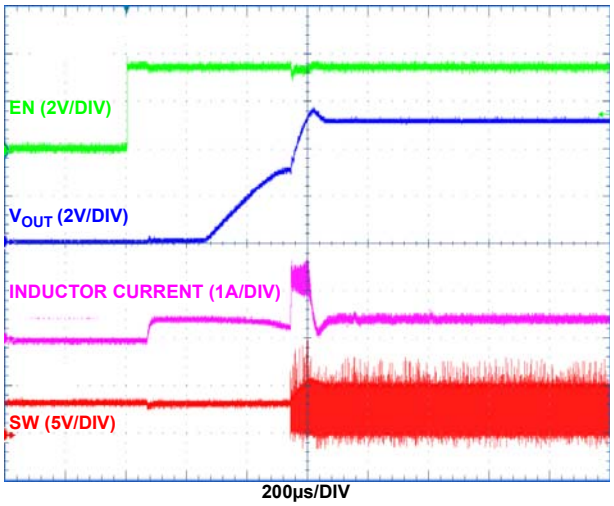


FIGURE 11. START-UP AFTER ENABLE (I_{LOAD} = 250mA)

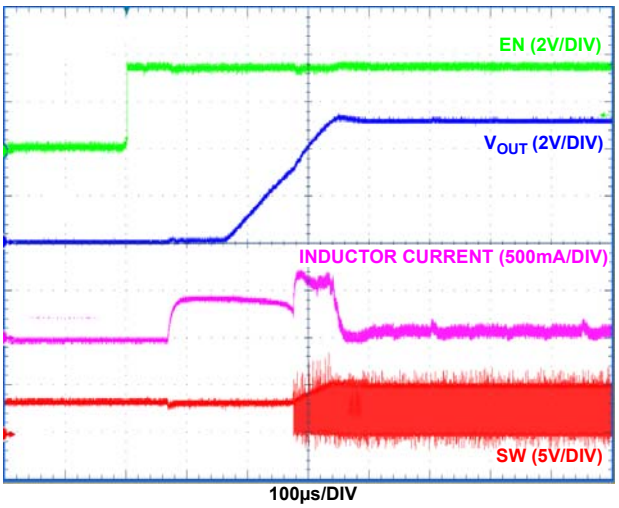


FIGURE 12. START-UP AFTER ENABLE (I_{LOAD} = 50mA)

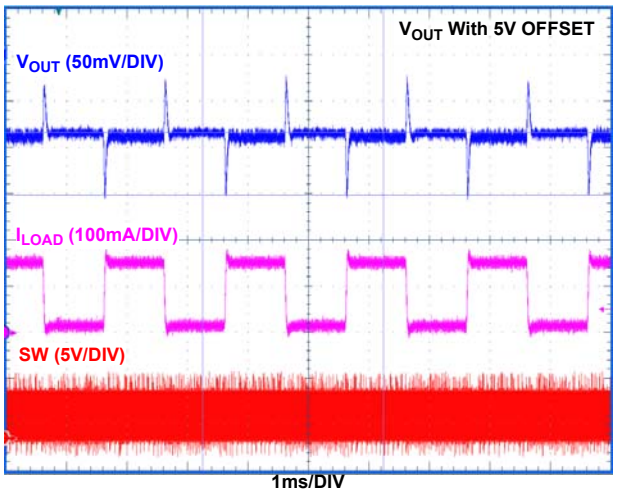


FIGURE 13. LOAD TRANSIENT RESPONSE (20mA TO 150mA)

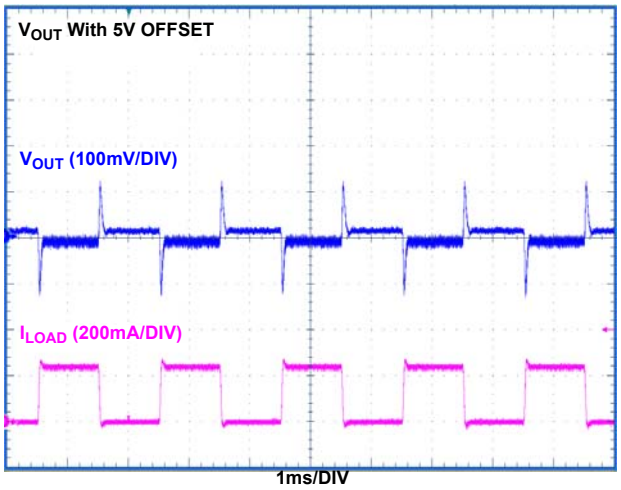


FIGURE 14. LOAD TRANSIENT RESPONSE (20mA TO 250mA)

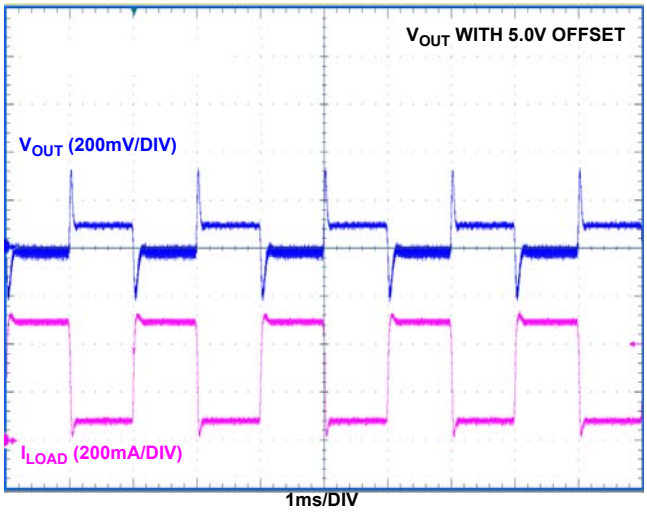


FIGURE 15. LOAD TRANSIENT RESPONSE (100mA TO 500mA)

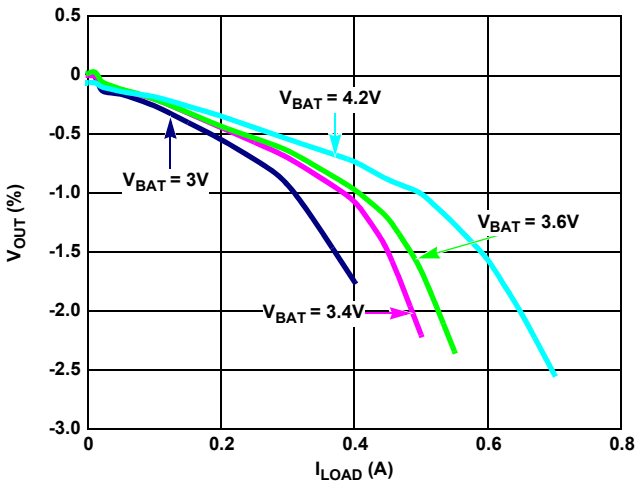


FIGURE 16. LOAD REGULATION

Typical Characteristics

V_{IN} = 3.4V, V_{OUT} = 5V, L = 6.8µH, C_{OUT} = 10µF, R_1 = 422Ω, R_2 = 80.6Ω; unless otherwise noted.

Typical values are at T_A = +25°C. **(Continued)**

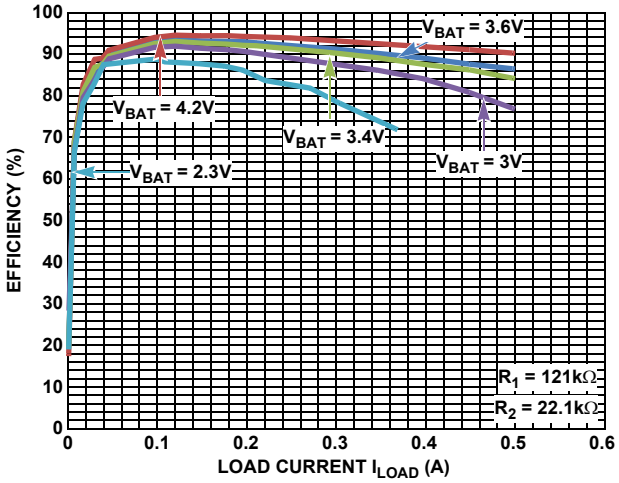


FIGURE 17. EFFICIENCY vs LOAD CURRENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 1, 2014	FN8638.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

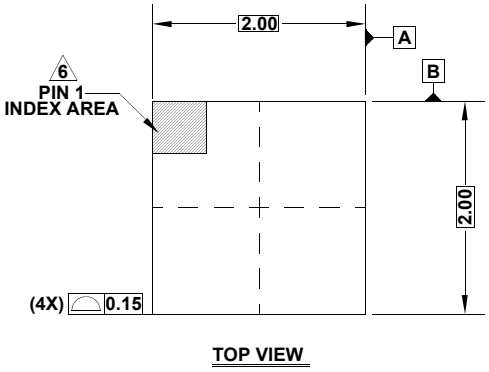
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

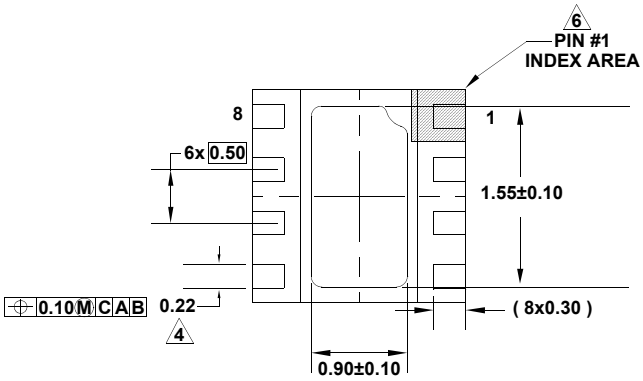
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

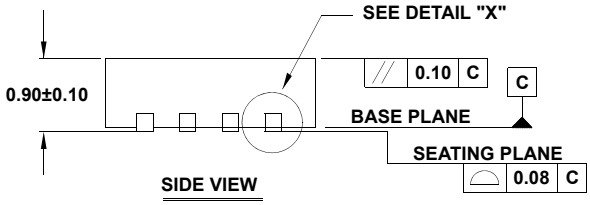
Rev 0, 3/11



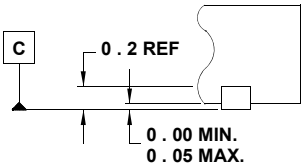
TOP VIEW



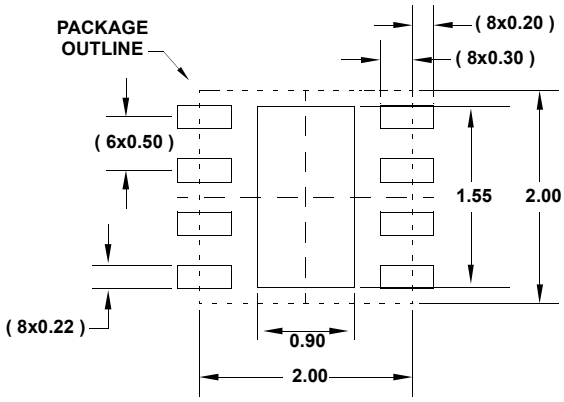
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.