ISL9216, ISL9217

8 to 12 Cell Li-Ion Battery Overcurrent Protection and Analog Front End Chip Set

FN6488
Rev 1.00
November 2, 2007

The ISL9216 and ISL9217 chipset provides overcurrent protection and voltage monitoring for multi-cell li-ion battery packs consisting of 8 to 12 cells. When used together, these devices provide integrated overcurrent protection circuitry, short circuit protection, an internal voltage regulator, internal cell balancing switches, cell voltage level shifters, and drive circuitry for external FET devices that control pack charge and discharge. Level shifting of the analog output voltage from the upper cells and communication between the chips is handled automatically.

Overcurrent and short circuit thresholds reside in internal RAM registers and are selected independently via software using an I^2C serial interface. Detection and time-out delays can be individually varied using internal registers.
Using an internal analog multiplexer, the device provides monitoring of cell voltage by a separate microcontroller with A/D converter. Software on this microcontroller implements all battery control functionality, except for overcurrent and short circuit shutdown.

Applications

- Power Tools
- Battery Backup Systems
- E-bikes
- Portable Test Equipment
- Medical Systems
- Hybrid Vehicle
- Military Electronics

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9216IRZ*	ISL9216 IRZ	32 Ld 5x5 QFN	L32.5x5B
ISL9217IRZ*	921 7IRZ	24 Ld 4x4 QFN	L24.4x4D

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

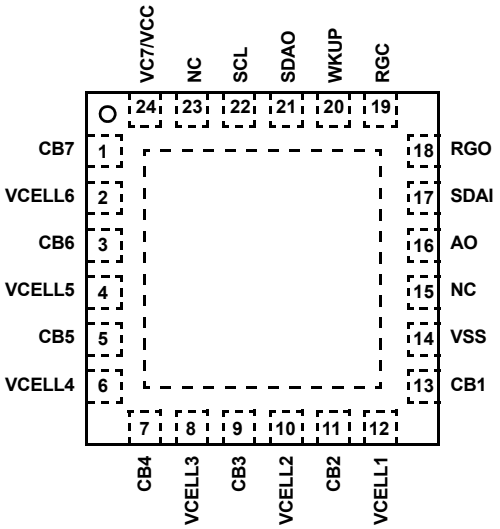
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

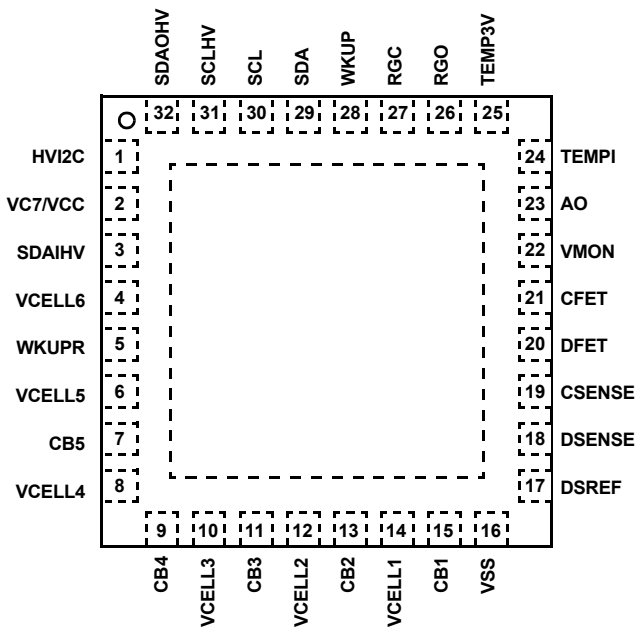
- Software selectable overcurrent protection levels and variable protect detection/release times
  - 4 Discharge overcurrent thresholds
  - 4 Short circuit thresholds
  - 4 Charge overcurrent thresholds
  - 8 Overcurrent delay times (Charge)
  - 8 Overcurrent delay times (Discharge)
  - 2 Short circuit delay times (Discharge)
- Automatic FET turn-off and cell balance disable on reaching external (battery) or internal (IC) temperature limit
- Automatic over-ride of cell balance on reaching internal (IC) temperature limit
- Fast short circuit pack shutdown
- Can use current sense resistor, FET $r_{DS(ON)}$, or Sense FET for overcurrent detection
- Four battery backed software controlled flags
- Allows three different FET controls:
  - Back-to-back N-Channel FETs for charge and discharge control
  - Single N-Channel FET for discharge control
  - N-Channel FET for discharge, with separate, optional (smaller) back-to-back FET for charge
- Chips cascade for packs of 8 to 12 cells
- Integrated charge/discharge FET drive circuitry with 200µA (typ) turn on current and 150mA (typ) discharge FET turn off current
- 10% accurate 3.3V voltage regulator (35mA out with external NPN transistor having current gain of 70)
- Cell voltage monitor accurate to within 25mV
- Monitored cell voltage output stable in 100µs
- Internal cell balancing FETs handle up to 200mA of balancing current for each cell (with the number of cells being balanced limited by the maximum power dissipation of 400mW)
- Simple I^2C host interface
- Sleep operation with programmable negative edge or positive edge wake-up
- <10µA sleep mode
- Pb-free (RoHS compliant)

Pinouts

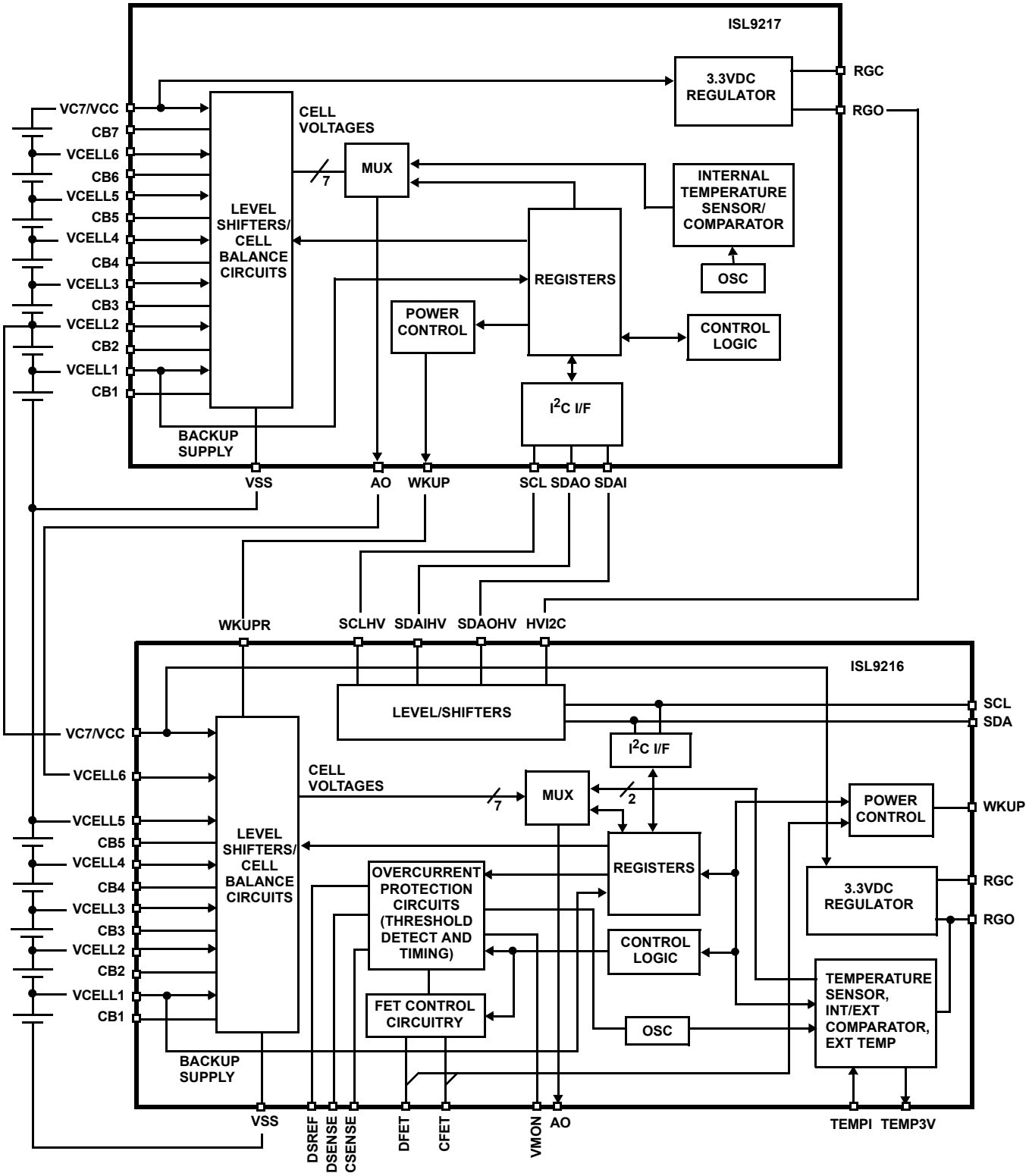
ISL9217 (UPPER)
(24 LD 4X4 QFN)
TOP VIEW



ISL9216 (LOWER)
(32 LD 5X5 QFN)
TOP VIEW



Functional Diagram



Pin Descriptions

SYMBOL	DESCRIPTION
VC7/VCC	**Battery Cell 7 Voltage Input/VCC Supply.** This pin is used to monitor the voltage of this battery cell externally at pin AO. This pin also provides the operating voltage for the IC circuitry.
VCELLN	**Battery Cell N Voltage Input.** This pin is used to monitor the voltage of this battery cell externally at pin AO. VCELLN connects to the positive terminal of CELLN and the negative terminal of CELLN+1.
CBN	**Cell Balancing FET Control Output N.** This internal FET diverts a fraction of the current around a cell while the cell is being charged or adds to the current pulled from a cell during discharge in order to perform a cell voltage balancing operation. This function is generally used to reduce the voltage on an individual cell relative to other cells in the pack. The cell balancing FETs are turned on or off by an external controller.
VSS	**Ground**. This pin connects to the most negative terminal in the battery string.
DSREF	**Discharge Current Sense Reference (ISL9216 only).** This input provides a separate reference point for the charge and discharge current monitoring circuits. with a separate reference connection, it is possible to minimize errors that result from voltage drops on the ground lead when the load is drawing large currents. If a separate reference is not necessary, connect this pin to VSS.
DSENSE	**Discharge Current Sense Monitor (ISL9216 only).** This input monitors the discharge current by monitoring a voltage. It can monitor the voltage across a sense resistor, or the voltage across the DFET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to DSREF.
CSENSE	**Charge Current Sense Monitor (ISL9216 only).** This input monitors the charge current by monitoring a voltage. It can monitor the voltage across a sense resistor, or the voltage across the CFET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to VSS.
DFET	**Discharge FET Control (ISL9216 only).** The ISL9216 controls the gate of a discharge FET through this pin. The power FET is a N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL9216 can also turn off the FET in the event of an overcurrent or short circuit condition. If the microcontroller detects an undervoltage condition on any of the battery cells, it will turn off the FET off by controlling this output with a control bit.
CFET	**Charge FET Control (ISL9216 only).** The ISL9216 controls the gate of a charge FET through this pin. The power FET is a N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL9216 can also turn off the FET in the event of an overcurrent condition. If the microcontroller detects an overvoltage condition on any of the battery cells, it will turn off the FET off by controlling this output with a control bit.
VMON	**Discharge Load Monitoring (ISL9216 only).** In the event of an overcurrent or short circuit condition, the microcontroller can enable a series diode and resistor that connects between the VMON pin and VSS. When FETs open because of an overcurrent or short circuit condition, and the load remains, the voltage at VMON will be near the VCC voltage. When the load is released, the voltage at VMON drops below a threshold indicating that the overcurrent or short circuit condition is resolved. At this point, the LDFAIL flag is cleared and operation can resume.
AO	**Analog Multiplexer Output.** The analog output pin is used by an external microcontroller to monitor the cell voltages and temperature sensor voltages. The microcontroller selects the specific voltage being applied to the output by writing to a control register.
TEMP3V	**Temperature Monitor Output Control (ISL9216 only).** This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the cells. The TEMP3V output is connected internally to the RGO voltage through a PMOS switch only during a measurement of the temperature, otherwise the output is off. The TEMP3V output can be turned on continuously with a special control bit. **Microcontroller Wake-up Control.** This pin is also turned on when any of the DSC, DOC, or COC bits are set. This can be used to wake-up a sleeping microcontroller to respond to overcurrent conditions with its own control mechanism.
TEMPI	**Temperature Monitor Input (ISL9216 only).** This pin inputs the voltage across a thermistor to determine the temperature of the cells. When this input voltage drops below TEMP3V/13, an external over-temperature condition exists. The TEMPI voltage is also fed to the AO output pin through an analog multiplexer so the temperature of the cells can be monitored by the microcontroller.
RGO	**Regulated Output Voltage.** This pin connects to the emitter of an external NPN transistor and works in conjunction with the RGC pin to provide a regulated 3.3V. The voltage at this pin provides feedback for the regulator and power for many of the ISL9216 and ISL9217 internal circuits. For the ISL9216, this output also provides the 3.3V output voltage for the microcontroller and other external circuits.
RGC	**Regulated Output Control.** This pin connects to the base of an external NPN transistor and works in conjunction with the RGO pin to provide a regulated 3.3V. The RGC output provides the control signal to provide the 3.3V regulated voltage on the RGO pin.
WKUP	**Wake-up Voltage.** This input wakes up the part when the voltage crosses a turn-on threshold (wake-up is edge triggered) and the condition of the pin is reflected in the WKUP bit (The WKUP bit is level sensitive). • WKPOL bit = ”1”: the device wakes up on the rising edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage > threshold. • WKPOL bit = ”0”, the device wakes up on the falling edge of the WKUP pin. Also, the WKUP bit is HIGH only when the WKUP pin voltage < threshold.

Pin Descriptions (Continued)

SYMBOL	DESCRIPTION
WKUPR	**Wake-up Upper Device Signal (ISL9216 only).** This output wakes up the ISL9217 (upper device) when the output is turned on by the microcontroller. Once the upper device is awake, this output can be turned off.
SDA	**Serial Data (ISL9216 only).** This is the bi-directional data line for an I^2C interface.
SCL	**Serial Clock.** This is the clock line for an I^2C communication link.
SDAI	**Serial Data Input (ISL9217 only).** This pin is a uni-directional I^2C serial data input from the ISL9216 to the cascaded ISL9217 device. This pin connects to the ISL9216 SDAOHV pin.
SDAO	**Serial Data Output (ISL9217 only).** This pin is a uni-directional I^2C serial data output to the ISL9216 from the cascaded ISL9217 device. This pin connects to the ISL9216 SDAIHV pin.
SDAIHV	**Serial Data Input (ISL9216 only).** This pin is a uni-directional I^2C serial data input from the cascaded ISL9217 device to the ISL9216. This pin connects to the ISL9217 SDAO pin.
SDAOHV	**Serial Data Output (ISL9216 only).** This pin is a uni-directional serial data output from the ISL9216 to the cascaded ISL9217 device. This pin connects to the ISL9217 SDAI pin.
SCLHV	**Serial Clock Output (ISL9216 only).** This pin sends clock pulses from the lower device (ISL9216) to the upper device (ISL9217) for communication between cascaded devices
HVI^{2}C	**HV I^2C Reference Voltage (ISL9216 only).** This is a reference voltage for the ISL9216 to facilitate the communication link between cascaded devices. Tie this pin on the ISL9216 to the RGO pin of the ISL9217.

Absolute Maximum Ratings

Power Supply Voltage, VCC . . . . . V_{SS} - 0.5V to V_{SS} + 36.0V
Cell Voltage, VCELL
VCELLN to (VCELLN-1), VCELL1-VSS . . . . . -0.5V to 5V
Terminal Voltage, V_{TERM1}
(SCL, SDA, CSENSE, DSENSE, TEMPI, RGO, AO, TEMP3V, SDAI, SDAO) . . . . . V_{SS} - 0.5 to V_{RGO} + 0.5V
Terminal Voltage
V_{TERM2} (CFET, VMON). . . . . V_{SS} - 22.0V to V_{CC}
V_{TERM3} (WKUP) . . . . . V_{SS} - 0.5V to V_{CC}(V_{CC} <27V)
V_{TERM4} (RGC). . . . . V_{SS} - 0.5V to 5V
V_{TERM5}, (SDAOHV, SDAIHV, SCLHV) . . . . . V_{CELL5} - 0.5V to V_{HVI2C} + 0.5V
V_{TERM6}, (all other pins) . . . . . V_{SS} - 0.5V to V_{CC} + 0.5V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN	31	2
24 Ld QFN	32	2

Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . .-55 to +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Operating Temperature . . . . . .-40°C to +85°C
Operating Voltage
VCC pin . . . . . 9.2V to 30.1V
VCELL1-VSS . . . . . 2.3V to 4.3V
VCELLN-(VCELLN-1) . . . . . 2.2V to 4.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Operating Specifications

All Specifications Apply to Both the ISL9216 and ISL9217 Separately Over the Recommended Operating Conditions, Unless Otherwise Specified.

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{CC}		9.2		31	V
Power-up Condition 1	V_{PORVCC}	V_{CC} voltage (Note 3)		4	9.2	V
Power-up Condition 2 Threshold	V_{POR123}	V_{CELL1} - V_{SS} and V_{CELL2} - V_{CELL1} and V_{CELL3} - V_{CELL2} (rising) (Note 3)	1.1	1.7	2.3	V
Power-up Condition 2 Hysteresis	V_{PORhys}	V_{CELL1} - V_{SS} and V_{CELL2} - V_{CELL1} and V_{CELL3} - V_{CELL2} (falling) (Note 3)		70		mV
3.3V Regulated Voltage	V_{RGO}	0µA < I_{RGC} < 350µA	3.0	3.3	3.6	V
3.3VDC Voltage Regulator Control Current Limit	I_{RGC}	(Control current at output of RGC. Recommend NPN with gain of 70+)	0.35	0.50		mA
V_{CC} Supply Current	I_{VCC1}	Power-up defaults, WKUP pin = 0V.		400	510	µA
RGO Supply Current	I_{RGO1}			300	410	µA
V_{CC} Supply Current	I_{VCC2}	LDMONEN bit = 1, VMON floating, CFET = 1, DFET = 1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 06H.		400	700	µA
RGO Supply Current	I_{RGO2}			450	650	µA
V_{CC} Supply Current	I_{VCC3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1			10	µA
RGO Supply Current	I_{RGO3}				1	µA
VCELL Input Current - V_{CELL1}	I_{VCELL1}	AO3:AO0 = 0000H			14	µA
VCELL Input Current - V_{CELL5}	I_{VCELL1}	AO3:AO0 = 0000H (ISL9216 Only)			20	µA
VCELL Input Current - V_{CELLN}	I_{VCELLN}	AO3:AO0 = 0000H			10	µA
OVERCURRENT/SHORT CIRCUIT PROTECTION SPECIFICATIONS (ISL9216 only)						
Overcurrent Detection Threshold (Discharge) Voltage Relative to DSREF **(Default in Boldface)**	V_{OCD}	**V_{OCD} = 0.10V (OCDV1, OCDV0 = 0, 0)**	**0.08**	**0.10**	**0.12**	**V**
		V_{OCD} = 0.12V (OCDV1, OCDV0 = 0, 1)	0.10	0.12	0.14	V
		V_{OCD} = 0.14V (OCDV1, OCDV0 = 1, 0)	0.12	0.14	0.16	V
		V_{OCD} = 0.16V (OCDV1, OCDV0 = 1, 1)	0.14	0.16	0.18	V

Operating Specifications All Specifications Apply to Both the ISL9216 and ISL9217 Separately Over the Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent Detection Threshold (Charge) Voltage Relative to DSREF **(Default in Boldface)**	V_{OCC}	**V_{OCC} = 0.10V (OCCV1, OCCV0 = 0, 0)**	**-0.12**	**-0.10**	**-0.07**	**V**
		V_{OCC} = 0.12V (OCCV1, OCCV0 = 0, 1)	-0.14	-0.12	-0.09	V
		V_{OCC} = 0.14V (OCCV1, OCCV0 = 1, 0)	-0.16	-0.14	-0.11	V
		V_{OCC} = 0.16V (OCCV1, OCCV0 = 1, 1)	-0.18	-0.16	-0.13	V
Short Current Detection Threshold (Discharge) Voltage Relative to DSREF **(Default in Boldface)**	V_{SC}	**V_{OC} = 0.20V (SCDV1, SCDV0 = 0, 0)**	**0.15**	**0.20**	**0.25**	**V**
		V_{OC} = 0.35V (SCDV1, SCDV0 = 0, 1)	0.30	0.35	0.40	V
		V_{OC} = 0.65V (SCDV1, SCDV0 = 1, 0)	0.60	0.65	0.70	V
		V_{OC} = 1.20V (SCDV1, SCDV0 = 1, 1)	1.10	1.20	1.30	V
Load Monitor Input Threshold (falling edge)	V_{VMON}	LDMONEN bit = “1”	1.1	1.45	1.8	V
Load Monitor Input Threshold (hysteresis)	V_{VMONH}	LDMONEN bit = “1”		0.25		mV
Load Monitor Current	I_{VMON}		20	40	60	µA
Short Circuit Time-out	t_{SCD}	Internal short circuit detection delay (SCLONG bit = ‘0’)	90	190	290	µs
		Internal short circuit detection delay (SCLONG bit = ‘1’)	5	10	15	ms
Over Discharge Current Time-out **(Default in Boldface)**	t_{OCD}	**t_{OCD} = 160ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 0)**	**80**	**160**	**240**	**ms**
		t_{OCD} = 320ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 0)	160	320	480	ms
		t_{OCD} = 640ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 0)	320	640	960	ms
		t_{OCD} = 1280ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 0)	640	1280	1920	ms
		t_{OCD} = 2.5ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 1)	1.25	2.50	3.75	ms
		t_{OCD} = 5ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 1)	2.5	5	7.5	ms
		t_{OCD} = 10ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 1)	5	10	15	ms
		t_{OCD} = 20ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 1)	10	20	30	ms
Over Charge Current Time-out **(Default in Boldface)**	t_{OCC}	**t_{OCC} = 80ms (OCCT1, OCCT0 = 0, 0 and CTDIV = 0)**	**40**	**80**	**120**	**ms**
		t_{OCC} = 160ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 0)	80	160	240	ms
		t_{OCC} = 320ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 0)	160	320	480	ms
		t_{OCC} = 640ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 0)	320	640	960	ms
		t_{OCC} = 2.5ms (OCCT1, OCCT0 = 0, 0 and CTDIV = 1)	1.25	2.50	3.75	ms
		t_{OCC} = 5ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 1)	2.5	5	7.5	ms
		t_{OCC} = 10ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 1)	5	10	15	ms
		t_{OCC} = 20ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 1)	10	20	30	ms

Operating Specifications All Specifications Apply to Both the ISL9216 and ISL9217 Separately Over the Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Shutdown Threshold	T_{INTSD}			115		°C
Internal Temperature Hysteresis	T_{HYS}	Temperature drop needed to restore operation after an over-temperature shutdown.		105		°C
Internal Over-Temperature Turn-on Delay Time	T_{ITD}			128		ms
External Temperature Output Current	I_{XT}	Current output capability at TEMP3V pin (ISL9216 only)	1.2			mA
External Temperature Limit Threshold	T_{XTF}	Voltage at V_{TEMPI} (ISL9216 only); Relative to: $\frac{V_{TEMP3V}}{13}$. (Falling edge)	-20	0	+20	mV
External Temperature Limit Hysteresis	T_{XTH}	Voltage at V_{TEMPI} (ISL9216 only).	60	110	160	mV
External Temperature Monitor Delay	t_{XTD}	Delay between activating the external sensor and the internal over-temp detection. (ISL9216 only)		1		ms
External Temperature Autoscan On Time	t_{XTAON}	TEMP3V is ON (3.3V) (ISL9216 only)		5		ms
External Temperature Autoscan Off Time	t_{XTAOFF}	TEMP3V output is off. (ISL9216 only)		635		ms
ANALOG OUTPUT SPECIFICATIONS						
Cell Monitor Analog Output Voltage Accuracy	V_{AO6A}	$[V_{CELL1} - (V_{SS})]/2$ - AO $[V_{CELLN} - (V_{CELLN-1})]/2$ - AO for N = 1 to 5. (ISL9216 only)	-25		30	mV
	V_{AO6B}	V_{CELL6} - AO. (ISL9216 only)	-42		58	mV
	V_{AO7A}	$[V_{CELL1} - (V_{SS})]/2$ - AO $[V_{CELLN} - (V_{CELLN-1})]/2$ - AO for N = 1 to 5. (ISL9217 only)	-20		25	mV
	V_{AO7B}	$[V_{CELLN} - (V_{CELLN-1})]/2$ - AO for N = 6 to 7. (ISL9217 only)	-32		43	mV
Cell Monitor Analog Output External Temperature Accuracy	V_{AOXT}	External temperature monitoring accuracy. Voltage error at AO when monitoring TEMPI voltage (measured with TEMPI = 1V)	-10		10	mV
Internal Temperature Monitor Output Voltage Slope	V_{INTMON}	Internal temperature monitor voltage change		-3.5		mV/°C
Internal Temperature Monitor Output	T_{INT25}	Output at +25°C		1.31		V
AO Output Stabilization Time	t_{VSC}	From SCL falling edge at data bit 0 of command to AO output stable within 0.5% of final value. AO voltage steps from 0V to 2V. (Note 6)			0.1	ms
CELL BALANCE SPECIFICATIONS						
Cell Balance Transistor $r_{DS(ON)}$	R_{CB}	(Note 5)		5		Ω
Cell Balance Transistor Current	I_{CB}				200	mA

Operating Specifications All Specifications Apply to Both the ISL9216 and ISL9217 Separately Over the Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP/SLEEP SPECIFICATIONS						
Device WKUP Pin Voltage Threshold (WKUP pin active HIGH rising edge)	V_{WKUP1}	WKUP pin rising edge (WKPOL = 1) Device wakes up and sets WKUP flag HIGH. (ISL9216 only)	3.5	5.0	6.5	V
Device WKUP Pin Hysteresis (WKUP pin active HIGH)	V_{WKUP1H}	WKUP pin falling edge hysteresis (WKPOL = 1) sets WKUP flag LOW (does not automatically enter sleep mode) (ISL9216 only)		100		mV
Internal Resistor on WKUP	R_{WKUP}	Resistance from WKUP pin to VSS (WKPOL = 1) (ISL9216 only)	130	230	330	kΩ
Device WKUP Pin Voltage Threshold (WKUP pin active LOW - Falling Edge)	V_{WKUP2}	WKUP pin falling edge (WKPOL = 0) Device wakes up and sets WKUP flag HIGH.	V_{CELL1} - 2.6	V_{CELL1} - 2.0	V_{CELL1} - 1.2	V
Device WKUP Pin Hysteresis (WKUP pin active LOW)	V_{WKUP2H}	WKUP pin rising edge hysteresis (WKPOL = 0) sets WKUP flag LOW (does not automatically enter sleep mode)		200		mV
Device Wake-up Delay	t_{WKUP}	Delay after voltage on WKUP pin crosses the threshold (rising or falling) before activating the WKUP bit.	20	40	60	ms
FET CONTROL SPECIFICATIONS (For VCELL1, VCELL2, VCELL3 voltages from 2.8V to 4.3V - ISL9216 only)						
Control Outputs Response Time (CFET, DFET)	t_{CO}	Bit 0 to start of control signal (DFET) Bit 1 to start of control signal (CFET)		1.0		µs
CFET Gate Voltage	VCFET	No load on CFET	V_{CELL3} - 0.5		V_{CELL3}	V
DFET Gate Voltage	VDFET	No load on DFET	V_{CELL3} - 0.5		V_{CELL3}	V
FET Turn-on Current (DFET)	$I_{DF(ON)}$	DFET voltage = 0 to VCELL3 - 1.5V	80	130	400	µA
FET Turn-on Current (CFET)	$I_{CF(ON)}$	CFET voltage = 0 to VCELL3 - 1.5V	80	200	400	µA
FET Turn-off Current (DFET)	$I_{DF(OFF)}$	DFET voltage = VDFET to 1V	100	180		mA
DFET Resistance to VSS	$R_{DF(OFF)}$	VDFET <1V (When turning off the FET)			11	Ω
SERIAL INTERFACE CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)						
SCL Clock Frequency	f_{SCL}				100	kHz
SCL Falling Edge to SDA Output Data Valid	t_{AA}	From SCL falling crossing V_{IH}(min), until SDA exits the V_{IL}(max) to V_{IH}(min) window.			3.5	µs
Time the Bus Must be Free Before Start of New Transmission	t_{BUF}	SDA crossing V_{IH}(min) during a STOP condition to SDA crossing V_{IH}(min) during the following START condition.	4.7			µs
Clock LOW Time	t_{LOW}	Measured at the V_{IL}(max) crossing.	4.7			µs
Clock HIGH Time	t_{HIGH}	Measured at the V_{IH}(min) crossing.	4.0			µs
Start Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing the V_{IH}(min) level.	4.7			µs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL}(max) to SCL falling edge crossing V_{IH}(min).	4.0			µs
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the V_{IL}(max) to V_{IH}(min) window to SCL rising edge crossing V_{IL}(min).	250			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing V_{IH}(min) to SDA entering the V_{IL}(max) to V_{IH}(min) window.	300			ns
Stop Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH}(min) to SDA rising edge crossing V_{IL}(max).	4.0			µs

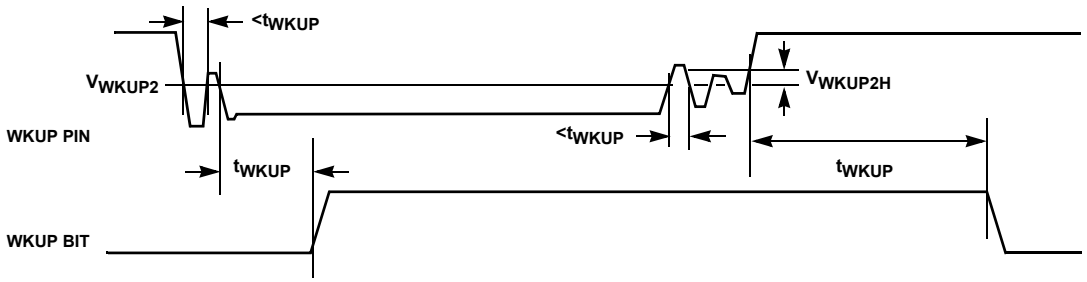
Operating Specifications All Specifications Apply to Both the ISL9216 and ISL9217 Separately Over the Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing V_{IH}(min).	4.0			µs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing V_{IL}(max) until SDA enters the V_{IL}(max) to V_{IH}(min) window. (Note 4)	0			ns
SDA and SCL Rise Time	t_R	From V_{IL}(max) to V_{IH}(min).			1000	ns
SDA and SCL Fall Time	t_F	From V_{IH}(min) to V_{IL}(max).			300	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip			400	pF
SDA and SCL Bus Pull-up Resistor - Off Chip	R_{OUT}	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ For Cb = 40pF, max is about 15kΩ to 20kΩ	1			kΩ
Input Leakage Current (SCL, SDA, SDAI, SDAO, SCLHV, SDAIHV, SDAOHV)	I_{LI}		-10		10	µA
Input Buffer LOW Voltage (SCL, SDA, SDAI)	V_{IL1}	Voltage relative to V_{SS} of the device.	-0.3		V_{RGO} x 0.3	V
Input Buffer HIGH Voltage (SCL, SDA, SDAI)	V_{IH1}	Voltage relative to V_{SS} of the device.	V_{RGO} x 0.7		V_{RGO} + 0.1V	V
Input LOW Voltage (SDAIHV)	V_{IL2}	SDAIHV pulled up to HCI2C. (ISL9216 only)	V_{CELL5} - 0.3		V_{VCELL5} + [V_{HVI2C} - V_{VCELL5}] x 0.3	V
Input HIGH Voltage (SDAIHV)	V_{IH2}	SDAIHV pulled up to HCI2C. (ISL9216 only)	V_{VCELL5} + [V_{HVI2C} - V_{VCELL5}] x 0.7		V_{HVI2C} + 0.1V	V
Output Buffer LOW Voltage (SDA, SDAO)	VOL1	I_{OL} = 1mA (voltage relative to V_{SS} of the device)			0.4	V
Output Buffer LOW Voltage (SDAOHV)	VOL2	I_{OL} = 1mA			V_{VCELL5} + 0.5	V
SDA, SCL, SDAI Input Buffer Hysteresis	I2CHYST (Note 4)	Sleep bit = 0	0.05*V_{RGO}			V

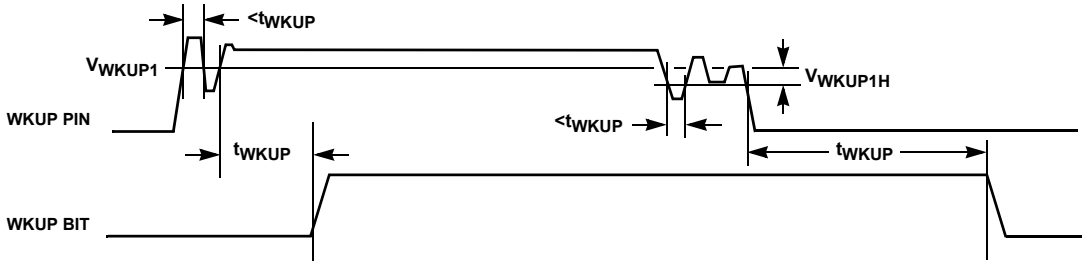
NOTES:

3. Power-up of the device requires all VCELL1, VCELL2, VCELL3, and VCC to be above the limits specified.
4. The device provides an internal hold time of at least 300ns for the SDA signal to bridge the unidentified region of the falling edge of SCL.
5. Limits established by characterization and are not production tested.
6. Maximum output capacitance = 15pF

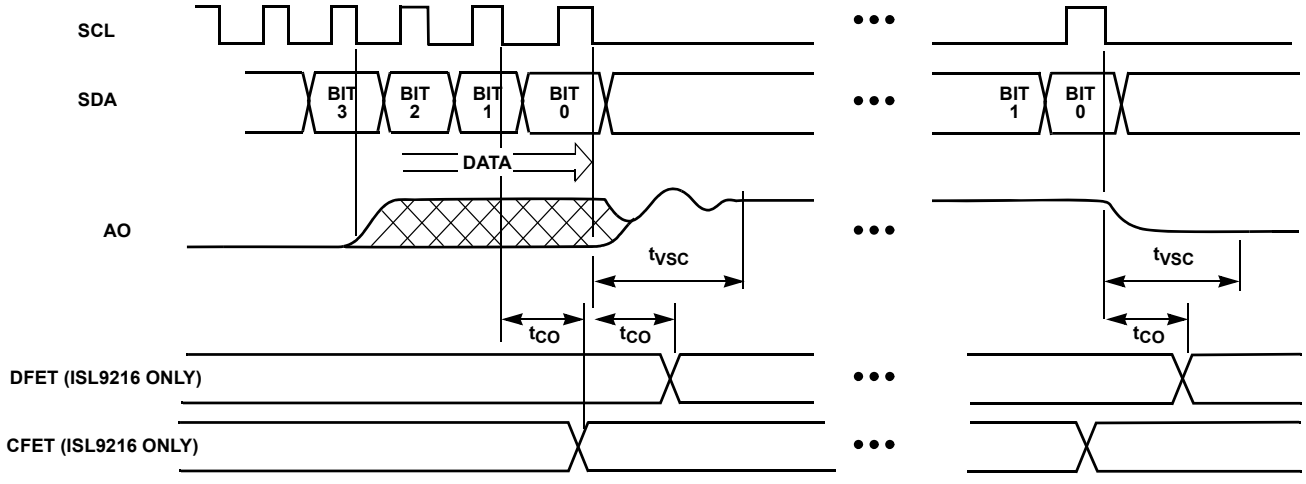
Wake-up Timing (WKPOL = 0)



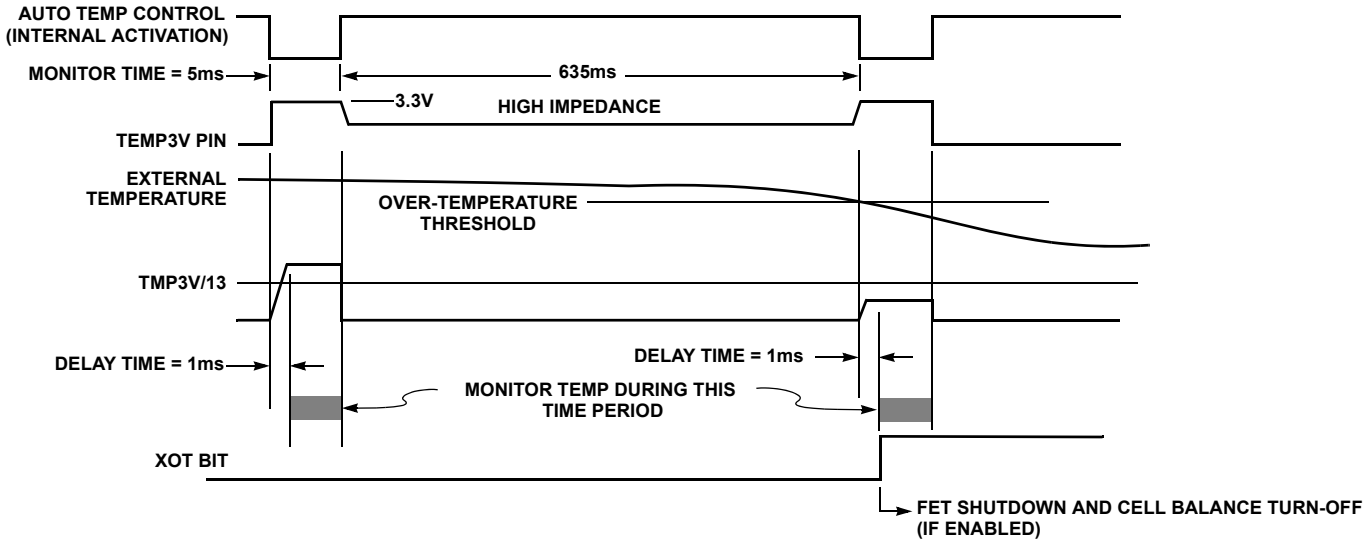
Wake-up Timing (WKPOL = 1)



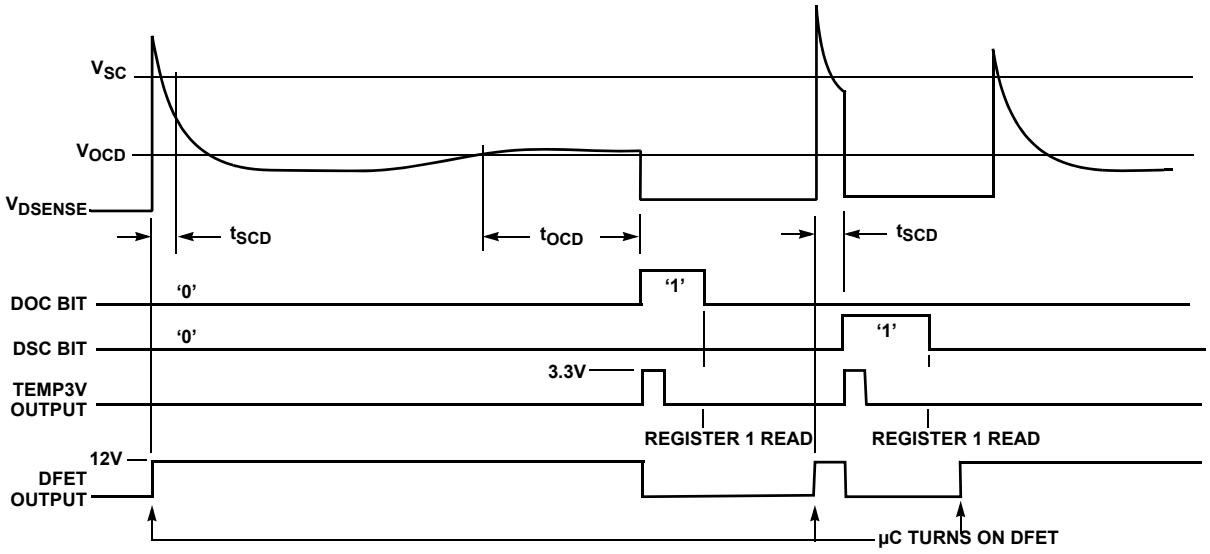
Change in Voltage Source, FET Control



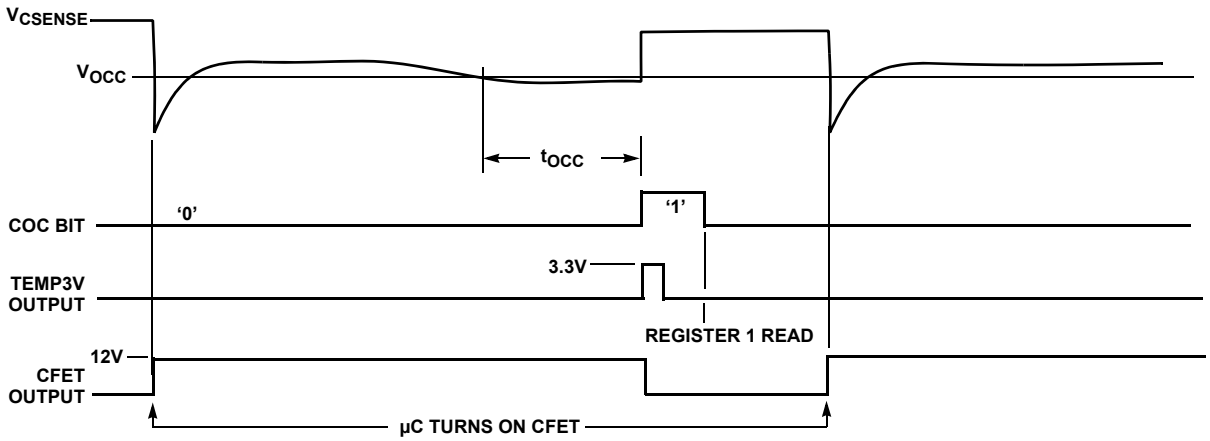
Automatic Temperature Scan (ISL9216 only)



Discharge Overcurrent/Short Circuit Monitor (ISL9216 only) (Assumes DENOCD and DENSCD bits are '0')

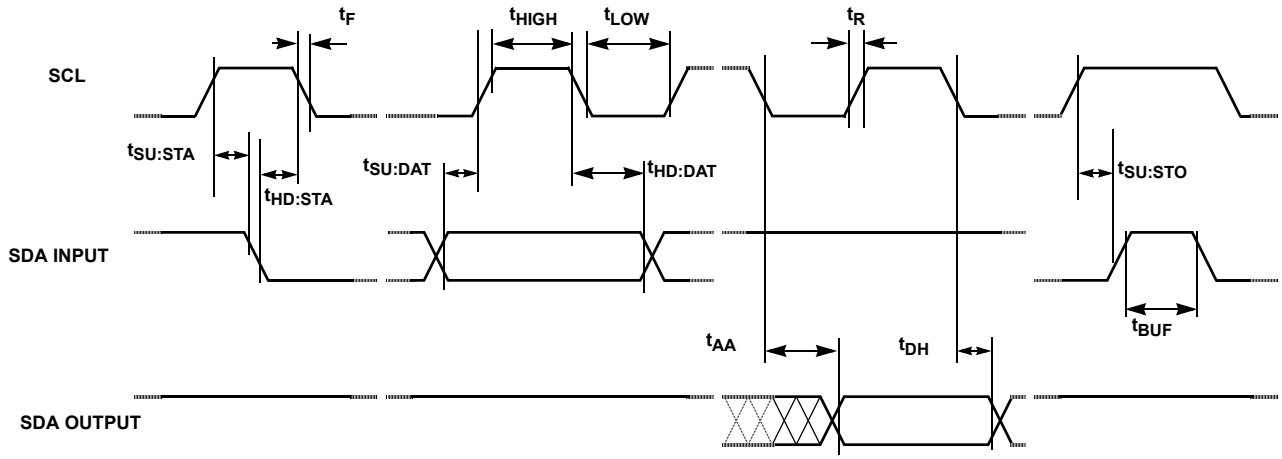


Charge Overcurrent Monitor (ISL9216 only) (Assumes DENOCC bit is '0')



Serial Interface Timing Diagrams

Bus Timing



This timing shows the communication with the ISL9216. Communication with the ISL9217 (through the ISL9216) adds some lag time, however, overall the communication with the ISL9217 meets the same timing requirements as communication with the ISL9216.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Registers

TABLE 1. REGISTERS

ADDR	REGISTER	READ/WRITE	7	6	5	4	3	2	1	0
00H	Configuration Status	Read only	**CU** Cascade U	**CL** Cascade L	**Reserved**	**WKUP** WKUP pin Status	**Reserved**	**Reserved**	**Reserved**	**Reserved**
01H	Operating Status (Note 9)	Read only	**Reserved**	**Reserved**	**XOT** Ext over temp	**IOT** Int over Temp	**LDFAIL** Load Fail (VMON)	**DSC** Short Circuit	**DOC** Discharge OC	**COC** Charge OC
02H	Cell Balance	Read/Write	**CB7ON**	**CB6ON/ WKUPR**	**CB5ON**	**CB4ON**	**CB3ON**	**CB2ON**	**CB1ON**	**Reserved**
			Cell balance FET control bits (plus WKUP of ISL9217 in cascade)							
03H	Analog Out	Read/Write	**UFLG1** User Flag 1	**UFLG0** User Flag 0	**Reserved**	**Reserved**	**AO3**	**AO2**	**AO1**	**AO0**
							Analog output select bits			
04H	FET Control	Read/Write	**SLEEP** Force Sleep (Note 10)	**LDMONEN** Turn on VMON connection	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**CFET** Turn on Charge FET (Note 11)	**DFET** Turn on Disharge FET (Note 11)
05H	Discharge Set	Read/Write (Write only if DISSETEN bit set)	**DENOCD** Turn off automatic OCD control	**OCDV1**	**OCDV0**	**DENSCD** Turn off automatic SCD control	**SCDV1**	**SCDV0**	**OCDT1**	**OCDT0**
				Configure Overcurrent Discharge Threshold			Configure Short Circuit Discharge Threshold		Configure Overcurrent Discharge Time-out	
06H	Charge Set	Read/Write (Write only if CHSETEN bit set)	**DENOCC** Turn off automatic OCC control	**OCCV1**	**OCCV0**	**SCLONG** Long Short-circuit delay	**CTDIV** Divide charge time by 32	**DTDIV** Divide discharge time by 64	**OCCT1**	**OCCT0**
				Configure Overcurrent Charge Threshold					Configure Overcurrent Charge Time-out	
07H	Feature Set	Read/Write (Write only if FSETEN bit set)	**ATMPOFF** Turn off automatic external temp scan	**DIS3** Disable 3.3V reg. (device requires external 3.3V)	**TMP3ON** Temp 3.3V keep on	**DISXTSD** Disable external thermal shutdown	**DISITSD** Disable internal thermal shutdown	**POR** Force POR	**DISWKUP** Disable WKUP pin	**WKPOL** Wake-up Polarity
08H	Write Enable	Read/Write	**FSETEN** Enable Feature Set writes	**CHSETEN** Enable Charge Set writes	**DISSETEN** Enable Discharge Set writes	**UFLG3** User Flag 3	**UFLG2** User Flag 2	**Reserved**	**Reserved**	**Reserved**
09H: FFH	Reserved	NA	RESERVED							

NOTES:

7. A “1” written to a control or configuration bit causes the action to be taken. A “1” read from a status bit indicates that the condition exists.
8. “Reserved” indicates that the bit or register is reserved for future expansion. When writing to addresses 2, 3, 4, 6, 7, and 8: write a reserved bit with the value “0”. Do not write to reserved registers at addresses 09H through FFH. Ignore reserved bits that are returned in a read operation.
9. These status bits are automatically cleared when the register is read. All other status bits are cleared when the condition is cleared.
10. This SLEEP bit is cleared on initial power-up, by the WKUP pin going high (when WKPOL = ”1”) or by the WKUP pin going low (when WKPOL = ”0”), and by writing a “0” to the location with an I^2C command.
11. When the automatic responses are enabled, these bits are automatically reset by hardware when an overcurrent or short circuit condition turns off the FETs. At all other times, an I^2C write operation controls the output to the respective FET and a read returns the current state of the FET drive output circuit (though not the actual voltage at the output pin).
12. The shaded registers are not used in the ISL9217 device. Shaded status registers return ‘0’ when read. Shaded “read/write” registers can be read and written, but they provide no functionality. When writing to the shaded areas in the ISL9217, the locations must be written as “0”.

Status Registers

TABLE 2. CONFIGURATION STATUS REGISTER (ADDR: 00H)

BIT	FUNCTION	DESCRIPTION
7	**CU** Cascade U	Indicates the device is an ISL9217. This bit is set in hardware and cannot be changed.
6	**CL** Cascade L	Indicates the device is an ISL9216. This bit is set in hardware and cannot be changed.
5	**SA**	Reserved for ISL9208 devices.
4	**WKUP** Wake-up Pin Status	This bit is set and reset by hardware. When 'WKPOL' is HIGH, 'WKUP' HIGH = WKUP pin > Threshold voltage 'WKUP' LOW = WKUP pin < Threshold voltage When 'WKPOL' is LOW 'WKUP' HIGH = WKUP pin < Threshold voltage 'WKUP' LOW = WKUP pin > Threshold voltage
3	**RESERVED**	Reserved for future expansion.
2	**RESERVED**	Reserved for future expansion.
1	**RESERVED**	Reserved for future expansion.
0	**RESERVED**	Reserved for future expansion.

TABLE 3. OPERATING STATUS REGISTER (ADDR: 01H)

BIT	FUNCTION	DESCRIPTION
7	**RESERVED**	Reserved for future expansion.
6	**RESERVED**	Reserved for future expansion.
5	**XOT** Ext Over-temp (ISL9216 only)	This bit is set to "1" when the external thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
4	**IOT** Int Over-temp	This bit is set to "1" when the internal thermistor indicates an over-temperature condition. If the temperature condition has cleared, this bit is reset when the register is read.
3	**LDFAIL** Load Fail (VMON) (ISL9216 only)	When the function is enabled, this bit is set to "1" by hardware when a discharge overcurrent or short circuit condition occurs and the load remains heavy. When the load fail condition is cleared or under a light load, the bit is reset when the register is read.
2	**DSC** Short Circuit (ISL9216 only)	This bit is set by hardware when a short circuit condition occurs during discharge. When the discharge short circuit condition is removed, the bit is reset when the register is read.
1	**DOC** Discharge OC (ISL9216 only)	This bit is set by hardware when an overcurrent condition occurs during discharge. When the discharge overcurrent condition is removed, the bit is reset when the register is read.
0	**COC** Charge OC (ISL9216 only)	This bit is set by hardware when an overcurrent condition occurs during charge. When the charge overcurrent condition is removed, the bit is reset when the register is read.

Control Registers

TABLE 4. CELL BALANCE CONTROL REGISTER (ADDR: 02H)

CONTROL REGISTER BITS							
BIT 7 CB7ON	**BIT 6 CB6ON WKUPR**	**BIT 5 CB5ON**	**BIT 4 CB4ON**	**BIT 3 CB3ON**	**BIT 2 CB2ON**	**BIT 1 CB1ON**	**BALANCE**
x	x	x	x	x	x	1	Cell1 ON
x	x	x	x	x	x	0	Cell1 OFF
x	x	x	x	x	1	x	Cell2 ON
x	x	x	x	x	0	x	Cell2 OFF
x	x	x	x	1	x	x	Cell3 ON
x	x	x	x	0	x	x	Cell3 OFF
x	x	x	1	x	x	x	Cell4 ON
x	x	x	0	x	x	x	Cell4 OFF
x	x	1	x	x	x	x	Cell5 ON
x	x	0	x	x	x	x	Cell5 OFF
x	1	x	x	x	x	x	Cell6 ON/WKUPR On (Note 13)
x	0	x	x	x	x	x	Cell6 OFF/WKUPR OFF (Note 13)
1	x	x	x	x	x	x	Cell7 ON (ISL9217 only)
0	x	x	x	x	x	x	Cell7 OFF (ISL9217 only)
Bit 0	**RESERVED**		Reserved for future expansion				

NOTE:

13. WKUPR Pin refers to the ISL9216

TABLE 5. ANALOG OUT CONTROL REGISTER (ADDR: 03H)

BITS	FUNCTION		DESCRIPTION	
7	**UFLG1** User Flag 1		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
6	**UFLG0** User Flag 0		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
5:4	**RESERVED**		Reserved for future expansion	
BIT 3 AO3	**BIT 2 AO2**	**BIT 1 AO1**	**BIT 0 AO0**	**OUTPUT VOLTAGE**
0	0	0	0	No Output (low power state)
0	0	0	1	VCELL1
0	0	1	0	VCELL2
0	0	1	1	VCELL3
0	1	0	0	VCELL4
0	1	0	1	VCELL5
0	1	1	0	VCELL6
0	1	1	1	VCELL7
1	0	0	0	External Temperature
1	0	0	1	Internal Temperature
1	x	1	x	Reserved
1	1	x	x	Reserved

TABLE 6. FET CONTROL REGISTER (ADDR: 04H)

BIT	FUNCTION	DESCRIPTION
7	**SLEEP** Force Sleep	Setting this bit to “1” forces the device to go into a sleep condition. This turns off both FET outputs, the cell balance outputs and the voltage regulator. This also resets the CFET, DFET, and CB7ON:CB1ON bits. The SLEEP bit is automatically reset to “0” when the device wakes up. This does not reset the AO3:AO0 bits.
6	**LDMONEN** Turn on VMON connection (ISL9216 only)	Writing a “1” to this bit turns on the VMON circuit. Writing a “0” to this bit turns off the VMON circuit. As such, the microcontroller has full control of the operation of this circuit.
5:2	**RESERVED**	Reserved for future expansion.
1	**CFET** (ISL9216 only)	Setting this bit to “1” turns on the charge FET. Setting this bit to “0” turns off the charge FET. This bit is automatically reset in the event of a charge overcurrent condition, unless the automatic response is disabled by the DENOCC bit.
0	**DFET** (ISL9216 only)	Setting this bit to “1” turns on the discharge FET. Setting this bit to “0” turns off the discharge FET. This bit is automatically reset in the event of a discharge overcurrent or discharge short circuit condition, unless the automatic response is disabled by the DENOCD or DENSCD bits.

Configuration Registers

The device is configured for specific application requirements using the Configuration Registers. The configuration register consists of SRAM memory. This memory is powered by the RGO output. In a sleep condition, an internal switch powers the contents of these registers from the VCELL1 input.

TABLE 7. DISCHARGE SET CONFIGURATION REGISTER (ADDR: 05H)

SETTING		FUNCTION
Bit 7	**DENOCD** Turn off automatic OCD control (ISL9216 only)	When set to ‘0’, a discharge overcurrent condition automatically turns off the FETs. When set to ‘1’, a discharge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the DOC bit, which also turns on the TEMP3V output.
Bit 6 **OCDV1**	**Bit 5** **OCDV0**	**Discharge Overcurrent Threshold** (ISL9216 only)
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V
Bit 4	**DENSCD** Turn off automatic SCD control (ISL9216 only)	When set to ‘0’, a discharge short circuit condition turns off the FETs. When set to ‘1’, a discharge short circuit condition will not automatically turn off the FETs. In either case, the condition sets the SCD bit, which also turns on the TEMP3V output.
Bit 3 **SCDV1**	**Bit 2** **SCDV0**	**Discharge Short Circuit Threshold** (ISL9216 only)
0	0	V_{SCD} = 0.20V
0	1	V_{SCD} = 0.35V
1	0	V_{SCD} = 0.65V
1	1	V_{SCD} = 1.20V
Bit 1 **OCDT1**	**Bit 0** **OCDT0**	**Discharge Overcurrent Time-out** (ISL9216 only)
0	0	t_{OCD} = 160ms (2.5ms if DTDIV = 1)
0	1	t_{OCD} = 320ms (5ms if DTDIV = 1)
1	0	t_{OCD} = 640ms (8ms if DTDIV = 1)
1	1	t_{OCD} = 1280ms (16ms if DTDIV = 1)

TABLE 8. CHARGE/TIME SCALE CONFIGURATION REGISTER (ADDR: 06H)

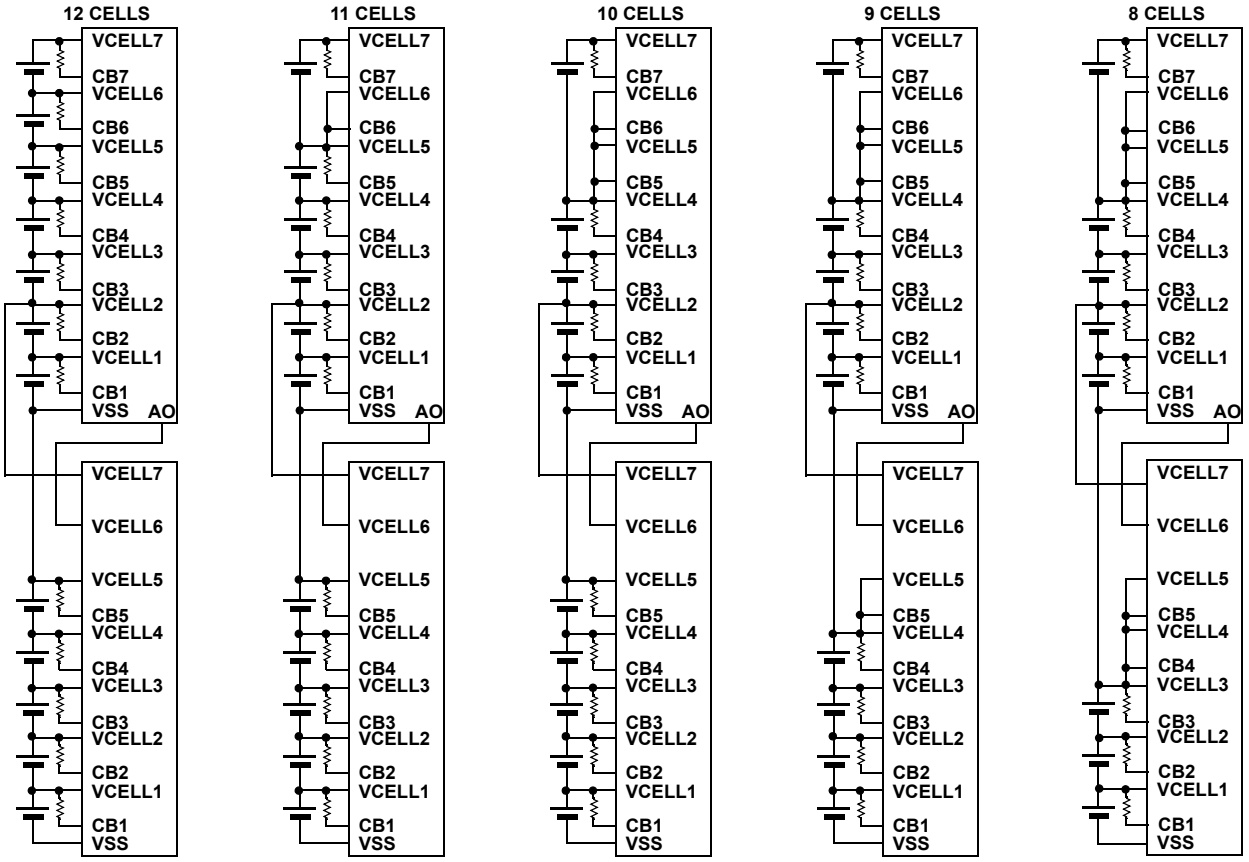
SETTING		FUNCTION
Bit 7	**DENOCC** Turn off automatic OCC control (ISL9216 only)	When set to ‘0’, a charge overcurrent condition automatically turns off the FETs. When set to ‘1’, a charge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the COC bit, which also turns on the TEMP3V output.
Bit 6 **OCCV1**	**Bit 5** **OCCV0**	**Charge Overcurrent Threshold** (ISL9216 only)
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V
Bit 4	**SCLONG** Short circuit long delay (ISL9216 only)	When this bit is set to ‘0’, a short circuit needs to be in effect for 100µs before a shutdown begins. When this bit is set to ‘1’. a short circuit needs to be in effect for 10ms before a shutdown begins.
Bit 3	**CTDIV** Divide charge time by 32 (ISL9216 only)	When set to “1”, the charge overcurrent delay time is divided by 32.
Bit 2	**DTDIV** Divide discharge time by 64 (ISL9216 only)	When set to “1”, the discharge overcurrent delay time is divided by 64.
Bit 1 **OCCT1**	**Bit 0** **OCCT0**	**Charge Overcurrent Time-out** (ISL9216 only)
0	0	t_{OCC} = 80ms (2.5ms if CTDIV=1)
0	1	t_{OCC} = 160ms (4ms if CTDIV=1)
1	0	t_{OCC} = 320ms (8ms if CTDIV=1)
1	1	t_{OCC} = 640ms (16ms if CTDIV=1)

TABLE 9. FEATURE SET CONFIGURATION REGISTER (ADDR: 07H)

BIT	FUNCTION	DESCRIPTION
7	**ATMPOFF** Turn off automatic external temp scan (ISL9216 only)	When set to ‘1’ this bit disables the automatic temperature scan. When set to ‘0’, the temperature is turned on for 5ms in every 640ms.
6	**DIS3** Disable 3.3V reg	Setting this bit to “1” disables the internal 3.3V regulator. Setting this bit to “1” requires that there be an external 3.3V regulator connected to the RGO pin.
5	**TMP3ON** Temp 3.3V keep on	Setting this bit to “1” keeps ON the 3.3V output to the external temperature sensor.
4	**DISXTSD** Disable external thermal shutdown (ISL9216 only)	Setting this bit to “1” disables the automatic shutdown of the cell balance and power FETs in response to an out of limit external temperature. While the automatic response is disabled, the microcontroller can initiate a shutdown based on the XOT flag.
3	**DISITSD** Disable internal thermal shutdown	Setting this bit to “1” disables the automatic shutdown of the cell balance and power FETs in response to an out of limit internal temperature. While the automatic response is disabled, the microcontroller can initiate a shutdown based on the IOT flag.
2	**POR** Force POR	Setting this bit to “1” forces a POR condition. This resets all internal registers to zero.
1	**DISWKUP** Disable WKUP pin	Setting this bit to “1” disables the WKUP pin function. CAUTION: Setting this pin to ‘1’ prevents a wake-up condition. If the device then goes to sleep, it cannot be waken without a communication link that resets this bit, or by power cycling the device.
0	**WKPOL** Wake-up Polarity	Setting this bit to “1” sets the device to wake-up on a rising edge at the WKUP pin. Setting this bit to “0” sets the device to wake-up on a falling edge at the WKUP pin. CAUTION: Setting this pin to ‘1’ in the ISL9217 prevents a wake-up condition. If the device then goes to sleep, it cannot be waken without power cycling the device.

TABLE 10. WRITE ENABLE REGISTER (ADDR: 08H)

BIT	FUNCTION	DESCRIPTION
7	**FSETEN** Enable discharge set writes	When set to “1”, allows writes to the Feature Set register. When set to “0”, prevents writes to the Feature Set register (Addr: 07H). Default on initial power-up is “0”.
6	**CHSETEN** Enable charge set writes (ISL9216 only)	When set to “1”, allows writes to the Charge Set register. When set to “0”, prevents writes to the Feature Set register (Addr: 06H). Default on initial power-up is “0”.
5	**DISSETEN** Enable discharge set writes (ISL9216 only)	When set to “1”, allows writes to the Discharge Set register (Addr: 05H). When set to “0”, prevents writes to the Feature Set register. Default on initial power-up is “0”.
4	**UFLG3** User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
3	**UFLG2** User Flag 3	General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.
2	**RESERVED**	Reserved for future expansion.
1	**RESERVED**	Reserved for future expansion.
0	**RESERVED**	Reserved for future expansion.



NOTE: MULTIPLE CELLS CAN BE CONNECTED IN PARALLEL

FIGURE 1. BATTERY CONNECTION OPTIONS

Device Description

Design Theory

Instructed by the microcontroller, the ISL9216 and ISL9217 chip set performs cell voltage monitoring and cell balancing operations. The ISL9216 has automatic overcurrent and short circuit monitoring, and shut-down with built-in selectable time delays. The ISL9216 also provides automatic turn off of the power FETs and cell balancing FETs in an over-temperature condition. All automatic functions of the ISL9216 can be turned off and the microcontroller can manage the operations through software.

Battery Connection

The ISL9216 and ISL9217 support packs of 8 to 12 series connected Li-ion cells. Connection guidelines for each cell combination are shown in Figure 1.

System Power-Up/Power-Down

The ISL9216 and ISL9217 power-up when the voltages on their VCELL1, VCELL2, VCELL3, and VCC pins all exceed their POR threshold. At this time, the devices each wake-up and turn on their RGO output.

The regulator circuit provides 3.3VDC at pin RGO. It does this by using a control voltage on the RGC pin to drive an external NPN transistor (See Figure 2). For the ISL9216, the transistor should have a beta of at least 70 to provide ample current to the device and external circuits and should have a V_{CE} of greater than 60V (preferably higher) for a 12 cell pack. For the ISL9217, the transistor selection is not as critical because it will likely not drive any external circuits, however, it should be rated with a V_{CE} greater than 50V.

The voltage at the emitter of the NPN transistor is monitored and regulated to 3.3V by the control signal RGC. RGO also powers most of the ISL9216 and ISL9217 internal circuits. A 500Ω resistor is recommended in the collector of each NPN transistor to minimize initial current surge when the regulator turns on.

Once powered up, the devices remain in a wake-up state until put to sleep by the microcontroller (typically when the cells drop too low in voltage) or until the VCELL1, VCELL2, VCELL3, or VCC voltages drop below their POR threshold.

WKUP Pin Operation

There are two ways to design a wake-up of the ISL9216. In an active LOW connection (WKPOL = ’0’ - default), the device wakes up when a charger is connected to the pack. This pulls the WKUP pin low when compared to a reference based on the VCELL1 voltage. In an active HIGH connection (WKPOL = ‘1’) the device wakes up when then WKUP pin is pulled high by a connection through an external switch. See Figure 3.

Once the ISL9216 wakes up, the RGO powers up the microcontroller. The microcontroller then wakes up the ISL9217 by setting the WKUPR bit in the ISL9216. The WKUPR pin of the ISL9216 connects to the ISL9217 WKUP pin. When the ISL9216 WKUPR bit is set to “1”, the ISL9217 WKUP pin pulls low and the ISL9217 wakes up. Because of this operation, it is important that the WKPOL bit of the ISL9217 remain in the default state (ISL9217 WKPOL = 0).

Protection Functions

In the default, recommended condition, the ISL9216 automatically responds to discharge overcurrent, discharge short circuit, charge overcurrent, internal over-temperature, and external over-temperature. The designer can set optional over-ride conditions that allow the response to be dictated by the microcontroller. These are discussed in the following section.

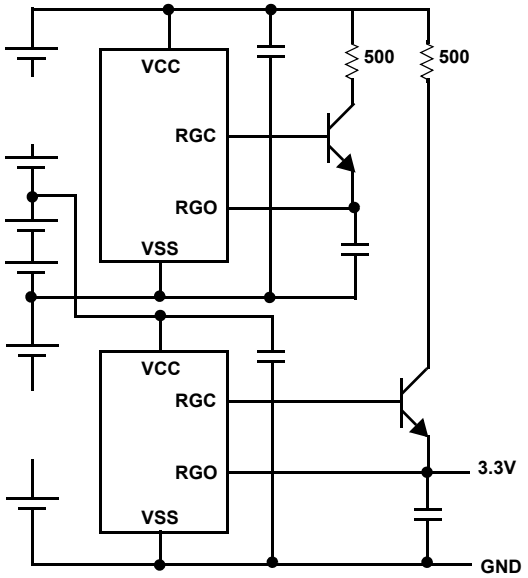


FIGURE 2. VOLTAGE REGULATOR CIRCUITS

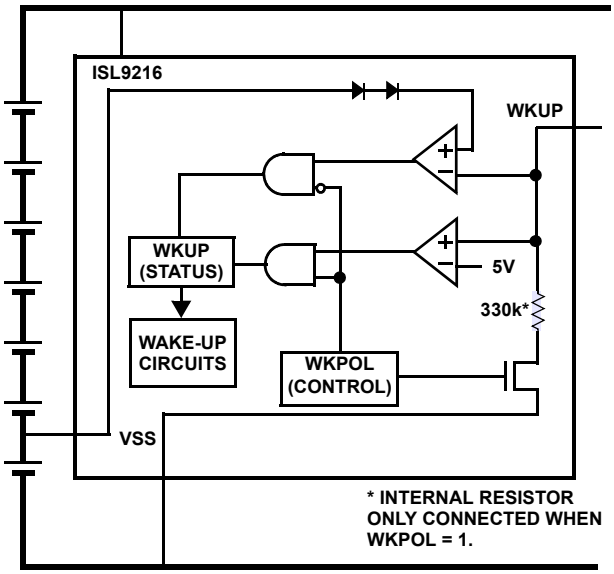


FIGURE 3. WAKE-UP CONTROL CIRCUITS

OVERCURRENT SAFETY FUNCTIONS

The ISL9216 continually monitors the discharge current by monitoring the voltage at the CSENSE and DSENSE pins. If that voltage exceeds a selected value for a time exceeding a selected delay, then the device enters an overcurrent or short circuit protection mode. In these modes, the ISL9216 automatically turns off both power FETs and hence prevents current from flowing through the terminals P+ and P-.

The voltage thresholds and the response times of the overcurrent protection circuits are selectable for discharge overcurrent, charge overcurrent, and discharge short circuit conditions. The specific settings are determined by bits in the "DISCHARGE SET CONFIGURATION REGISTER (ADDR: 05H)" on page 18, and "CHARGE/TIME SCALE CONFIGURATION REGISTER (ADDR: 06H)" on page 19. (See also "REGISTERS" on page 14).

In an overcurrent condition, the ISL9216 automatically turns off the voltage on CFET and DFET pins. The DFET output drives the discharge FET gate low, turning off the FET quickly. The CFET output turns off and allows the gate of the charge FET to be pulled low through a resistor.

By turning off the FETs the ISL9216 prevents damage to the battery pack caused by excessive current into or out of the cells (as in the case of a faulty charger or short circuit condition).

When the ISL9216 detects a discharge overcurrent condition, the ISL9216 turns off both power FETs and sets the DOC bit. (When the FETs are turned off, the DFET and CFET bits are also reset). The automatic response to overcurrent during discharge is prevented by setting the DENOCD bit to "1". The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually turn on the load monitor function (by setting the LDMONEN bit) and monitor the LDFAIL bit to detect that the overcurrent condition has been removed.

When the ISL9216 detects a discharge short circuit condition, both power FETs are turned off and DSC bit is set. (When the FETs are turned off, the DFET and CFET bits are also reset). The automatic response to short circuit during discharge is prevented by setting the DENSCD bit to "1". The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually turn on the load monitor function (by setting the LDMONEN bit) and monitor the LDFAIL bit to detect that the overcurrent condition has been removed.

When the ISL9216 detects a charge overcurrent condition, both power FETs are turned off and COC bit is set. (When the FETs are turned off, the DFET and CFET bits are also reset). The automatic response to overcurrent during discharge is prevented by setting the DENOCC bit to "1". The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually wait to do this until the cell voltages are not over charged and that the overcurrent condition has been removed. Or, the microcontroller could wait until the pack is removed from the charger and then re-attached.

An alternative method of providing the protection function, if desired by the designer, is to turn off the automatic safety response. In this case, the ISL9216 device still monitors the conditions and sets the status bits, but takes no action in overcurrent or short circuit conditions. Safety of the pack depends, instead, on the microcontroller to send commands to the ISL9216 to turn off the FETs.

To facilitate a microcontroller response to an overcurrent condition, especially if the microcontroller is in a low power state, a charge overcurrent flag (COC), a discharge overcurrent flag (DOC), or the short circuit flag (DSC) being set causes the ISL9216 TEMP3V output to turn on and pull high. (See Figure 5). This output can be used as an external interrupt by the microcontroller to wake-up quickly to handle the overcurrent condition.

LOAD MONITORING

The load monitor function in the ISL9216 (see Figure 4) is used primarily to detect that the load has been removed following an overcurrent or short circuit condition during discharge. This can be used in a control algorithm to prevent the FETs from turning on while the overload or short circuit condition remains.

The load monitor can also be used by the microcontroller algorithms after an undervoltage condition on any cells causes the FETs to turn off. Use of the load monitor prevents the FETs from turning on while the load is still present. This minimizes the possible "oscillations" that can occur when a load is applied in a low capacity pack. It can also be part of a system protection mechanism to prevent the load from turning on automatically - i.e. some action must be taken before the pack is again turned on.

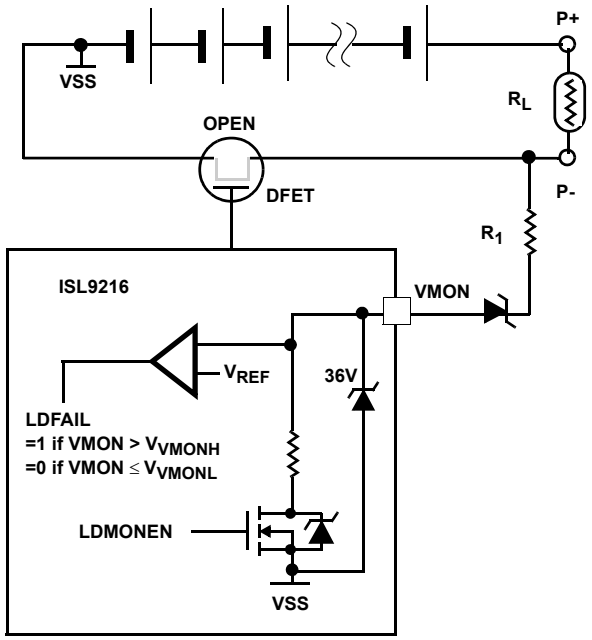


FIGURE 4. LOAD MONITOR CIRCUIT

The load monitor circuit can be turned on or off by the microcontroller. It is normally turned off to minimize current

consumption. It must be activated by the external microcontroller for it to operate. The circuit works by internally connecting the VMON pin to VSS through a resistor. The circuit operates as shown in Figure 4.

In a typical pack operation, when an overcurrent or short circuit event happens, the DFET turns off, opening the battery circuit to the load. At this time, the R_L is small and the load monitor is initially off. In this condition, the voltage at VMON could rise to nearly the pack voltage. However, since in most configurations, this voltage would exceed the maximum limits on the VMON pin, a series zener diode is required.

Once the power FETs turn off, the microcontroller activates the load monitor by setting the LDMONEN bit. This turns on an internal FET that adds a pull-down resistor to the load monitor circuit. While still in the overload condition the combination of the load resistor, an external adjustment resistor (R_1), the zener diode, and the internal load monitor resistor form a voltage divider. R_1 is chosen so that when the load is released to a sufficient level, the LDFAIL condition is reset.

OVER-TEMPERATURE SAFETY FUNCTIONS

External Temperature Control

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL9216 TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, the ISL9216 continuously turns on TEMP3V output (and the external temperature monitor) for 5ms every 640ms. In this way, the external temperature is monitored even if the microcontroller is asleep. If the ATMPOFF bit is set, this automatic temperature scan is turned off.

When the TEMP3V output turns on, the ISL9216 waits 1ms for the temperature reading to stabilize, then compares the external temperature voltage with an internal voltage divider that is set to TEMP3V/13. When the thermistor voltage is below the reference threshold after the delay, an external temperature fail condition exists. To set the external over-temperature limit, set the value of R_X resistor to the 12 times the resistance of the thermistor at the over-temperature threshold.

The TEMP3V output pin also turns on when the microcontroller sets the AO3:AO0 bits to select that the external temperature voltage. This causes the TEMPI voltage to be placed on AO and activates (after 1ms) the over-temperature detection. As long as the AO3:AO0 bits point to the external temperature, the TEMP3V output remains on.

Because of the manual scan of the temperature, it may be desired to turn off the automatic scan, although they can be used at the same time without interference. To turn off the automatic scan, set the ATMPOFF bit.

The microcontroller can over-ride both the automatic temperature scan and the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns on the TEMP3V output to keep the temperature control voltage on all the time, for a continuous monitoring of an over-temperature condition. This likely will consume a significant amount of current, so this feature is usually used for special or test purposes.

Protection

As a default, when the ISL9216 detects an internal or external over-temperature condition, the FETs are turned off, the cell balancing function is disabled, and the IOT bit or XOT bit (respectively) is set.

Turning off the FETs in the event of an over-temperature condition prevents continued discharge or charge of the cells when they are over heated. Turning off the cell balancing in the event of an over-temperature condition prevents damage to the IC in the event too many cells are being balanced, causing too much power dissipation in the ISL9216.

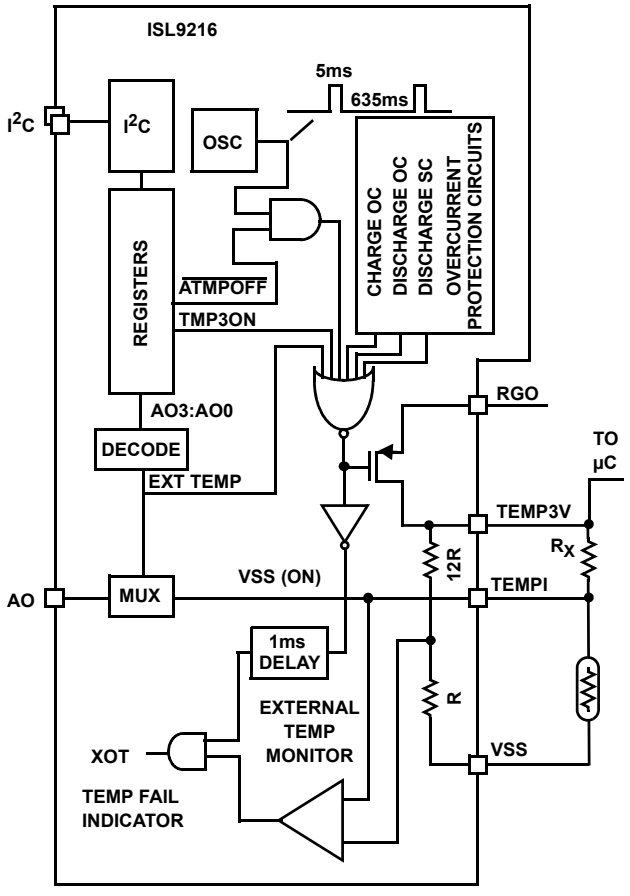


FIGURE 5. EXTERNAL TEMPERATURE MONITORING AND CONTROL (ISL9216 ONLY)

In the event of an automatic over-temperature condition, cell balancing is prevented and FETs are held off until the temperature drops back below the temperature recovery threshold. During this temperature shutdown period, the

microcontroller can monitor the internal temperature through the analog output pin (AO), but any writes to the CFET bit, DFET bit, or cell balancing bits are ignored

The automatic response to an internal over-temperature is prevented by setting the DISITSD bit to “1”. The automatic response to an external over-temperature is prevented by setting the DISXTSD bit to “1”. In either case, it is important for the microcontroller to monitor the internal and external temperature to protect the pack and the electronics in an over-temperature condition.

Analog Multiplexer Selection

The ISL9216 and ISL9217 devices can be used to externally monitor individual battery cell voltages and temperatures. Each quantity can be monitored at the analog output pin (AO) and is selected using the I^2C interface. See Figure 6.

To monitor the voltages on the ISL9217 inputs, set the ISL9216 to monitor VCELL6, then set the ISL9217 to the desired VCELL input. The ISL9216 and ISL9217 VCELL input voltages are divided by 2, except for the ISL9216 VCELL6 input. This is a divide by 1 input. In this way, the value read at the ISL9216 AO output is always a divide by 2 of the original cell voltage.

VOLTAGE MONITORING

Since the voltage on each of the Li-Ion Cells are normally higher than the regulated supply voltage, it is necessary to both level shift and divide the voltage. To get into the voltage range required by the external A/D converter, the voltage level shifter divides the cell voltage by 2. Therefore, a Li-Ion cell with a voltage of 4.2V is reported via the AO pin to be 2.1V.

TEMPERATURE MONITORING

The voltage representing the external temperature applied at the TEMPI terminal is directed to the AO terminal through a MUX, as selected by the AO control bits (see Figures 5 and 6). The external temperature voltage is not divided by 2 as are the cell voltages. Instead it is a direct reflection of the voltage at the TEMPI pin.

A similar operation occurs when monitoring the internal temperature through the AO output, except there is no external “calibration” of the voltage associated with the internal temperature. For the internal temperature monitoring, the voltage at the output is linear with respect to temperature. (See “Operating Specifications” on page 6 for information about the output voltage at +25°C and the output slope relative to temperature).

Cell Balancing

OVERVIEW

A typical ISL9216 and ISL9217 Li-ion battery pack consists of 8 to 12 cells in series, with one or more cells in parallel. This combination gives both the voltage and power necessary for power tools, e-bikes, electric wheel chairs, portable medical equipment, and battery powered industrial applications. While the series/parallel combination of Li-ion cells is common, the configuration is not as efficient as it could be, because any capacity mismatch between series-connected cells reduces the overall pack capacity. This mismatch is greater as the number of series cells and the load current increase. Cell balancing techniques increase the capacity and the operating time of Li-ion battery packs.

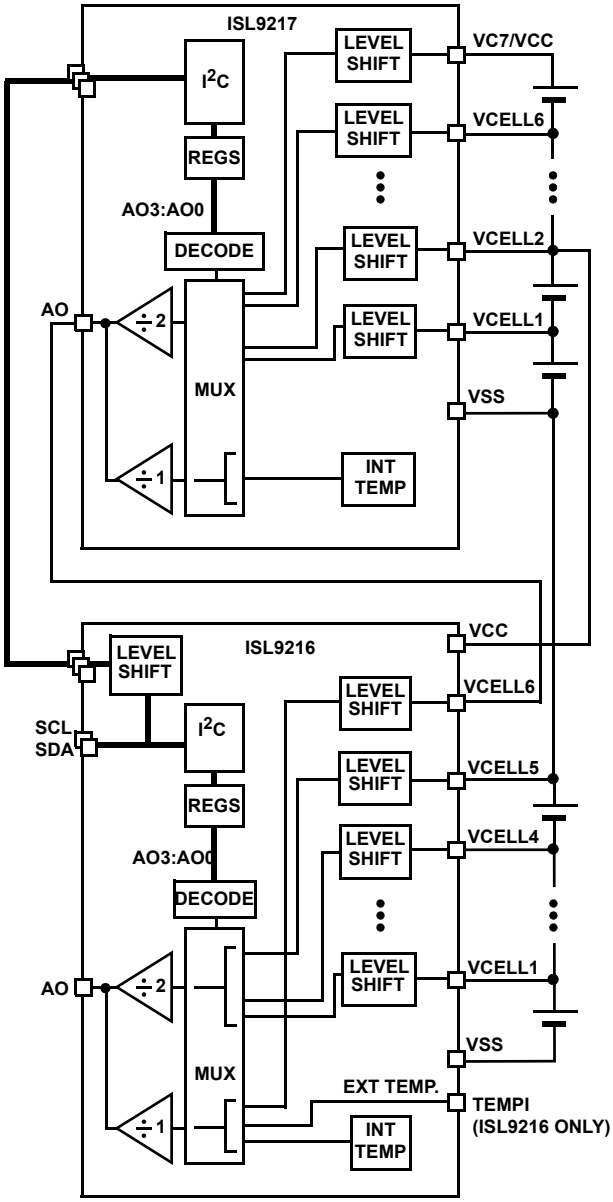


FIGURE 6. ANALOG OUTPUT MONITORING DIAGRAM

DEFINITION OF CELL BALANCING

Cell balancing is defined as the application of differential currents to individual cells (or combinations of cells) in a series string. Normally, of course, cells in a series string receive identical currents. A battery pack requires additional components and circuitry to achieve cell balancing. For the ISL9216 and ISL9217 devices, the only external components required are balancing resistors.

CELL BALANCE OPERATION

Cell balancing is accomplished through a microcontroller algorithm. This algorithm compares the cell voltages (a representation of the pack capacity) and turns on balancing for the cells that have the higher voltages. There are many parameters that should be considered when writing this algorithm. An example cell balancing algorithm is available in the ISL9216EVAL1Z evaluation kit.

The microcontroller turns on the specific cell balancing by setting a bit in the Cell Balance Register. Each bit in the register corresponds to one cell's balancing control. When the bit is set, an internal cell balancing FET turns on. This shorts an external resistor across the specified cell. The maximum current that can be drawn from (or bypassed around) the cell is 200mA. This current is set by selecting the value of the external resistor. Figure 7 shows an example with a 200mA (maximum) balancing current.

With lower balancing current, more balancing FETs can be turned on at once, without exceeding the device power dissipation limits or generating excessive balancing current that will heat the external resistor.

External VMON/CFET Protection Mechanisms

When there is a single charge/discharge path, a blocking diode is required in the ISL9216 VMON to P- path. See D1 in Figure 8. This diode is to protect against a negative voltage on the VMON pin that can occur when the FETs are off and the charger connects to the pack. This diode is not needed when there is a separate charge and discharge path, because the voltages on P- (discharge) are likely always positive.

For the cascaded combination of ISL9216 and ISL9217, a zener diode (D2 in Figure 8) needs to be in the ISL9216 VMON path to the P- pin to protect the ISL9216 from an overvoltage condition when the FETs open due to a short circuit or overcurrent condition.

With the single set of charge/discharge FETs, the ISL9216 CFET pin needs to be protected in the event of an over-current or short circuit shut-down. When this happens, the FET opens suddenly. The flyback voltage from the motor windings will likely exceed the maximum input voltage on the CFET pin. So, when operating in this configuration, an additional external series diode must be placed between the CFET pin of the ISL9216 and the gate of the Charge FET. See Diode D3 in Figure 8. This will reduce the CFET gate voltage, but not significantly.

Finally, in all configurations, to protect the Charge FET itself in the event of a large negative voltage on the Pack- pin, zener diode D4 is added. The large negative voltage can occur when the P- pin goes significantly negative, while the CFET pin is being internally clamped at VSS. The zener voltage of D4 should be less than the V_{GS}(max) specification of the FET.

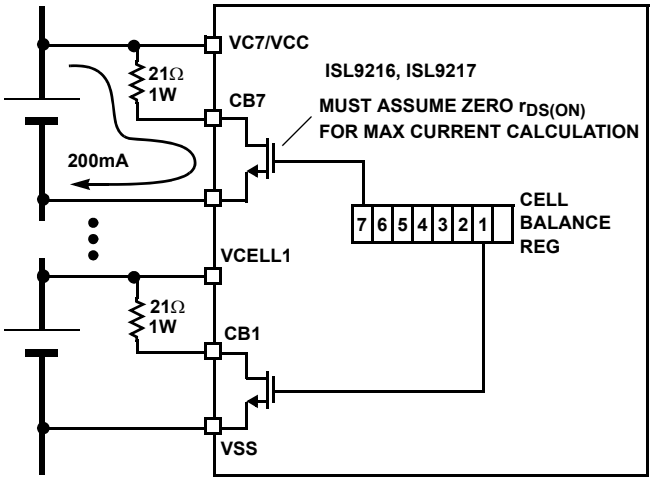


FIGURE 7. CELL BALANCING CONTROL EXAMPLE WITH 100mA BALANCING CURRENT

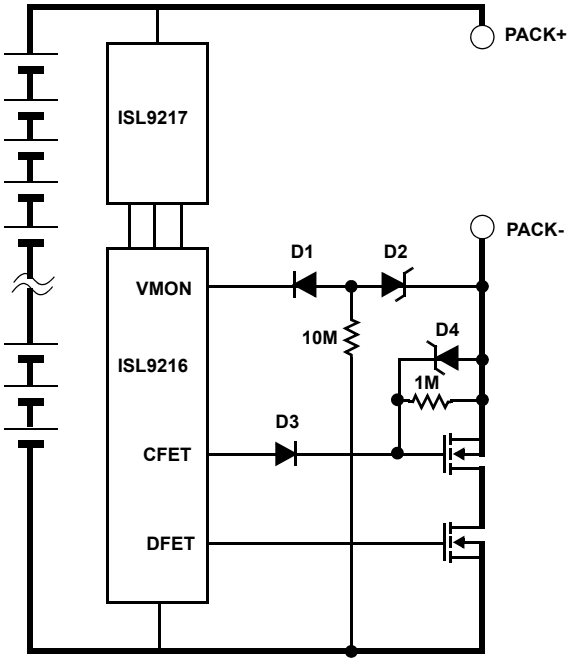


FIGURE 8. USE OF A DIODES FOR PROTECTING THE CFET AND VMON PINS.

User Flags

The ISL9216 and ISL9217 each contain four flags in the register area that the microcontroller can use for general purpose indicators. These bits are designated UFLG3, UFLG2, UFLG1, and UFLG0. The microcontroller can set or reset these bits by writing into the appropriate register.

The user flag bits are battery backed up, so the contents remain even after a sleep mode. However, if the mirocontroller sets the POR bit to force a power on reset, all of the user flags will also be reset. In addition, if the voltage on cell1 ever drops below the POR voltage, the contents of the user flags (as well as all other register values) could be lost.

Serial Interface

INTERFACE CONVENTIONS

The device supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the ISL9216 and ISL9217 devices operate as slaves in all applications.

When sending or receiving data, the convention is the most significant bit (MSB) is sent first. So, the first address bit sent is bit 7.

CLOCK AND DATA

Data states on the SDA line can change only while SCL is LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 9.

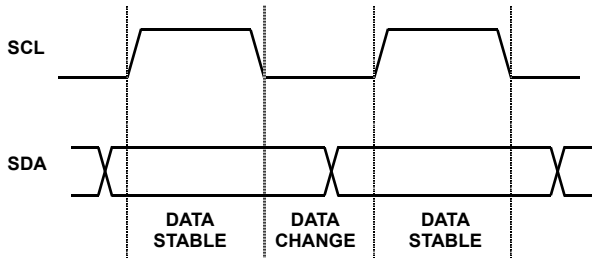


FIGURE 9. VALID DATA CHANGES ON I^2C BUS

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 10.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition is only issued after the transmitting device has released the bus. See Figure 10.

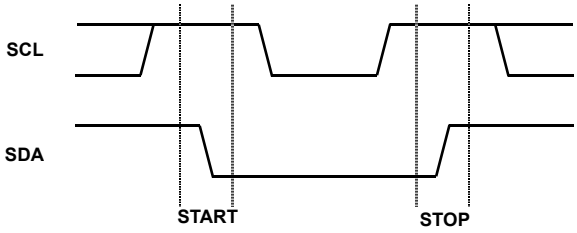


FIGURE 10. I^2C START AND STOP BITS

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge that it received the 8-bits of data. See Figure 11.

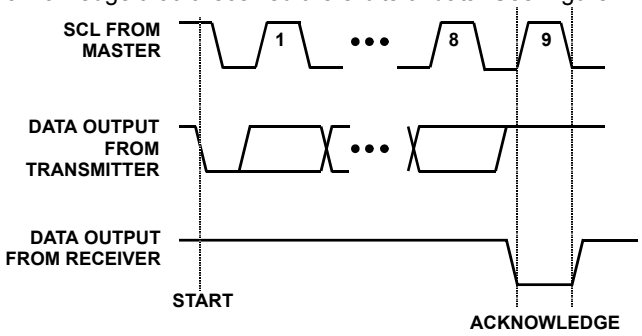


FIGURE 11. ACKNOWLEDGE RESPONSE FROM RECEIVER

The device responds with an acknowledge after recognition of a start condition and the correct slave byte. If a write operation is selected, the device responds with an acknowledge after the receipt of each subsequent 8-bits. The device acknowledges all incoming data and address bytes, except for the slave byte when the contents do not match the devices internal pattern.

In the read mode, the device transmits 8-bits of data, releases the SDA line, then monitors the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continues to transmit data. The device terminates further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

WRITE OPERATIONS

For a write operation, the device requires a slave byte and an address byte. The slave byte specifies which of the devices (in a cascade configuration) the master is writing to. The address specifies one of the registers in that device. After receipt of each byte, the device responds with an acknowledge, and awaits the next 8-bits from the master. After the acknowledge, following the transfer of data, the master terminates the transfer by generating a stop condition. See Figure 12.

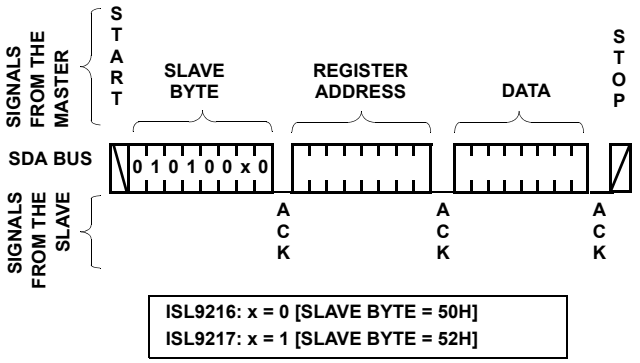


FIGURE 12. WRITE SEQUENCE

When receiving data from the master, the value in the data byte is transferred into the register specified by the address byte on the falling edge of the clock following the 8th data bit.

After receiving the acknowledge after the data byte, the device automatically increments the address. So, before sending the stop bit, the master may send additional data to the device without re-sending the slave and address bytes. After writing to address 0AH, the address “wraps around’ to address 0.

Read Operations

Read operations are initiated in the same manner as write operations with the host sending the address where the read is to start (but no data). Then, the host sends an ACK, a repeated start and the slave byte with the LSB = 1. After the device acknowledges the slave byte, the device sends out one bit of data for each master clock. After the slave sends 8 bits to the master, the master sends a NACK (Not acknowledge) to the device to indicate that the data transfer is complete, then the master sends a stop bit. See Figure 13.

After sending the eighth data bit to the master, the device automatically increments its internal address pointer. Therefore, the master, instead of sending a NACK and the stop bit, can send additional clocks to read the contents of the next register - without sending another slave and address byte.

If the last address read or written is known, the master can initiate a current address read. In this case, only the slave byte is sent before data is returned. See Figure 13.

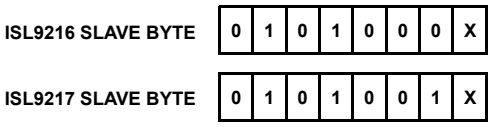


FIGURE 14. DEVICE SLAVE BYTES

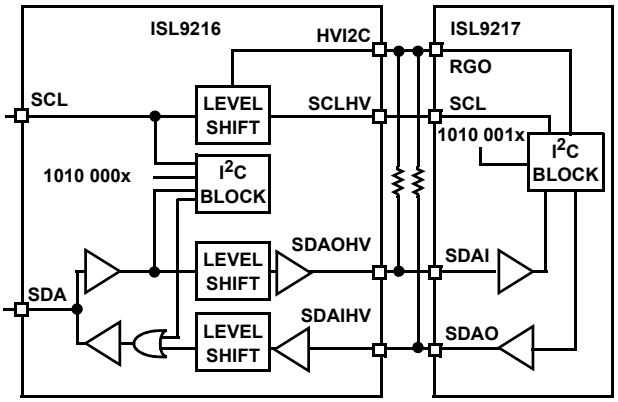


FIGURE 15. I^2C CASCADED INTERFACE

Cascade Operation

When devices are cascaded, the lower device has the I^2C slave address of 0101 000x and the upper device has the address 0101 001x (See Figure 14), but the operation of cascaded devices is transparent to the microcontroller master device.

The serial interface between cascaded ISL9216 and ISL9217 devices has one clock and two data lines. There is also a high voltage reference for this commication link. See Figure 15. The interface lines are:

- SCLHV, which is a level shifted clock from the lower device (ISL9216) to the upper device (ISL9217);
- SDAOHV and SDAO, which send level shifted data out of the ISL9216 and ISL9217 (respectively); and
- SDAIHV and SDAI, which are level shifted inputs into the ISL9216 and ISL9217 (respectively).
- HVI2C (ISL9216), which is a reference voltage for the level shifted interface. This connects to the ISL9217 RGO pin.

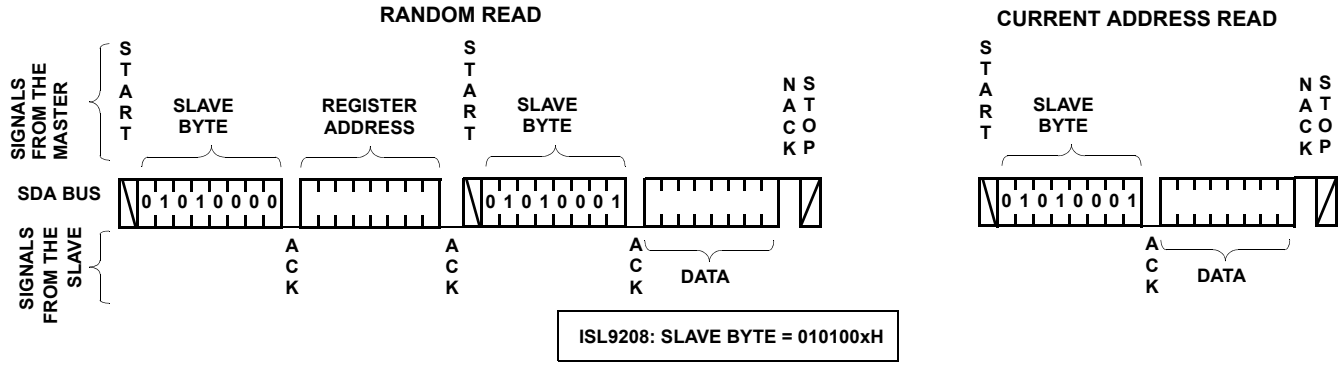


FIGURE 13. READ SEQUENCE

When data is clocked into the ISL9216 through the I^2C port, it is immediately transferred to the serial cascade port, so both the ISL9216 and ISL9217 see the slave byte at the same time. After the 8th slave bit, the device that receives the correct slave byte sends an acknowledge, while the other device ignores all subsequent data on the serial port until it receives a stop bit. However, even though the ISL9216 ignores the data, it still passes it through to the ISL9217.

The SDAI and SDAO pins of the ISL9217 need to have pull-up resistors of approximately 4.7kΩ, since the output drivers are open-drain devices.

Register Protection

The Discharge Set, Charge Set, and Feature Set configuration registers are write protected on initial power-up. In order to write to these registers it is necessary to set a bit to enable each one. These write enable bits are in the Write Enable register (Address 08H).

Write the FSETEN bit (Addr 8:bit 7) to “1” to change the data in the Feature Set register (Address 7).

Write the CHSETEN bit (Addr 8:bit 6) to “1” to change the data in the Feature Set register (Address 6).

Write the DISSETEN bit (Addr 8:bit 5) to “1” to change the data in the Feature Set register (Address 5).

The microcontroller can reset these bits back to zero to prevent inadvertent writes that change the operation of the pack.

Operation State Machine

Figure 16 shows a device state machine which defines how the ISL9216 and ISL9217 respond to various conditions.

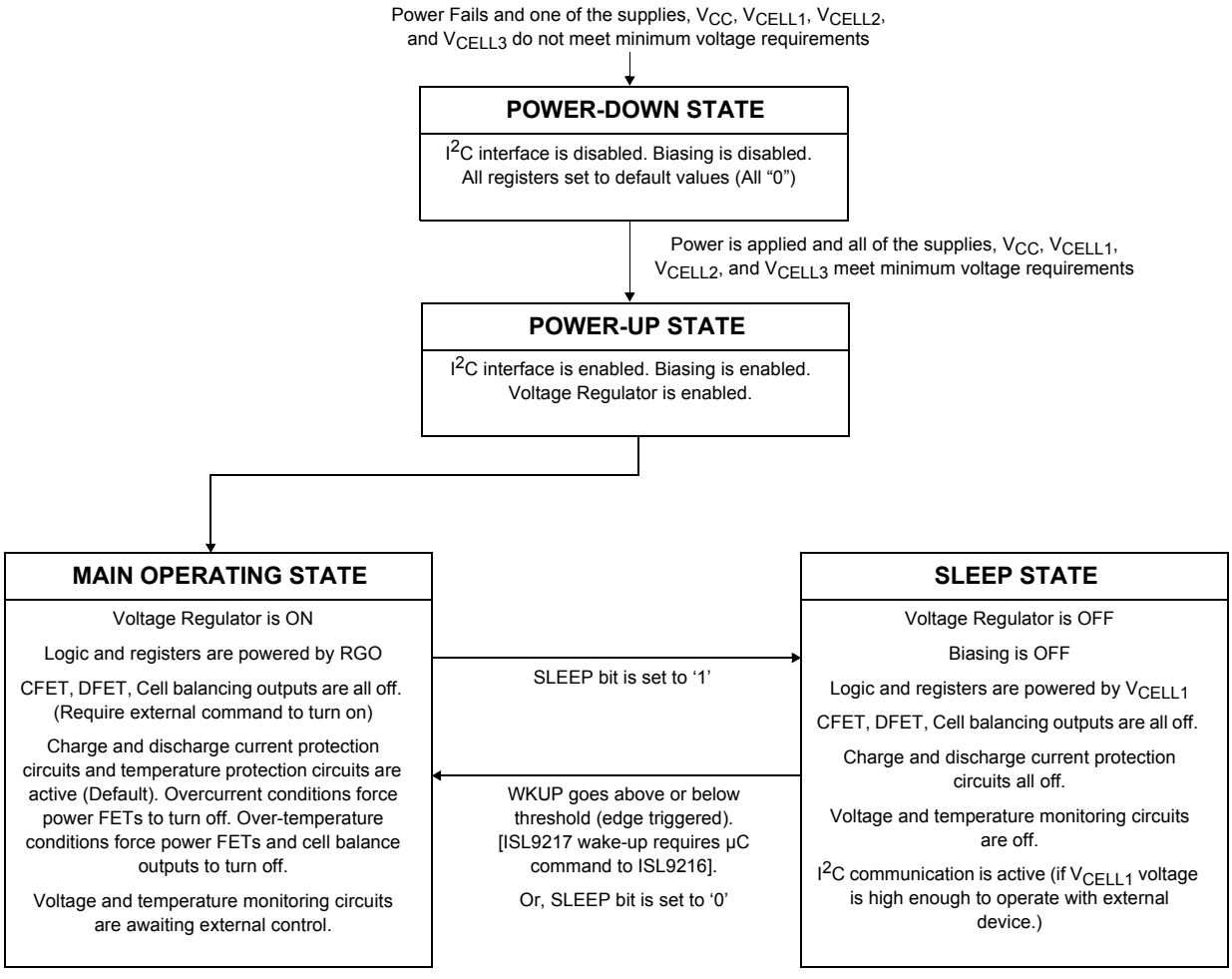


FIGURE 16. DEVICE OPERATION STATE MACHINE

Applications Circuits

The following application circuits are ideas to consider when developing a battery pack implementation. There are many more ways that the pack can be designed.

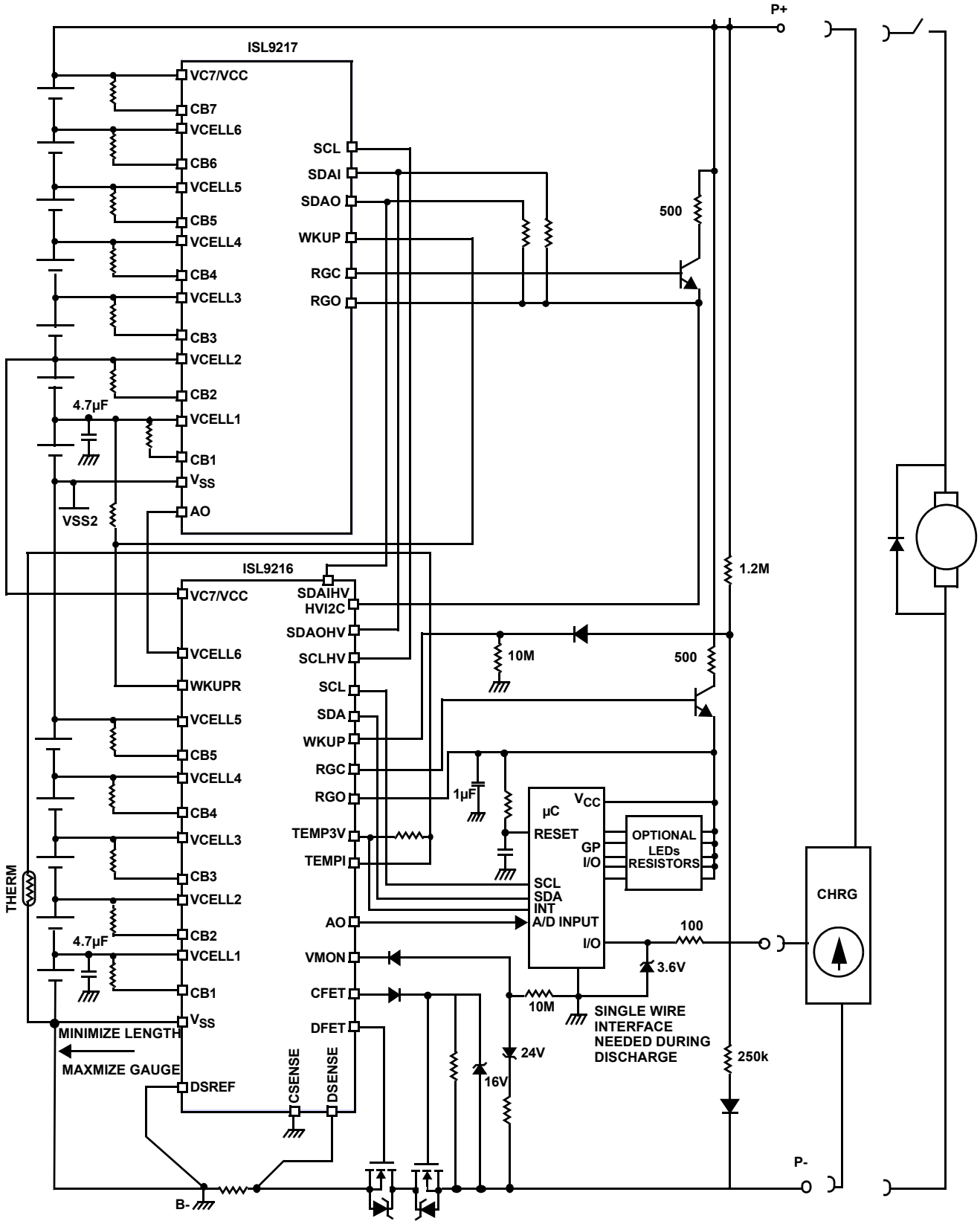


FIGURE 17. 12-CELL CASCADED APPLICATION CIRCUIT WITH INTEGRATED CHARGE/DISCHARGE

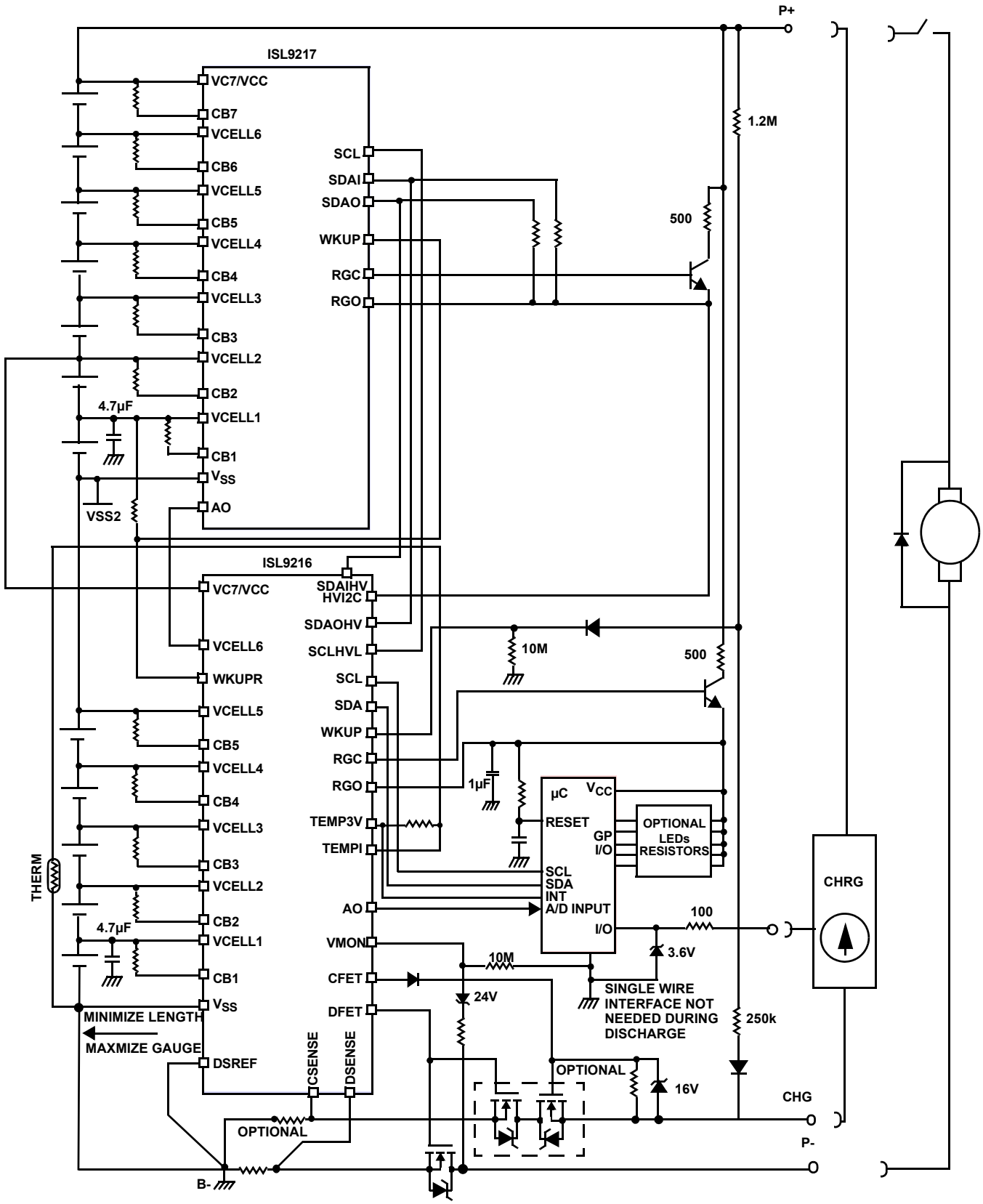


FIGURE 18. 12-CELL CASCADED APPLICATION CIRCUIT WITH SEPARATE CHARGE/DISCHARGE

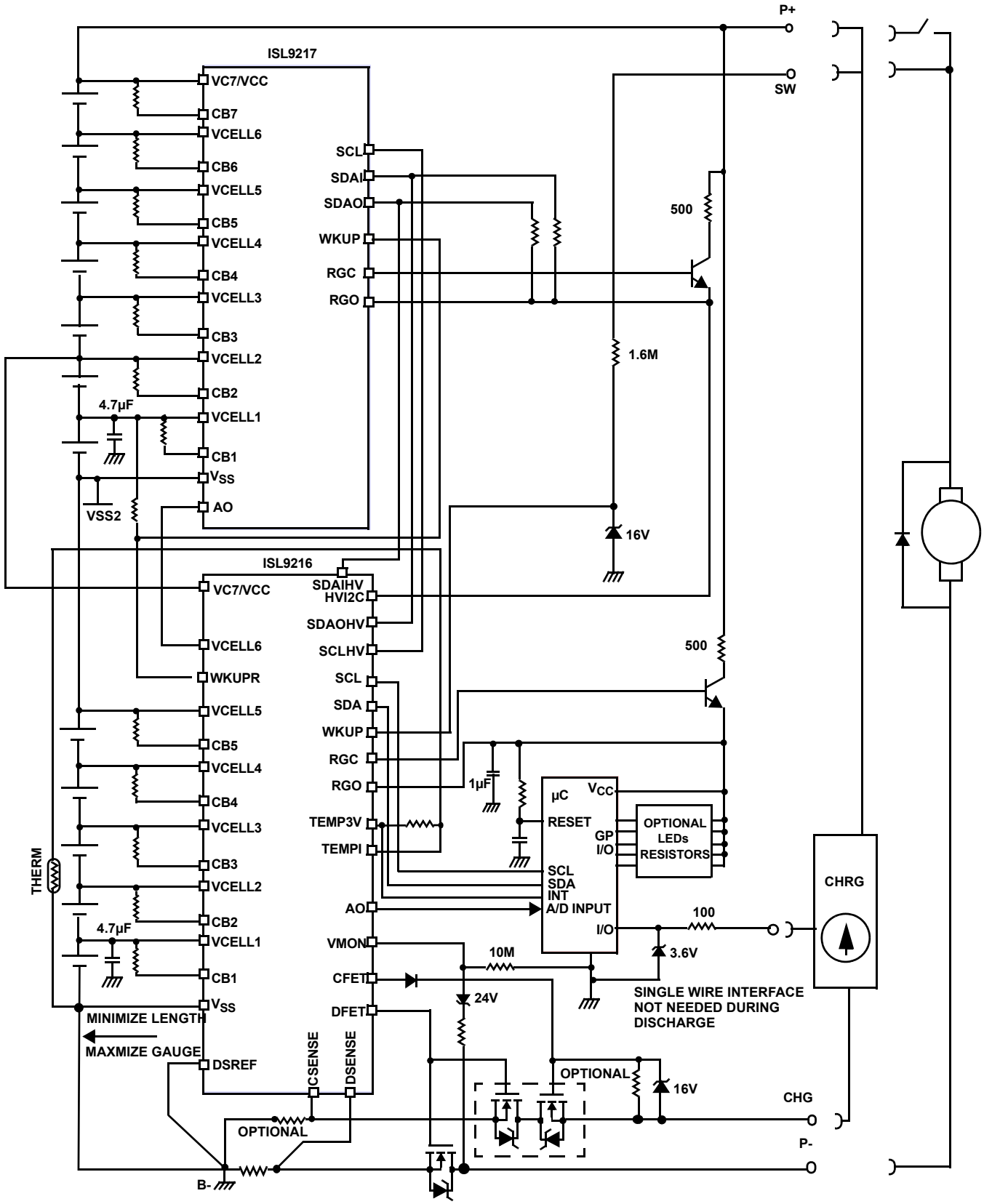
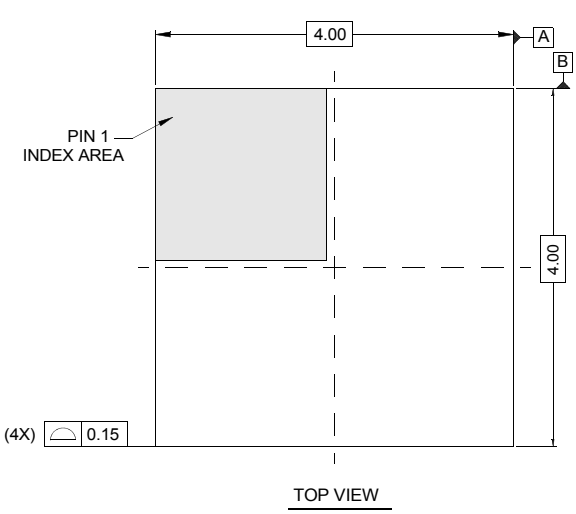


FIGURE 19. 12-CELL CASCADED APPLICATION CIRCUIT WITH SEPARATE CHARGE/DISCHARGE AND SWITCH WAKE-UP

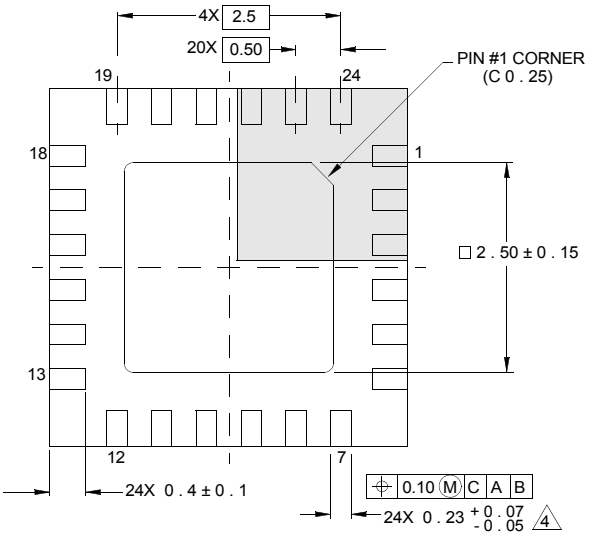
Package Outline Drawing

L24.4x4D

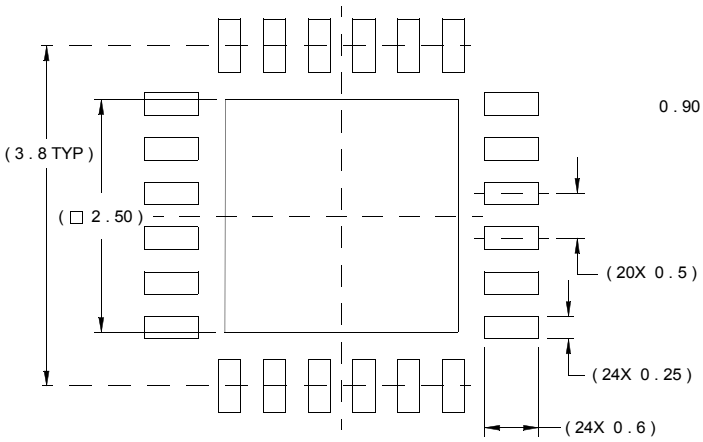
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



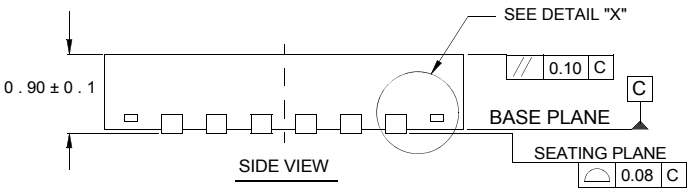
TOP VIEW



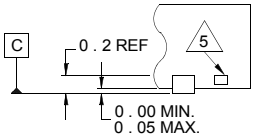
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

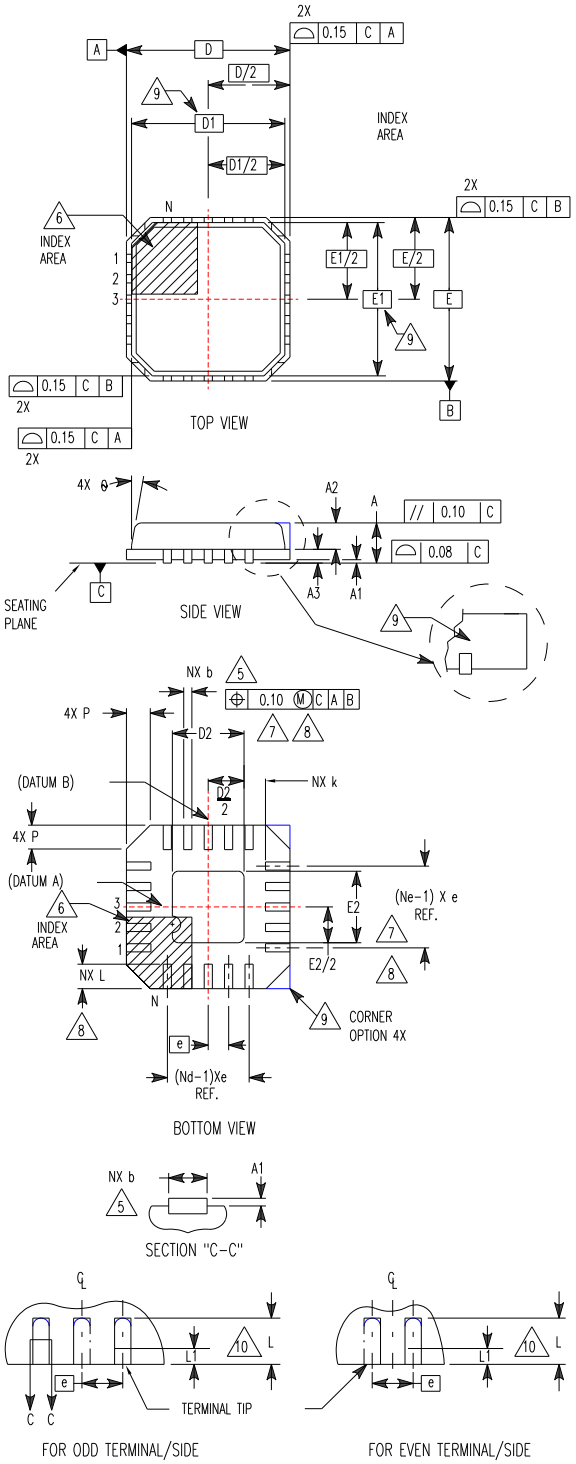


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5B

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	3.15	3.30	3.45	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	3.15	3.30	3.45	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne		8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.