Narrow VDC Regulator/Charger with SMBus Interface and Internal Switching FETs

ISL9519C

The ISL9519C is a highly integrated Narrow VDC system voltage regulator and battery charger controller. Operating parameters are programmable over the System Management Bus (SMBus). The ISL9519C is designed for applications where the system power source is either the battery pack or the output of the regulator/charger. This makes the max voltage to the system equal to the max battery voltage instead of the max adapter voltage. The ISL9519C also includes a patented system to control trickle charging deeply discharged batteries while maintaining system voltage at a user defined minimum. High efficiency is achieved with a DC/DC synchronous-rectifier buck converter, equipped with diode emulation and variable switching frequency for enhanced light load efficiency and AC-adapter boosting prevention. The ISL9519C can charge one, two or three series connected Lithium-ion cells, at up to 8A charge current. Default settings for 1-, 2- or 3-cell operation at power-up are selected by an external pin. Integrated MOSFETs, drivers and bootstrap diode result in fewer components and smaller implementation area. Low offset current-sense amplifiers provide high accuracy.

The ISL9519C provides an open drain digital output that indicates the presence of the AC-adapter. The ISL9519C also provides an analog output that indicates the adapter current.

Applications

- Notebook Computers
- Tablet PCs
- Portable Equipment with Rechargeable Batteries

Features

- ±0.5% System Voltage Accuracy (-10°C to +100°C)
- ±3% Accurate Input Current Limit
- ±3% Accurate Battery Charge Current Limit
- Variable Switching Frequency at Light Load Conditions for Higher Efficiency
- Fixed Frequency Operation at Higher Loads
  - Fixed Frequency Mode can be Forced by an External Pin
- Trickle Charge System for Deeply Discharged Batteries
  - Automatic Trickle Charge Current (256mA)
  - Holds Minimum Voltage to System
- SMBus 2-Wire Serial Interface
- Default System Voltage Values for 1-Cell, 2-Cell or 3-Cell Operation Selected by an External Pin
- Adapter In-rush FET Control
- Adapter Isolation FET Control
- Battery Short Circuit Protection
- Fast System-Load Transient Response
- Monitor Outputs
  - Adapter Current (2.5% Accuracy)
  - AC-adapter Present Indicator
- 11-Bit Max System Voltage Setting
- 7-Bit Min System Voltage Setting
- 6-Bit Charge Current Setting
  - Over 8A Battery Charger Current
- 6-Bit Adapter Current Setting
  - Over 8A Adapter Current
- +4.5V to +22V Adapter Voltage Range
- Pb-Free (RoHS Compliant)

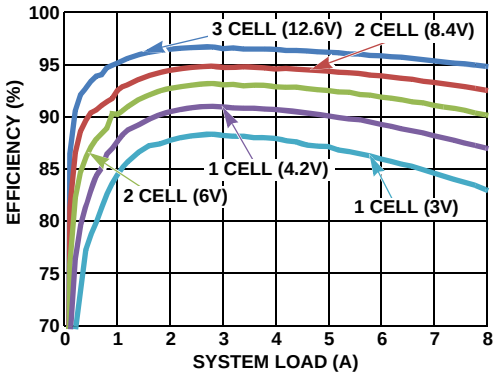


FIGURE 1. EFFICIENCY

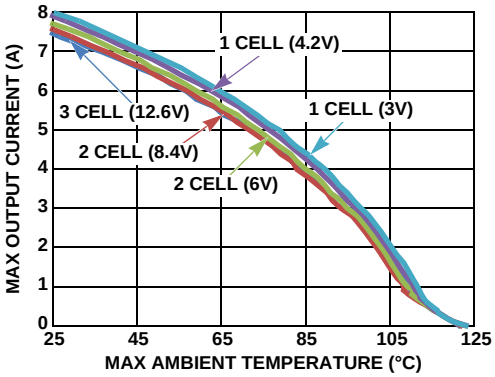


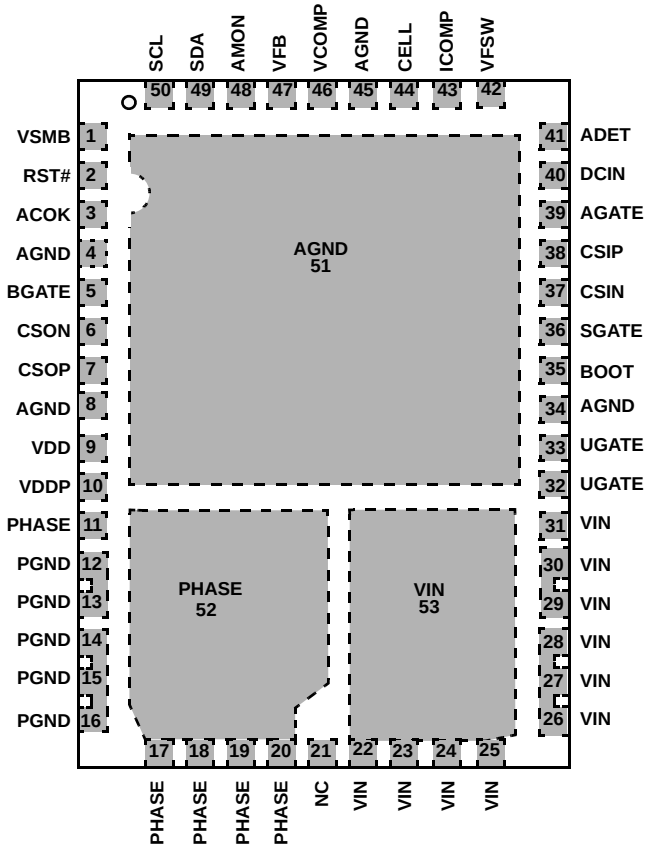
FIGURE 2. MAX LOAD CURRENT vs AMBIENT TEMPERATURE WITH 1M/s FORCED AIR COOLING

TABLE 1. ISL9519 FAMILY

PART NUMBER	LOGIC LEVELS	PIN 9 FUNCTION	DEFAULT ADAPTER CURRENT LIMIT	INTERNAL SWITCHING FETS
ISL9519	3.3V or 5V pull-up	AMON (Adapter Current Monitor)	3.584A	NO
ISL9519C	3.3V or 5V pull-up	AMON (Adapter Current Monitor)	3.584A	YES
ISL9519R	3.3V or 5V pull-up	AMON (Adapter Current Monitor)	0.128A	NO
ISL9519Q	1.8V or 2.5V pull-up	CCMON (Charge Current Monitor)	3.584A	NO

Pin Configuration

ISL9519C
(50 LD TQFN)
TOP VIEW



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	VSMB	SMBus interface Supply Voltage Input. Bypass with a 0.1µF capacitor to AGND.
2	RST#	Logic input sets all SMBus registers to default values when low.
3	ACOK	AC Detect Output. This open drain output is high impedance when ADET is greater than 3.2V. The ACOK output remains low when the ISL9519C is powered down. Connect a 10k pull-up resistor from ACOK to VSMB.
5	BGATE	Gate drive for the battery connection PFET. This pin can go high to disconnect the battery, low to connect the battery or operate in a linear mode to regulate minimum system voltage during trickle charge. It is also the compensation point for the Min System Voltage regulation loop.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
6	CSON	Charge Current-Sense Negative Input and system voltage feedback.
7	CSOP	Charge Current-Sense Positive Input.
4, 8, 34, 45, 51	AGND	Ground Connection for low power analog and digital circuits.
9	VDD	Linear Regulator Output. VDD is the output of the 5.1V linear regulator supplied from DCIN. VDD supplies regulated power input for internal analog circuits. Connect a 4.7Ω resistor from VDD to VDDP and a 1µF ceramic capacitor from VDD to AGND.
10	VDDP	VDDP directly supplies the LGATE driver and the BOOT strap diode. Bypass with a 1µF ceramic capacitor from VDDP to PGND.
11, 17, 18, 19, 20, 52	PHASE	Switching Power Output. Connect to the inductor.
12, 13, 14, 15, 16	PGND	Power Ground. Connect PGND to the system or power ground.
21	NC	NC.
22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 53	VIN	High-Side Power MOSFET Drain. Connect to the Power input and decouple with low ESR capacitors to PGND.
32, 33	UGATE	High-Side Power MOSFET Driver Output and the gate of the high side FET. Connect a 4700pF cap from UGATE to PHASE.
35	BOOT	High-Side Power MOSFET Driver Power-Supply Connection. Connect a 0.1µF capacitor from BOOT to PHASE.
36	SGATE	System Gate PFET driver. Controls the Adapter Connection FET that blocks current flow from the battery to the adapter connector.
37	CSIN	Adapter Current-Sense Negative Input.
38	CSIP	Adapter Current-Sense Positive Input.
39	AGATE	Adapter Gate (in-rush) FET control (open drain output).
40	DCIN	Charger Bias Supply Input. Bypass DCIN with a 0.1µF capacitor to AGND.
41	ADET	AC-adapter Detection Input. Connect to a resistor divider from the AC-adapter output.
42	VFSW	Logic input enables Variable Frequency Switching at light loads.
43	ICOMP	Output of the Current Control error amplifier.
44	CELL	Logic level input selects 1-cell, 2-cell or 3-cell default MaxSystemVoltage and MinSystemVoltage register values. Floating the cell pin selects 1-cell. Pulling CELL to VSMB selects 3-cell and pulling CELL low selects 2-cell defaults. The CELL pin is read only at VSMB POR or RST#.
46	VCOMP	Output of the Voltage loop error amplifier.
47	VFB	Negative input to the Min System Voltage and Max System Voltage control error amplifier.
48	AMON	Input Current Monitor Output. AMON voltage equals 20 x (V_{CSIP} - V_{CSIN}).
49	SDA	SMBus Data I/O. Open-drain Output. Connect an external pull-up resistor according to SMBus specifications.
50	SCL	SMBus Clock Input. Connect an external pull-up resistor according to SMBus specifications.
51	AGND	Connect the backside paddle to AGND and PGND (pins 8 and 12) and the system ground plane.

Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9519CHRZ	ISL 9519CHRZ	-10 to +100	50 Ld 5x7 QFN	L50.5x7B

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9519C. For more information on MSL please see techbrief TB363.

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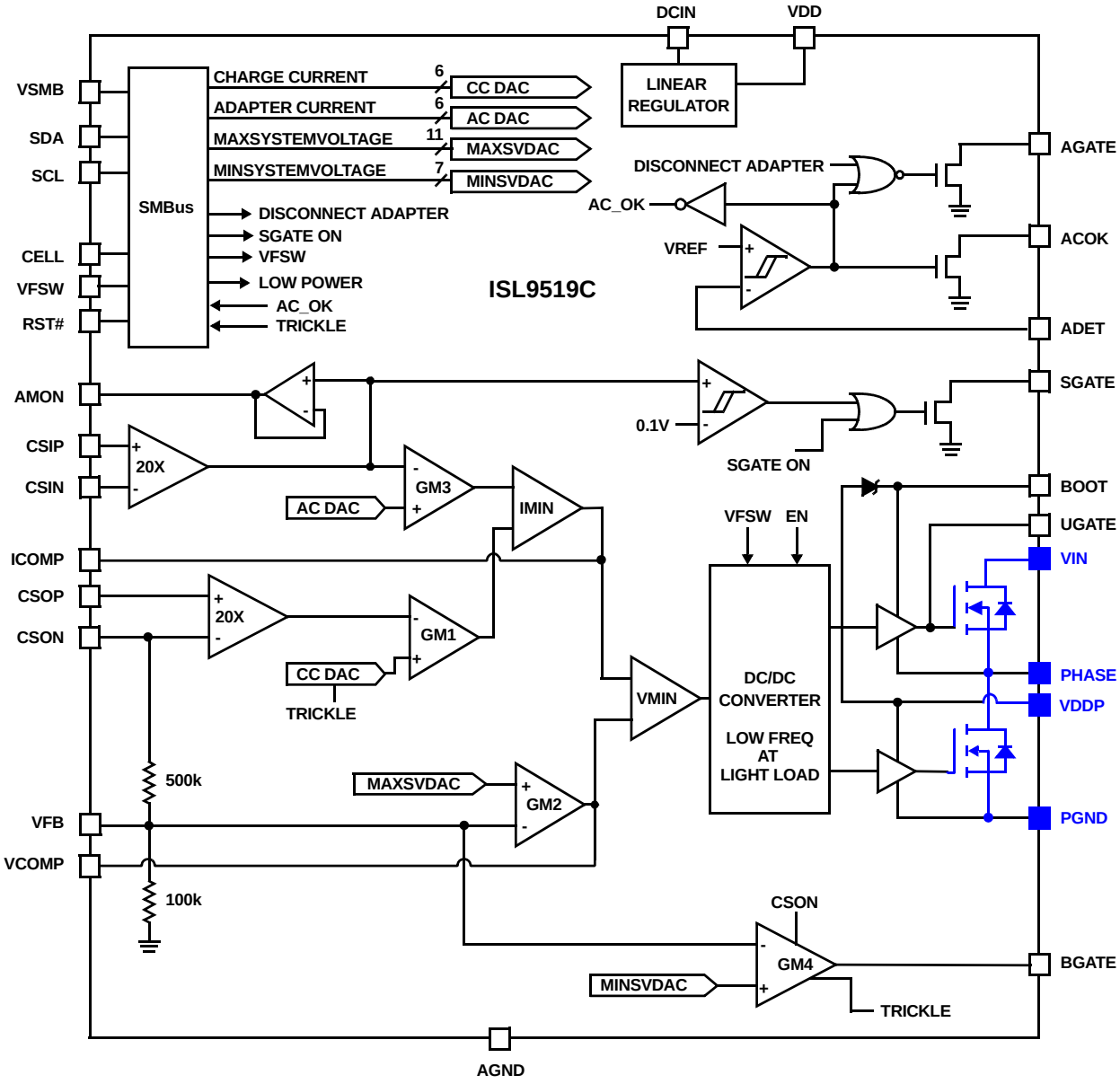


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

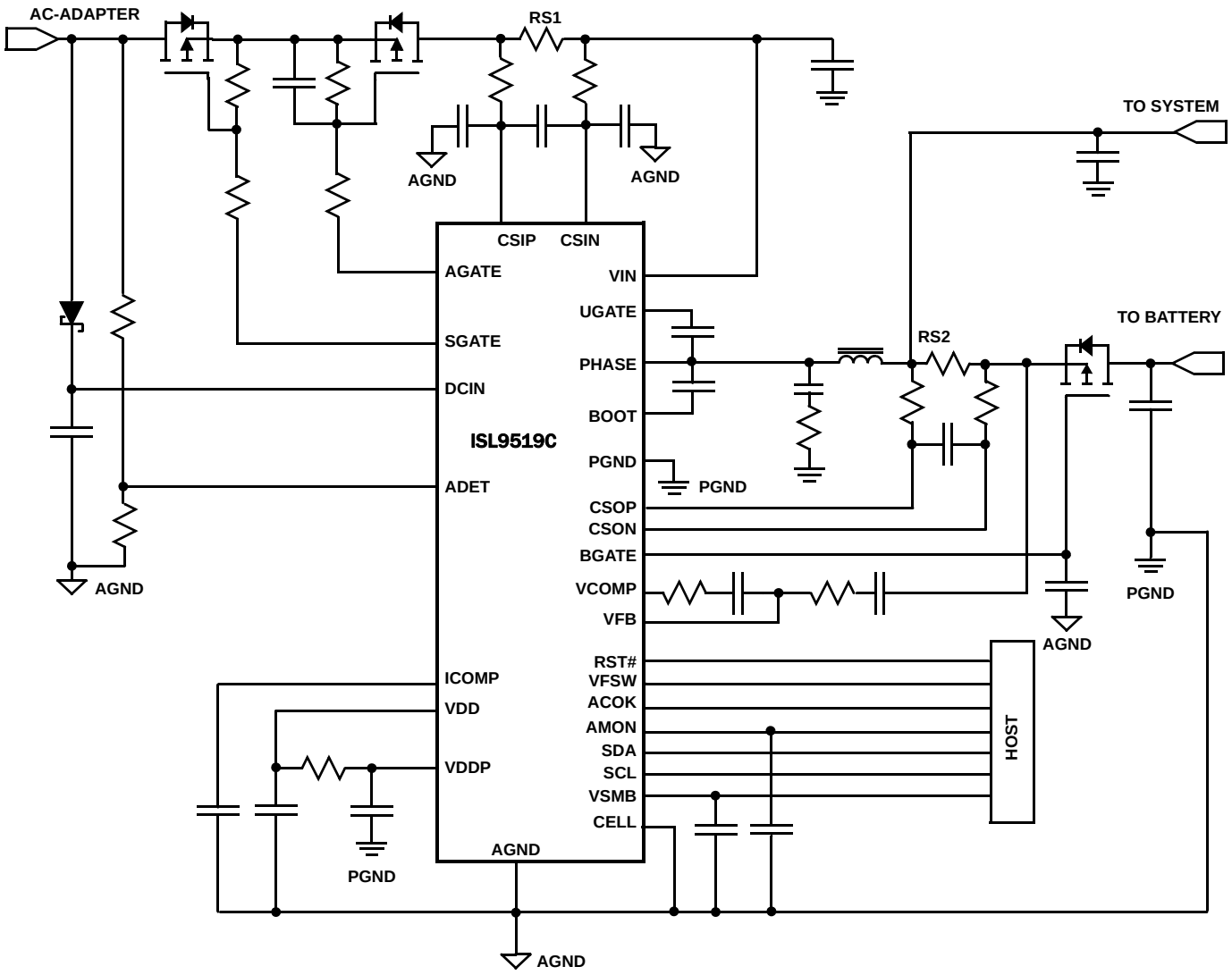


FIGURE 4. TYPICAL APPLICATION CIRCUIT

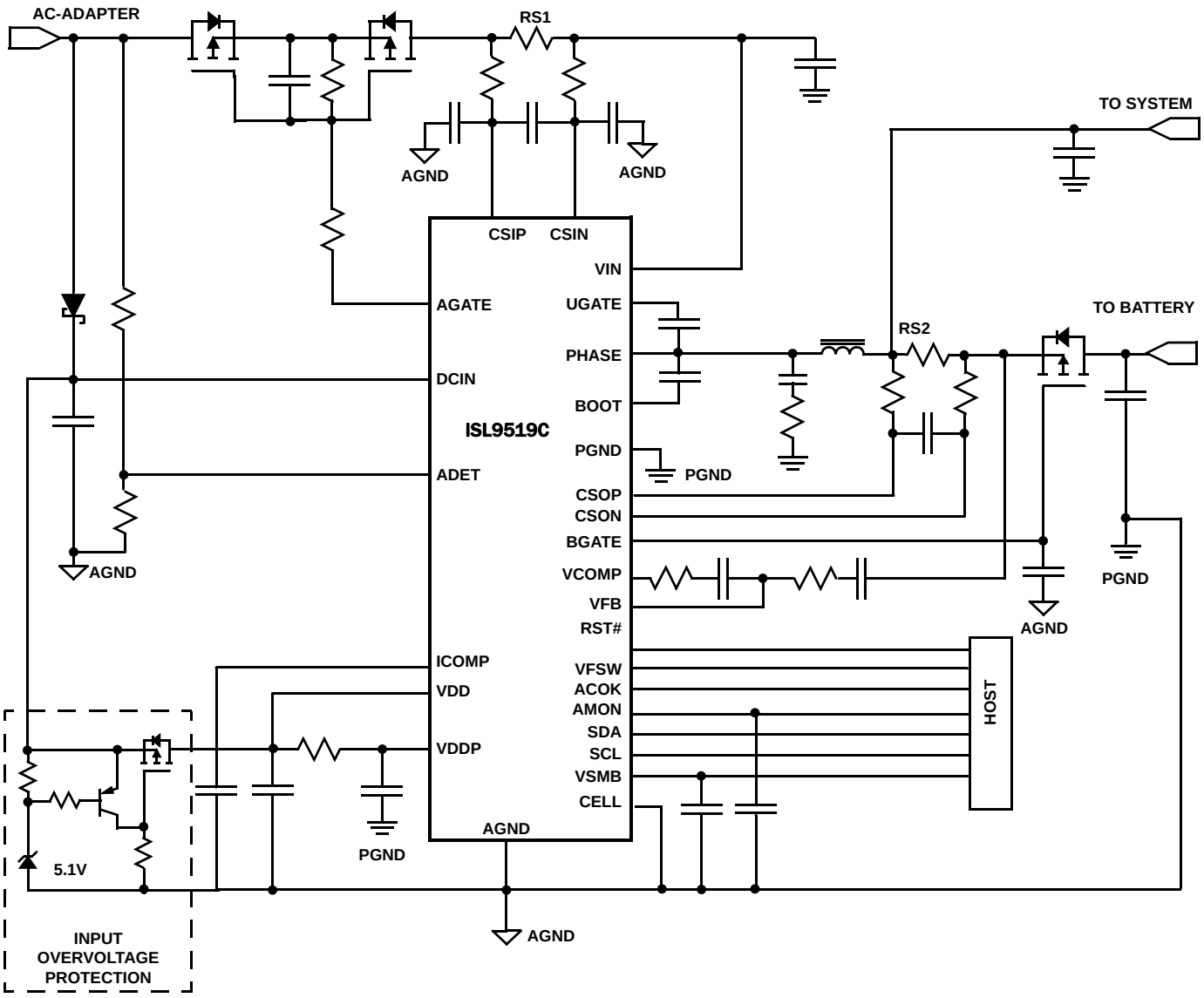


FIGURE 5. TYPICAL 5V INPUT APPLICATION CIRCUIT

Absolute Maximum Ratings

DCIN, CSIP, CSON, AGATE . . . . . -0.3V to +28V
CSIP-CSIN, CSOP-CSON, PGND-AGND- . . . . . 0.3V to +0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V
PHASE Voltage (Note 4) . . . . . PGND - 0.3V to 30V
UGATE Voltage. . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
AMON, ICOMP, VCOMP, VFB . . . . . -0.3V to VDD + 0.3V
VSMB, SCL, SDA . . . . . -0.3V to +6V
ADET, ACOK, CELL, VFSW, RST# . . . . . -0.3V to +6V
VDDP, VDD to AGND, VDDP to PGND . . . . . -0.3V to +6V
BGATE. . . . . AGND - 0.3V to CSON + 0.3V
CELL . . . . . -0.3V to VSMB + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
50 Ld TQFN Package (Notes 5, 6)	32	2

Operating Junction Temperature Range . . . . . -10°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range (see Figure 8). . . . . -10°C to +100°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. The Phase Voltage is capable of withstanding -7V when the BOOT pin is at GND.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SYSTEM VOLTAGE REGULATION					
Maximum System Voltage Accuracy	MaxSystemVoltage = 0x3130	**12.529**	12.592	**12.655**	V
		-0.5		**0.5**	%
	MaxSystemVoltage = 0x20D0	**8.358**	8.4	**8.442**	V
		-0.5		**0.5**	%
	MaxSystemVoltage = 0x1060	**4.171**	4.192	**4.213**	V
		-0.5		**0.5**	%
Minimum System Voltage Accuracy	MinSystemVoltage = 0x2400	**8.940**	9.216	**9.492**	V
		-3		**3**	%
	MinSystemVoltage = 0x1800	**5.898**	6.144	**6.390**	V
		-4		**4**	%
	MinSystemVoltage = 0x0C00	**2.888**	3.072	**3.256**	V
		6		**6**	%
CHARGE CURRENT REGULATION					
Charge Current and Accuracy	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x1f80	**7.822**	8.064	**8.306**	A
		-3		**3**	%
	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x1000	**3.973**	4.096	**4.219**	A
		-3		**3**	%
	RS2 = 10mΩ (see Figure 4) ChargingCurrent = 0x0100	**166**	256	**346**	mA
Trickle Charge Current	RS2 = 10mΩ (see Figure 4) CSON-BGATE < 4.3V or BGATE < 1V	**166**	256	**346**	mA
Trickle Charge Threshold	CSON-BGATE	**4.0**	4.7	**5.5**	V
Battery Quiescent Current	$I_{CSOP} + I_{CSON} + I_{PHASE} + I_{CSIP} + I_{CSIN} + I_{AGATE}$ $V_{PHASE} = V_{BOOT} = V_{CSON} = V_{CSOP} = V_{CSIN} = V_{CSIP} = V_{AGATE}$ = 12.6V, V_{DCIN} = VDD = VDDP = 0V		14	**25**	µA

Electrical Specifications DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
INPUT CURRENT REGULATION					
Input Current Accuracy	RS1 = 20mΩ (see Figure 4) Adapter Current = 512mA	**-7**		**7**	%
	RS1 = 20mΩ (see Figure 4) Adapter Current = 4096mA or 8064mA	**-3**		**3**	%
CSIP/CSIN Input Voltage Range		**5**		**26**	V
AMON Accuracy Ideal AMON = 20*(CSIP-CSIN)	$V_{CSIP-CSIN}$ = 161.28mV, AMON load < 1µA	**-2.5**		**2.5**	%
	$V_{CSIP-CSIN}$ = 81.92mV AMON load < 1µA	**-4**		**4**	%
	$V_{CSIP-CSIN}$ = 10.24mV, AMON load < 1µA	**-20**		**20**	%
	$V_{CSIP-CSIN}$ = 5.12mV, AMON load < 1µA	**-40**		**40**	%
AMON Min Output Voltage	$V_{CSIP-CSIN}$ = 0.0V, AMON load < 1µA		30	**80**	mV
AMON Max Source Current	$V_{CSIP-CSIN}$ = 161.28mV, V_{AMON} = 0V	**25**	40	**60**	µA
AMON Max Sink Current	$V_{CSIP-CSIN}$ = 0.0V, V_{AMON} = 2V	**25**	40	**60**	µA
SUPPLY AND LINEAR REGULATOR					
DCIN, Input Voltage Range		**6**		**26**	V
DCIN Quiescent Current	$V_{ADAPTER}$ = 5.5V to 26V, $V_{BATTERY}$ 4V to 16V		2	**5**	mA
VDD Output Voltage	6.0V < V_{DCIN} < 26V, no load	**4.975**	5.1	**5.23**	V
VDD Load Regulation	0 < I_{VDDP} < 30mA (see note 6)		35		mV
VDD UVLO Rising		**3.93**	4.0	**4.12**	V
VDD UVLO Hysteresis		**170**	235	**325**	mV
VSMB Range		**2.7**		**5.5**	V
VSMB UVLO Rising		**2.5**	2.75	**2.95**	V
VSMB UVLO Hysteresis		**75**	125	**175**	mV
VSMB Quiescent Current	VSMB = SCL = SDA = 3.42V		30	**50**	µA
VSMB Quiescent Current	VSMB = SCL = SDA = 3.42V, LOW POWER BIT = 1		14	**25**	µA
ADET					
ADET Rising Threshold		**3.15**	3.2	**3.25**	V
ADET Threshold Hysteresis		**35**	60	**90**	mV
ADET Input Leakage Current				**1**	µA
ACOK					
Sink Current	V_{ACOK} = 0.4V, ADET = 2.7V	**2**	8		mA
Leakage Current	V_{ACOK} = 5.5V, ADET = 3.7V			**1**	µA
AGATE					
Sink Current	V_{ADET} > 3.5V, AGATE = 0.4V	**1**	2.3		mA
Leakage Current	V_{ADET} = 0V, AGATE = 26V			**1**	µA
SGATE					
CSIP-CSIN Threshold for SGATE Going High			6.6	**9**	mV
CSIP-CSIN Threshold Hysteresis		**1.5**	3.3		mV
Sink Current	CSIP-CSIN > 10mV, AGATE = 0.4V	**1**	2.3		mA
Leakage Current	CSIP-CSIN = 0V, AGATE = 26V			**1**	µA

Electrical Specifications

DCIN = CSIP = CSIN = 19V, CSOP = CSON = 12V, VDDP = 5V, VSMB = 3.42V, BOOT-PHASE = 5V, AGND = PGND = 0V, CVDD = 1µF, T_A = -10°C to +100°C. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
VFSW					
VFSW Input Low Voltage				**0.8**	V
VFSW Input High Voltage		**2**			V
VFSW Input Leakage Current				**1**	µA
RST#					
Input Low Voltage	VSMB = 2.7V to 5.5V			**0.8**	V
Input High Voltage	VSMB = 2.7V to 5.5V	**2**			V
Input Leakage Current	VSMB = 2.7V to 5.5V			**1**	µA
BATTERY CELL SELECTOR					
CELL Input Voltage for 3-Cell Select		**VSMB -0.4**			V
CELL Input Voltage for 1-Cell Select		**0.85**		**VSMB -1.2**	V
CELL Input Voltage for 2-Cell Select				**0.4**	V
CELL Input Current Lo	CELL = GND, RST# = GND	**-40**			µA
CELL Input Current Hi	CELL = VSMB, RST# = GND			**40**	µA
CELL Float Voltage	CELL = Open, RST# = GND		1.23		V
CELL Input Current Hi Z	CELL = 0V or VSMB, RST# = VSMB		0.05	**1**	µA
SWITCHING REGULATOR					
Frequency 400kHz	Register 0x3D = xx1x0x00b	**330**	400	**440**	kHz
Max Variable Frequency	Register 0x3D = xx1x1x0xb, CCM load	**330**	400	**440**	kHz
Min Variable Frequency 1	Register 0x3D = xx1x1x0xb, no load		140		kHz
Min Variable Frequency 2	Register 0x3D = xx1x1x1xb, no load		80		kHz
ERROR AMPLIFIERS					
gm2 Amplifier Transconductance	Transconductance from VFB to VCOMP	**200**	250	**300**	µA/V
gm1 Amplifier Transconductance	Transconductance from (CSOP-CSON) to ICOMP	**40**	50	**60**	µA/V
gm3 Amplifier Transconductance	Transconductance from (CSIP-CSIN) to ICOMP	**40**	50	**60**	µA/V
gm4 Amplifier Transconductance	Transconductance from VFB to BGATE	**50**	100	**150**	µA/V
gm1/gm3 Saturation Current		**15**	21	**25**	µA
gm2 Saturation Current		**10**	17	**25**	µA
ICOMP, VCOMP Clamp Voltage	Max Voltage between V_{VCOMP} and V_{ICOMP}	**200**	300	**400**	mV
LOGIC LEVELS					
SDA/SCL Input Low Voltage	VSMB = 2.7V to 5.5V			**0.8**	V
SDA/SCL Input High Voltage	VSMB = 2.7V to 5.5V	**2**			V
SDA/SCL Input Bias Current	VSMB = 2.7V to 5.5V			**1**	µA
SDA, Output Sink Current	V_{SDA} = 0.4V	**4**	12		mA

SMB Timing Specification

VSMB = 2.7V to 5.5V.

PARAMETERS	SYMBOL	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SMBus Frequency	FSMB		10		100	kHz
Bus Free Time	t_{BUF}		4.7			µs

SMB Timing Specification VSMB = 2.7V to 5.5V. (Continued)

PARAMETERS	SYMBOL	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Set-up Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Set-up Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Set-up Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
SMBus Inactivity Time-out		Maximum Charging Period Without a SMBus Write to MaxSystemVoltage or ChargeCurrent Register	120	180	250	s

NOTES:

7. Limits should be considered typical and are not production tested.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Operating Performance DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted.

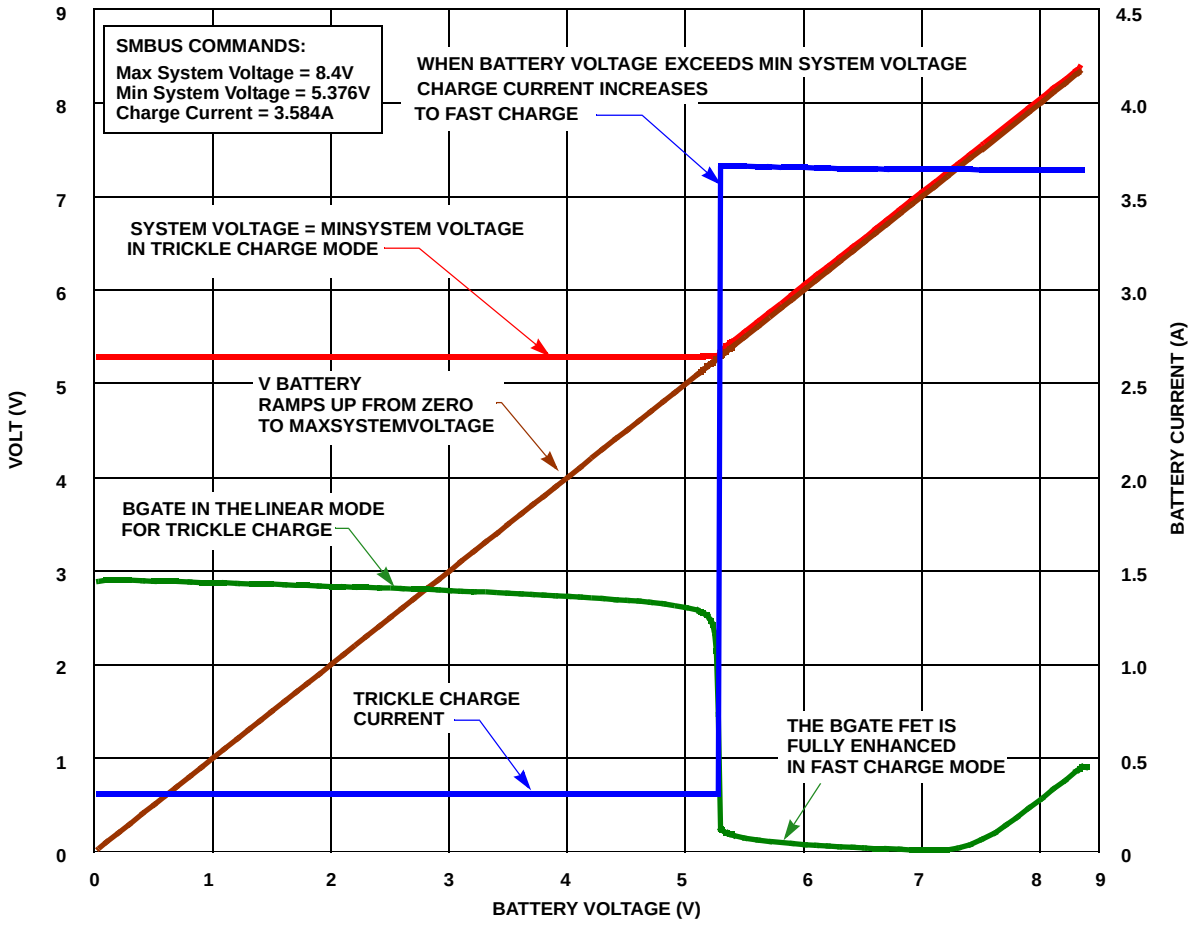


FIGURE 6. CHARGE CURRENT AND SYSTEM VOLTAGE vs BATTERY VOLTAGE

Typical Operating Performance

DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

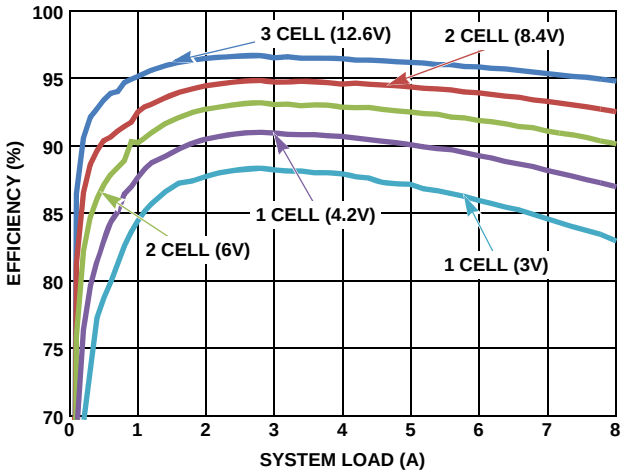


FIGURE 7. EFFICIENCY

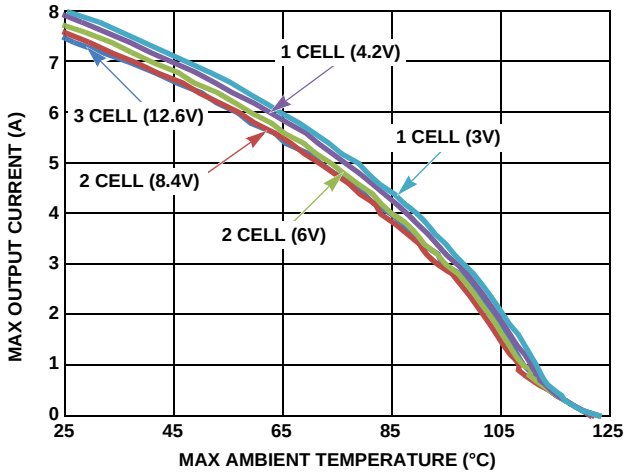


FIGURE 8. MAX LOAD CURRENT vs AMBIENT TEMPERATURE WITH 1M/s FORCED AIR COOLING

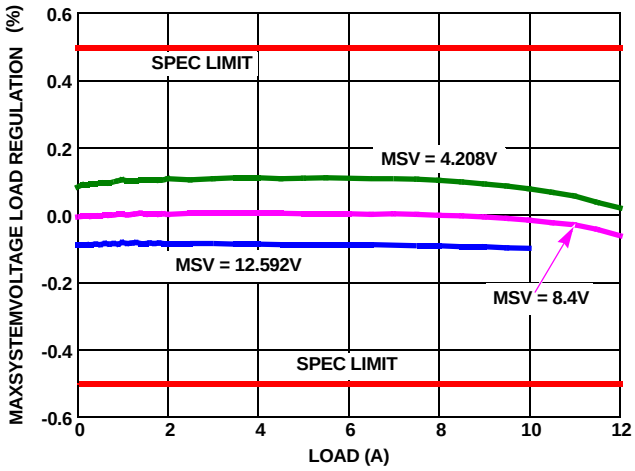


FIGURE 9. LOAD REGULATION

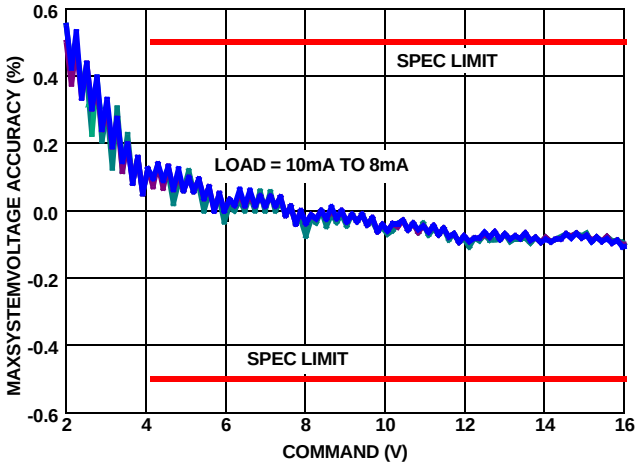


FIGURE 10. MAXSYSTEMVOLTAGE COMMAND ACCURACY

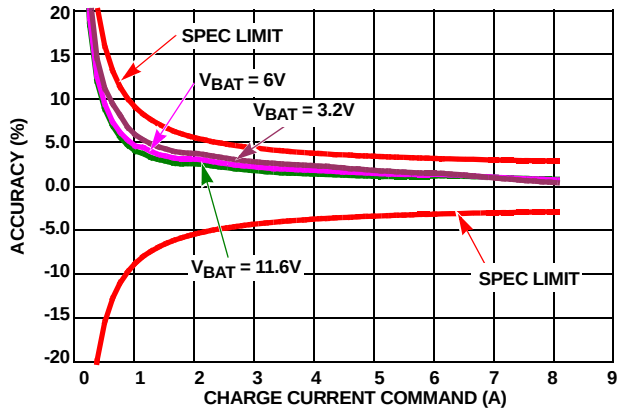


FIGURE 11. CHARGE CURRENT COMMAND ACCURACY

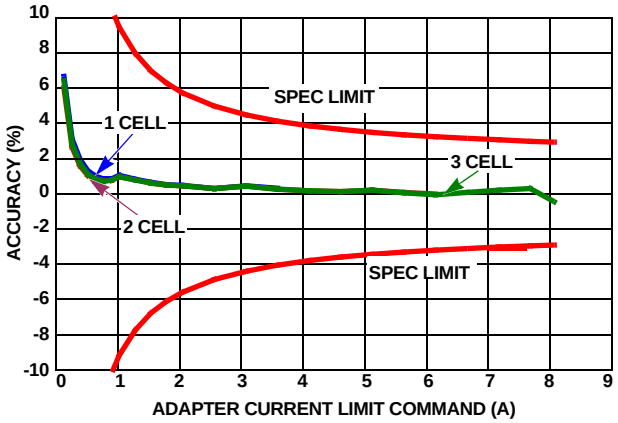


FIGURE 12. ADAPTER CURRENT LIMIT ACCURACY

Typical Operating Performance

DCIN = 20V, 2S2P Li-Battery, T_A = +25°C, unless otherwise noted. **(Continued)**

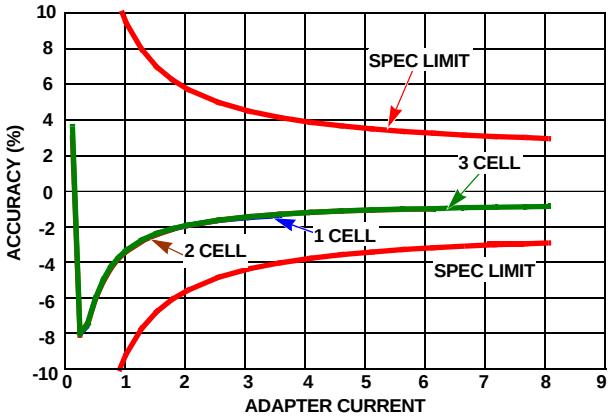


FIGURE 13. AMON ACCURACY

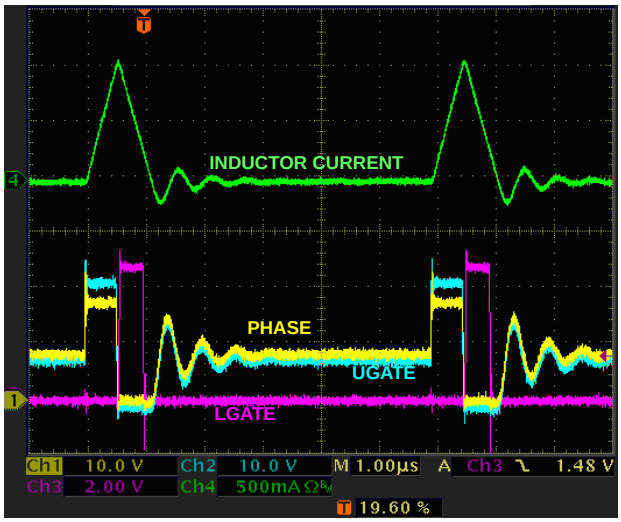


FIGURE 14. LIGHT LOAD, LOW FREQUENCY SWITCHING WAVEFORMS (LGATE IS INTERNAL)

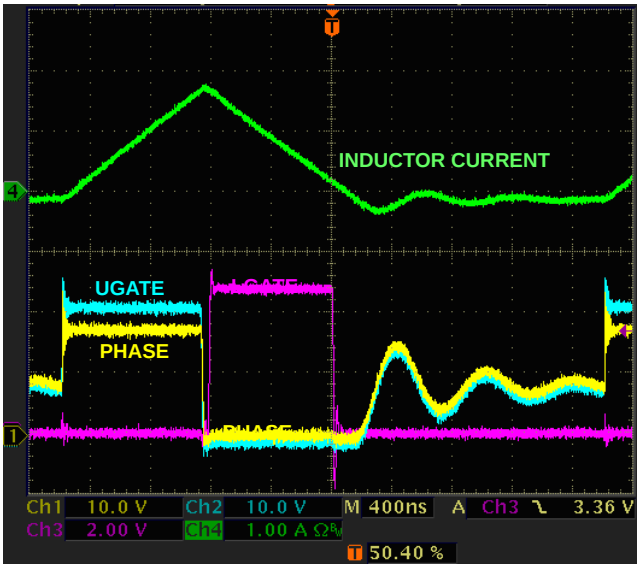


FIGURE 15. SWITCHING WAVEFORMS IN DISCONTINUOUS CONDUCTION MODE (LGATE IS INTERNAL)

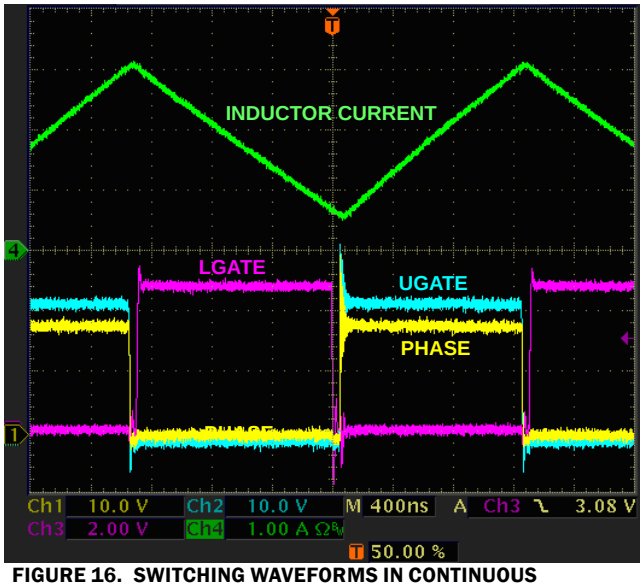


FIGURE 16. SWITCHING WAVEFORMS IN CONTINUOUS CONDUCTION MODE (LGATE IS INTERNAL)

Theory of Operation

Introduction

A high efficiency synchronous buck converter is used to control the system voltage up to 16.368V and charging current up to 6A. The ISL9519C also has input current limiting up to 8.064A (or higher with lower values of sense resistor). The Input current limit, charge current limit, minimum and maximum system voltage are set by internal registers written with SMBus. The ISL9519C “Typical Application Circuit” on page 6 is depicted in Figure 4.

The ISL9519C charges the battery with constant charge current, set by the ChargeCurrent register, until the battery voltage rises to a voltage set by the MaxSystemVoltage register. The charger will then operate at a constant voltage. The adapter current is monitored and if the adapter current rises to the limit set by the InputCurrent register, system voltage and battery charge current are reduced to limit adapter current. If battery voltage is below the min system voltage, the trickle charge system is activated.

The ISL9519C features two voltage regulation loops and two current regulation loops. The max system voltage loop controls the voltage at CSON with a precision voltage divider to the voltage error amplifier GM2. The min system voltage prevents the system voltage from dropping below a minimum value even if a deeply discharged battery is inserted that is below the minimum. The Charge Current regulation loop limits the battery charging current delivered to the battery to ensure that it never exceeds the current set by the ChargeCurrent register. The Input Current regulation loop limits the current drawn from the AC-adapter to ensure that it never exceeds the limit set by the InputCurrent register to prevent adapter overload.

PWM Control

The ISL9519C employs a variable frequency pulse width modulator (PWM) with feed-forward. The switching frequency is constant in Continuous Conduction Mode (CCM) but is reduced in Discontinuous Mode (DCM). Switching frequency can be fixed by setting bits in the control register and/or pulling the VFSW pin low.

AC-Adapter Detection

AC-adapter voltage is connected through a resistor divider to ADET to detect when AC power is available, as shown in Figure 4. ACOK is an open-drain output and is active low when ADET is less than $V_{th,fall}$, and high Z when ADET is above $V_{th,rise}$. The ADET rising threshold is 3.2V (typ) with 57mV hysteresis. ADET must be above the threshold to enable the output voltage.

VDD Regulator

VDD provides a 5.1V supply voltage from the internal LDO regulator from DCIN and can deliver up to 30mA of continuous current. VDD also supplies power to VDDP through a low pass filter, as shown in the "Typical Application Circuit" on page 6 in Figure 4. The MOSFET drivers are powered by VDDP. Bypass VDDP and VDD with a 1µF capacitor.

VSMB Supply

The VSMB input provides power to the SMBus interface. Connect an external supply to VSMB to keep the SMBus interface active while the supply to DCIN is removed. When VSMB is biased, the internal registers are maintained. Bypass VSMB to AGND with a 0.1µF or greater ceramic capacitor.

Current Measurement

AMON is an output voltage that is proportional to the adapter current being sensed across CSIP and CSIN. The output voltage range is 0.1V to 3.2V. The voltage of AMON is given by Equation 1:

$$AMON = 20 \cdot I_{INPUT} \cdot R_{S1} \quad \text{(EQ. 1)}$$

Where I_{INPUT} is the DC current drawn from the AC-adapter. A capacitor is required at the AMON output to stabilize the AMON amplifier and to minimize switching noise.

SGATE Function

SGATE is the System Isolation FET. The SGATE pin pulls low to turn an external PFET ON when current flowing from the adapter to the system exceeds a threshold (see "Electrical Specifications" table on page 9). SGATE is high (open drain) when the adapter current drops below the threshold. When the SGATE FET is OFF, its body diode blocks current flow from the system to the adapter connector.

AGATE Function

AGATE controls the Adapter Isolation FET. The AGATE pin pulls low to turn an external PFET ON when adapter voltage is above a threshold set by resistor divider to ADET. AGATE is high (open drain) when ADET is less than 3.2V. When the AGATE FET is OFF, its body diode blocks current flow from the adapter to the system. A capacitor between the gate and source of the AGATE FET can slow the turn-on of the FET and reduce in-rush current. The AGATE FET can be forced OFF by the ISLOLATE_ADAPTER bit in the control register.

BGATE Function

The BGATE pin drives the gate of an external PFET to control the minimum system voltage. If a battery is connected that is discharged below the value set in the MinSystemVoltage register, BGATE controls the system voltage at the value set in the MinSystemVoltage register.

Trickle Charging

If a battery that is discharged below the value set in the MinSystemVoltage register is connected to the system, the trickle charge system is activated. In trickle charge mode, the charge current is reduced to 256mA. The value in the ChargeCurrent register is not changed. The BGATE FET is controlled in a linear mode to regulate the system voltage at min system voltage and to drop voltage between the min system voltage and the battery. This state is communicated to the host system by the trickle bit in the control register.

When the battery is charged to the min system voltage, the BGATE FET becomes fully enhanced and BGATE is pulled more than 4.5V below the system voltage or to ground in a 1-cell application. This changes the charge mode from trickle to fast charge. The charge current is increased to the value in the ChargeCurrent register. The trickle bit in the control register is set to 0.

Short Circuit Protection and 0V Battery Charging

If a battery is connected that is completely discharged or a short circuit, the trickle charge system is activated. The Charge Current is reduced to 256mA and BGATE controls the BGATE FET to maintain system voltage at the value in the MinSystemVoltage register.

Over-Temperature Protection

If the die temperature exceeds +150°C, it turns both of the synchronous buck FETs off. The system bus and the battery charging are disabled. Once the die temp drops below +125°C, system bus regulation and battery charging will start-up again.

The System Management Bus

The System Management Bus (SMBus) is a 2-wire bus that supports bidirectional communications. The protocol is described briefly here. More detail is available from http://www.smbus.org.

General SMBus Architecture

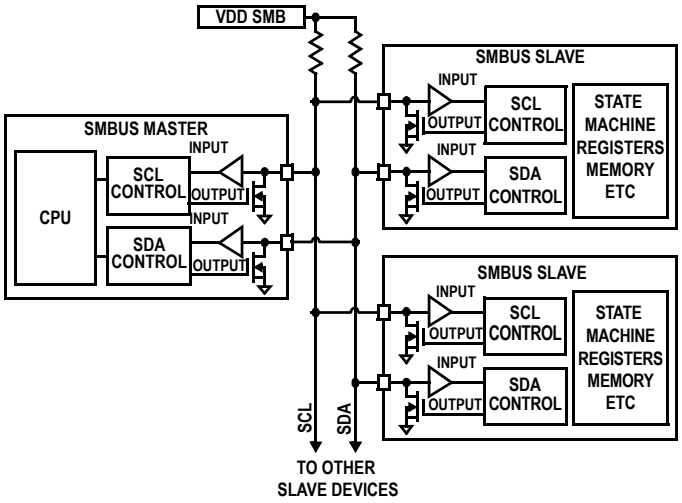


FIGURE 17.

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 18.

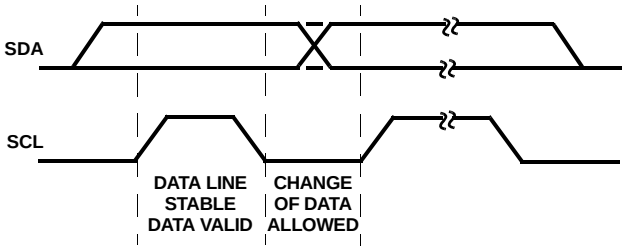


FIGURE 18. DATA VALIDITY

START and STOP Conditions

As shown in Figure 19, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

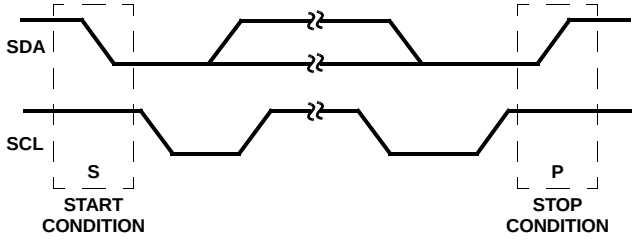


FIGURE 19. START AND STOP WAVEFORMS

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends 7 slave address bits and a R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (as shown in Figure 20). The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

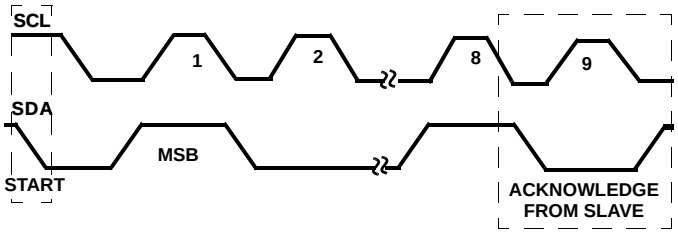


FIGURE 20. ACKNOWLEDGE ON THE SMBus

SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition, followed by 7-bits of slave address (0001001 for the ISL9519C) followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the SMBus bus recognize their address, they will acknowledge by pulling the serial data (SDA) line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition.

Once the control byte is sent, and the ISL9519C acknowledges it, the 2nd byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9519C which register the master will write or read. See Table 2 for details of the registers. Once the ISL9519C receives a register address byte it responds with an acknowledge.

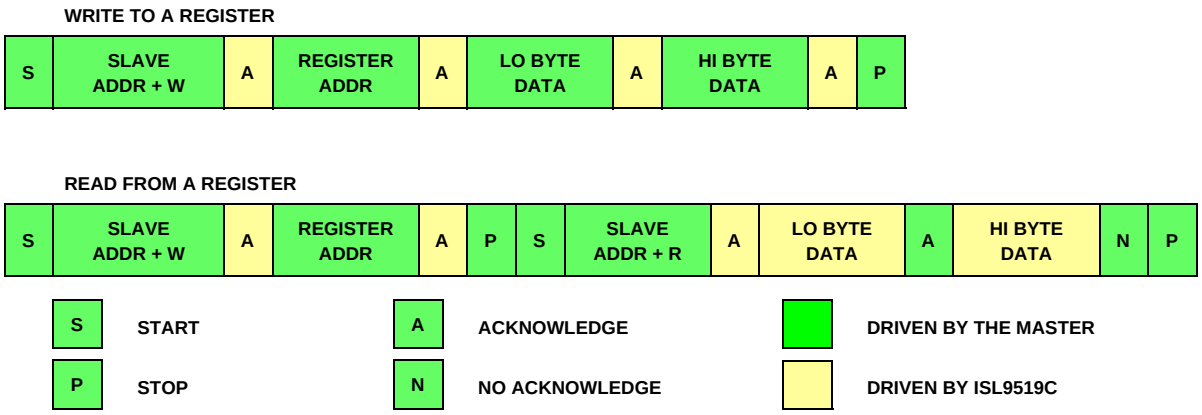


FIGURE 21. SMBus/ISL9519C READ AND WRITE PROTOCOL

TABLE 2. ISL9519C REGISTER SUMMARY

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	ISL9519C (1-CELL) POR STATE	ISL9519C (2-CELL) POR STATE	ISL9519C (3-CELL) POR STATE
0x14	ChargeCurrent	Read or Write	6-Bit Charge Current Setting	0x0000 = 0A	0x0000 = 0A	0x0000 = 0A
0x15	MaxSystemVoltage	Read or Write	11-Bit MaxSystemVoltage Setting	0x1000 = 4.096V	0x2000 = 8.192V	0x3000 = 12.288V
0x3D	Control	Read or Write	8-Bit Control bit register	0x0000	0x0000	0x0000
0x3E	MinSystemVoltage	Read or Write	7-Bit MinSystemVoltage Setting	0x0C00 = 3.072V	0x1800 = 6.144V	0x2400 = 9.216V
0x3F	InputCurrent	Read or Write	6-Bit Input Current Setting	0x0E00 = 3.584A	0x0E00 = 3.584A	0x0E00 = 3.584A
0xFE	ManufacturerID	Read Only	Manufacturer ID	0x0049	0x0049	0x0049
0xFF	DeviceID	Read Only	Device ID	0x0003	0x0003	0x0003

Byte Format

Every byte put on the SDA line must be 8-bits long and must be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB). The LO BYTE data is transferred before the HI BYTE data.

ISL9519C and SMBus

The ISL9519C receives control inputs from the SMBus interface. The serial interface complies with the SMBus protocols as documented in the ISL9519C system Management Bus Specification V1.1, which can be downloaded from http://www.smbus.org. The ISL9519C uses the SMBus Read-Word and Write-Word protocols (see Figure 21) to communicate with the host system and a smart battery. The ISL9519C is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001_ (0x12).

Read address = 0b00010011 and

Write address = 0b00010010.

In addition, the ISL9519C has two identification (ID) registers: a 16-bit device ID register (0xFF) and a 16-bit manufacturer ID register (0xFE).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications. The ISL9519C is controlled by the data written to the registers described in Table 2.

SMBus Registers

The ISL9519C supports 7 internal registers (described in Table 2) that use either Write-Word or Read-Word protocols (see Figure 21). ManufacturerID and DeviceID are “read only” registers and can be used to identify the ISL9519C. On the ISL9519C, ManufacturerID always returns 0x0049 (ASCII code for “I” for Intersil) and DeviceID always returns 0x0003.

Setting Max System Voltage

Max system voltage is set by writing a valid 16-bit number to the 16-bit MaxSystemVoltage register. The ISL9519C ignores the first 4 LSBs and uses the next 11 bits to set the voltage DAC. The max system voltage range of the ISL9519C is limited by the number of cells selected at the CELL pin. The maximum accepted commands for 1, 2, and 3 cells are listed in Table 4. Numbers requesting max system voltage greater than the value in Table 4 are ignored. The SMBus communication is not acknowledged (NAK) and the MaxSystemVoltage register is unchanged. The minimum command is 1.024V. All numbers requesting max system voltage below 1.024V result in a voltage set point of zero, which turns off the regulator.

The trickle charge system is activated when the BGATE FET is in its active region. Fast charging is active when the BGATE FET is fully enhanced (CSON-BGATE > 4.5V OR BGATE < 0.8V).

TABLE 3. MAXSYSTEMVOLTAGE (REGISTER 0x15)

BIT	BIT NAME	DESCRIPTION
0 to 3		Not used.
4	MaxSystemVoltage, MAXSVDAC 0	0 = Adds 0mV of charger voltage, 1 = Adds 16mV of charger voltage. 1024mV minimum
5	MaxSystemVoltage, MAXSVDAC 1	0 = Adds 0mV of charger voltage, 1 = Adds 32mV of charger voltage. 1024mV minimum
6	MaxSystemVoltage, MAXSVDAC 2	0 = Adds 0mV of charger voltage, 1 = Adds 64mV of charger voltage. 1024mV minimum
7	MaxSystemVoltage, MAXSVDAC 3	0 = Adds 0mV of charger voltage, 1 = Adds 128mV of charger voltage. 1024mV minimum
8	MaxSystemVoltage, MAXSVDAC 4	0 = Adds 0mV of charger voltage, 1 = Adds 256mV of charger voltage. 1024mV minimum
9	MaxSystemVoltage, MAXSVDAC 5	0 = Adds 0mV of charger voltage, 1 = Adds 512mV of charger voltage. 1024mV minimum
10	MaxSystemVoltage, MAXSVDAC 6	0 = Adds 0mA of charger voltage. 1 = Adds 1024mV of charger voltage.
11	MaxSystemVoltage, MAXSVDAC 7	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	MaxSystemVoltage, MAXSVDAC 8	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	MaxSystemVoltage, MAXSVDAC 9	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14		Not Used. Normally a 16384mV weight
15		Not used. Normally a 32768mV weight.

Upon initial power-up of the VSMB supply, the MaxSystemVoltage register is reset to the POR value in Table 3. Use the Write-Word protocol (Figure 21) to write to the MaxSystemVoltage register. The register address for MaxSystemVoltage is 0x15. The 16-bit binary number formed by D15-D0 represents the max system voltage set point in mV. However, the resolution of the ISL9519C is 16mV because the D0-D3 bits are ignored, as shown in Table 3. The D14 and D15 bits are ignored because they are not needed to span the accepted range. Table 3 shows the mapping between the 16-bit number written to the MaxSystemVoltage register and max system voltage set point. The MaxSystemVoltage register can be read back to verify its contents.

Smart Battery Registers

The MaxSystemVoltage and ChargeCurrent registers use addresses and the format defined in the Smart Battery Charger Specification (Level 2) for ChargeVoltage and ChargeCurrent. In some systems, the Smart Battery Pack may write commands to these registers in ISL9519C. If a Smart Battery is used with ISL9519C, please refer to the Smart Battery Charger Specification for details.

Max Accepted Max System Voltage Command

Commands that produce system voltage far higher than normal cell voltage are ignored. The max accepted MaxSystemVoltage commands depend on the CELL pin. Table 4 gives the maximum command that is accepted for 1, 2 and 3 cells.

TABLE 4. MAX ACCEPTED MAX SYSTEM VOLTAGE COMMAND

# OF CELLS	MAX ACCEPTED COMMAND	MIN IGNORED COMMAND
1 (CELL = floating)	0x17F0 (6.128V)	0x1800
2 (CELL = GND)	0x27F0 (10.224V)	0x2800
3 (CELL = VSMB)	0x3FF0 (16.368V)	0x4000

Setting Minimum System Voltage

Minimum System Voltage is set by writing a valid 16-bit number to the MinSystemVoltage register. This 16-bit number translates to a 65.535V full-scale voltage. The ISL9519C ignores the first 8 LSBs and uses the next 7 bits to set the MinSystemVoltage DAC. The minimum system voltage range of the ISL9519C is 0V to 19.2V. Numbers requesting minimum system voltage greater than 19.2V result in a minimum system voltage of 19.2V.

Upon initial power-up of the VSMB supply, the MinSystemVoltage register is reset to the POR value in Table 3. Use the Write-Word protocol (Figure 21) to write to the MinSystemVoltage register. The register address for MinSystemVoltage is 0x3E. The 16-bit binary number formed by D15-D0 represents the min system voltage set point in mV. However, the resolution of the ISL9519C is 256mV because the D0-D7 bits are ignored, as shown in Table 5. The D15 bit is also ignored because it is not needed to span the 0V to 19.2V range. Table 5 shows the mapping between the 16-bit number written to the MinSystemVoltage register and the min system voltage set point. The MinSystemVoltage register can be read back to verify its contents.

TABLE 5. MIN SYSTEM VOLTAGE (REGISTER 0x3E)

BIT	BIT NAME	DESCRIPTION
0 to 7		Not used.
8	MinSystemVoltage, MINSVDAC 0	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 256mV of charger voltage.
9	MinSystemVoltage, MINSVDAC 1	0 = Adds 0mV of charger voltage, 1024mV minimum 1 = Adds 512mV of charger voltage.
10	MinSystemVoltage, MINSVDAC 2	0 = Adds 0mA of charger voltage. 1 = Adds 1024mV of charger voltage.
11	MinSystemVoltage, MINSVDAC 3	0 = Adds 0mV of charger voltage. 1 = Adds 2048mV of charger voltage.
12	MinSystemVoltage, MINSVDAC 4	0 = Adds 0mV of charger voltage. 1 = Adds 4096mV of charger voltage.
13	MinSystemVoltage, MINSVDAC 5	0 = Adds 0mV of charger voltage. 1 = Adds 8192mV of charger voltage.
14	MinSystemVoltage, MINSVDAC 6	Not used.
15	-	Not used.

TABLE 6. CHARGECURRENT (REGISTER 0x14) (10mΩ SENSE RESISTOR, RS2)

BIT	BIT NAME	DESCRIPTION
0 to 6		Not used.
7	Charge Current, CCDAC 0	0 = Adds 0mA of charger current. 1 = Adds 128mA of charger current. (RS2 = 10mΩ)
8	Charge Current, CCDAC 1	0 = Adds 0mA of charger current. 1 = Adds 256mA of charger current. (RS2 = 10mΩ)
9	Charge Current, CCDAC 2	0 = Adds 0mA of charger current. 1 = Adds 512mA of charger current. (RS2 = 10mΩ)
10	Charge Current, CCDAC 3	0 = Adds 0mA of charger current. 1 = Adds 1024mA of charger current. (RS2 = 10mΩ)
11	Charge Current, CCDAC 4	0 = Adds 0mA of charger current. 1 = Adds 2048mA of charger current. (RS2 = 10mΩ)
12	Charge Current, CCDAC 5	0 = Adds 0mA of charger current. 1 = Adds 4096mA of charger current, (RS2 = 10mΩ) 8064mA maximum
13 to 15		Not used.

BGATE and 1 Cell Operation

When operating with a 1 cell battery, the BGATE FET must have a low threshold voltage (V_{TH}) and low r_{DSON} with V_{GS} = 2.5V. The V_{GS} at 256mA must be less than the programmed MinSystemVoltage -1.2V. For example, if the minimum system voltage is 3.072V, the BGATE FETs V_{GS} at ID = 256mA must be less than 1.872V (i.e., 3.072V-1.2V).

If the BGATE FETs V_{TH} is over 2V, and the minimum system voltage is 3.072V, BGATE will pull below 1.2V in the linear mode, and may not switch ISL9519C to trickle charge current.

Setting Charge Current

The ISL9519C has a 16-bit ChargeCurrent register that sets the battery charging current. The ISL9519C controls the charge current by controlling the CSOP-CSON voltage. The register's LSB translates to 10µV at CSON-CSOP. With a 10mΩ charge current R_{sense} resistor (RS2 in the "Typical Application Circuit" on page 6), the LSB translates to 1mA charge current. The ISL9519C ignores the first 7 LSBs and uses the next 6-bits to control the current DAC.

The charge-current range of the ISL9519C is 0A to 8.064A (using a 10mΩ current-sense resistor). All numbers requesting charge current above 8.064A result in a current setting of 8.064A. All numbers requesting charge current between 0mA to 128mA result in a current setting of 0mA. After initial power-up of VSMB, the ChargeCurrent register is reset to 0x0000, BGATE is high (BGATE FET is OFF) and charging is disabled. To charge the battery, write a valid, non-zero number to the ChargeCurrent register. The ChargeCurrent register uses the Write-Word protocol (Figure 21). The register code for ChargeCurrent is 0x14 (0b00010100). Table 6 shows the mapping between the 16-bit ChargeCurrent number and the charge current set point. The ChargeCurrent register can be read back to verify its contents.

Setting Input Current Limit

When the input current exceeds the set input current limit, the ISL9519C decreases the charge current to provide priority to system load current. As the system load rises, the available charge current drops linearly to zero. Higher system loads can be drawn from the battery. If the battery is not present, the system voltage is reduced to supply more system current at the same input current. The total input current can increase to the limit of the AC-adapter.

The internal amplifier compares the differential voltage between CSIP and CSIN to a scaled voltage set by the InputCurrent register. The total input current is a function of battery charge current, system load current, V_{OUT}, V_{IN} and efficiency. The total input current can be estimated by Equation 2:

$$I_{INPUT} = (I_{SYSTEM} + I_{BATTERY}) \times V_{SYSTEM} / (\eta \times V_{INPUT}) \quad \text{(EQ. 2)}$$

Where η is the efficiency of the DC/DC converter (typically 90% to 95%).

The ISL9519C has a 16-bit InputCurrent register that translates to a 1mA LSB and a 65.53A full scale current using a 20mΩ current-sense resistor (RS1 in Figure 4). Equivalently, the 16-bit Input Current number sets the voltage across CSIP and CSIN inputs in 20µV per LSB increments. To set the input current limit, use the SMBus to write a 16-bit InputCurrent register using the data format listed in Table 7. The InputCurrent register uses the Write-Word protocol (see Figure 21). The register code for InputCurrent is 0x3F (0b00111111). The InputCurrent register can be read back to verify its contents.

The ISL9519C ignores the first 7 LSBs and uses the next 6-bits to control the input current DAC. The input current range of the ISL9519C is from 128mA to 8.064A. All 16-bit numbers requesting input current above 8.064A result in an input-current setting of 8.064A. The default input current limit setting at power on of VSMB is the POR value in Table 2 on page 16.

TABLE 7. INPUT CURRENT (REGISTER 0x3F) (20mΩ SENSE RESISTOR, RS1)

BIT	BIT NAME	DESCRIPTION
0 to 6		Not used.
7	Input Current, ACDAC 0	0 = Adds 0mA of input current. 1 = Adds 128mA of input current. (RS1 = 20mΩ)
8	Input Current, ACDAC 1	0 = Adds 0mA of input current. 1 = Adds 256mA of input current. (RS1 = 20mΩ)
9	Input Current, ACDAC 2	0 = Adds 0mA of input current. 1 = Adds 512mA of input current. (RS1 = 20mΩ)
10	Input Current, ACDAC 3	0 = Adds 0mA of input current. 1 = Adds 1024mA of input current. (RS1 = 20mΩ)
11	Input Current, ACDAC 4	0 = Adds 0mA of input current. 1 = Adds 2048mA of input current. (RS1 = 20mΩ)
12	Input Current, ACDAC 5	0 = Adds 0mA of input current. 1 = Adds 4096mA of input current. (RS1 = 20mΩ) 8064mA maximum
13 to 15		Not used.

TABLE 8. CONTROL REGISTER (REGISTER 0x3D)

BIT	BIT NAME	DESCRIPTION
0	S_{GATE}ON	S_{GATE} ON = 1 forces ISL9519C to turn the SGATE FET ON. S_{GATE} ON = 0 allows ISL9519C to turn SGATE OFF if adapter current in below a min threshold
1	80kHz	When ISL9519C is in variable frequency mode, 80kHz = 1 sets min frequency to 80kHz. 80kHz = 0 sets min frequency to 140kHz
2	Isolate Adapter	Isolate Adapter = 1 disconnects the adapter from the charger by making the AGATE pin HI Z. Default 0
3	VariableFreq	0: Forces fixed frequency operation of the buck regulator; 1: Allows variable frequency
4	LowPower	LowPower = 1 removes power from the battery discharge monitor circuits to reduce power consumption. Default 0
5	SelVFBit	0: Listens to VFSW pin; 1: Listens to VariableFreqBit
6	AC_OK	Read only. The chip indicates the state. Default 0.
7	Trickle	Read only. The chip indicates the state. Default 0.
8 to 15		Not used.

Control Register

Each bit in the control register has a different function. Table 8 describes the actions of each bit. The register can be read or written. Bits 6 and 7 are controlled internally and are read only. Writing to bits 7 and 6 does not change their value or the function of ISL9519C.

The register returns to its default values on power-up of VSMB (see Table 2 on page 16).

Charger Timeout

The ISL9519C includes a timer to insure the SMBus master is active and to prevent over charging the battery. If the adapter is present and if ISL9519C does not receive a write to the MaxSystemVoltage or ChargeCurrent register within 175s, ISL9519C will terminate charging by turning the BGATE FET OFF. If a time-out occurs, either the MaxSystemVoltage or the ChargeCurrent register must be written to in order to re-enable charging. ISL9519C will continue to regulate the system voltage even if an SMBus time-out occurs. If the adapter is not present, ISL9519C turns the BGATE FET ON to supply system voltage from the battery.

ISL9519C Data Byte Order

Each register in ISL9519C contains 16-bits or two, 8-bit bytes. All data sent on the SMBus is in 8-bit bytes and 2 bytes must be written or read from each register in ISL9519C. The order in which these bytes are transmitted appears reversed from the way they are normally written. The LO BYTE is sent first and the HI BYTE is sent second. For example, when writing 0x41A0, 0xA0 is written first, and 0x41 is sent second. (See Figure 21.)

Writing to the Internal Registers

In order to set the ChargeCurrent, InputCurrent, MaxSystemVoltage, MinSystemVoltage or the Control registers, valid 16-bit numbers must be written to ISL9519C's internal registers via the SMBus.

To write to a register in the ISL9519C, the master sends a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. If it receives an Acknowledge from the ISL9519C it sends a register address byte setting the register to be written (i.e., 0x14 for the ChargeCurrent register). The ISL9519C will respond with an Acknowledge. The master then sends the lower data byte to be written into the desired register. The ISL9519C will respond with an Acknowledge. The master then sends the higher data byte to be written into the desired register. The ISL9519C will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL9519C that the current transaction is complete. Once this transaction completes, the ISL9519C will begin operating at the new current or voltage (see Figure 21).

The ISL9519C does not support writing more than one register per transaction.

Reading from the Internal Registers

The ISL9519C has the ability to read from 7 internal registers. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the registers address byte. This process begins by the master sending a control byte with the R/$\overline{W}$ bit set to 0, indicating a write. Once it receives an acknowledge from the ISL9519C, it sends a register address byte representing the internal register it wants to read. The ISL9519C will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition the master follows with a new Start condition, then sends a new control byte with the ISL9519C slave address and the R/$\overline{W}$ bit set to 1, indicating a read. The ISL9519C will Acknowledge then send the lower byte stored in that register. After receiving the byte, the master Acknowledges by holding SDA low during the 9th clock pulse. The ISL9519C then sends the higher byte stored in the register. After the second byte neither device holds SDA low (No Acknowledge). The master will then produce a Stop condition to end the read transaction (see Figure 21).

The ISL9519C does not support reading more than 1 register per transaction.

Application Information

The following battery charger design refers to the "Typical Application Circuit" on page 6 in Figure 4. This section describes how to select the external components including the inductor, input and output capacitors, switching MOSFETs and current sensing resistors.

Inductor Selection

The inductor selection has trade-offs between cost, size, crossover frequency and efficiency. For example, the lower the inductance, the smaller the size, but ripple current is higher. This also results in higher AC losses in the magnetic core and the windings, which decreases the system efficiency. Higher inductance results in lower ripple current and smaller output filter capacitors, but it has higher DCR (DC resistance of the inductor) loss, lower saturation current and has slower transient response. So, the practical inductor design is based on the inductor ripple current being ±15% to ±20% of the maximum operating DC current at maximum input voltage. Maximum ripple is at 50% duty cycle or $V_{BAT} = V_{IN,MAX}/2$. The required inductance for ±15% ripple current can be calculated from Equation 3:

$$L = \frac{V_{IN,\,MAX}}{4 \cdot F_{SW} \cdot 0.3 \cdot I_{OUT,\,MAX}} \quad \text{(EQ. 3)}$$

Where $V_{IN,MAX}$ is the maximum input voltage, F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the max DC current required by the system.

For $V_{IN,MAX}$ = 20V, V_{BAT} = 12.6V, $I_{BAT,MAX}$ = 4.5A, and f_s = 400kHz, the calculated inductance is 9.3µH. Choosing the closest standard value gives L = 10µH. Ferrite cores are often the best choice since they are optimized at 400kHz to 600kHz operation with low core loss. The core must be large enough not to saturate at the peak inductor current I_{Peak} in Equation 4:

$$I_{PEAK} = I_{OUT,MAX} + \frac{1}{2} \cdot I_{RIPPLE} \quad \text{(EQ. 4)}$$

Inductor saturation can lead to cascade failures due to very high currents. Conservative design limits the peak current in the inductor to less than 90% of the rated saturation current.

Crossover frequency is heavily dependent on the inductor value. F_{CO} should be less than 20% of the switching frequency and a conservative design has F_{CO} less than 10% of the switching frequency. The highest F_{CO} is in voltage control mode with the battery removed and may be calculated (approximately) from Equation 5:

$$F_{CO} = \frac{5 \cdot 11 \cdot R_{SENSE}}{2\pi \cdot L} \quad \text{(EQ. 5)}$$

Output Capacitor Selection

In Narrow VDC systems, one or more capacitors are connected at the charger output (CSON) and a large number of capacitors are connected to the system voltage output. Most of the system voltage capacitors are placed near the inputs to the system and core regulators. Some capacitance (on the order of 20µF to 100µF) with low ESR should be placed near the inductor and FETs to provide a path for switching currents that is short and has a small area.

A combination of 0.1µF, 10µF ceramic capacitors and organic polymer capacitors are a good choice for capacitors near the ISL9519C and the inputs to the other system regulators. Organic polymer capacitors have high capacitance with small size and have a significant equivalent series resistance (ESR). Although ESR adds to ripple voltage, it also creates a high frequency zero that helps the closed loop operation of the buck regulator.

Snubber Design

ISL9519C's buck regulator operates in discontinuous current mode (DCM) when the load current is less than half the peak-to-peak current in the inductor. After the low-side FET turns off, the phase voltage rings due to the high impedance with both FETs off. This can be seen in Figure 24. Adding a snubber (resistor in series with a capacitor) from the phase node to ground can greatly reduce the ringing. In some situations a snubber can improve output ripple and regulation.

The snubber capacitor should be approximately twice the parasitic capacitance on the phase node. This can be estimated by operating at very low load current (100mA) and measuring the ringing frequency. Other capacitor values can be used but smaller values will allow some ringing and larger values will increase the power dissipated in the snubber resistor.

C_{SNUB} and R_{SNUB} can be calculated from Equations 6 and 7:

$$C_{SNUB} = \frac{2}{(2\pi F_{ring})^2 \cdot L} \quad \text{(EQ. 6)}$$

$$R_{SNUB} = \sqrt{\frac{2 \cdot L}{C_{SNUB}}} \quad \text{(EQ. 7)}$$

Input Capacitor Selection

The input capacitor absorbs the ripple current from the synchronous buck converter, which is given by using Equation 8:

$$I_{RMS} = I_{BAT} \cdot \frac{\sqrt{V_{OUT} \cdot (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(EQ. 8)}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet. Non-tantalum chemistries (ceramic, aluminum, or OSCON) are preferred due to their resistance to power-up surge currents when the AC-adapter is plugged into the battery charger. For Notebook battery charger applications, it is recommended that ceramic capacitors or polymer capacitors from Sanyo be used due to their small size and reasonable cost.

Loop Compensation Design

ISL9519C has four closed loop control modes. One controls the output voltage when the battery is fully charged or absent. A second controls the current into the battery when charging, the third limits current drawn from the adapter and the fourth controls the minimum system voltage. The charge current and input current control loops are compensated by a single capacitor on the ICOMP pin. The voltage control loops are compensated by a network shown in Figure 24. Descriptions of these control loops and guidelines for selecting compensation components will be given in the following sections. Which loop controls the switching regulator is determined by the minimum current buffer and the minimum voltage buffer (IMIN and VMIN in Figure 3). These four loops will be described separately.

Transconductance Amplifiers gm1, gm2, gm3 and gm4

The ISL9519C uses several transconductance amplifiers (also known as gm amps). Most commercially available op amps are voltage controlled voltage sources with gain expressed as $A = V_{OUT}/V_{IN}$. gm amps are voltage controlled current sources with gain expressed as $gm = I_{OUT}/V_{IN}$. gm will appear in some of the equations for poles and zeros in the compensation.

PWM Gain F_m

The Pulse Width Modulator in the ISL9519C converts voltage at VCOMP (or ICOMP) to a duty cycle by comparing VCOMP to a triangle wave
(duty = $VCOMP/V_{P\text{-}P\ RAMP}$). The low-pass filter formed by L and C_O convert the duty cycle to a DC output voltage
($V_{OUT} = V_{DCIN}$*duty). In ISL9519C, the triangle wave amplitude is proportional to V_{DCIN}. Making the ramp amplitude proportional to DCIN makes the gain from VCOMP to the PHASE output a constant 11 and is independent of DCIN.

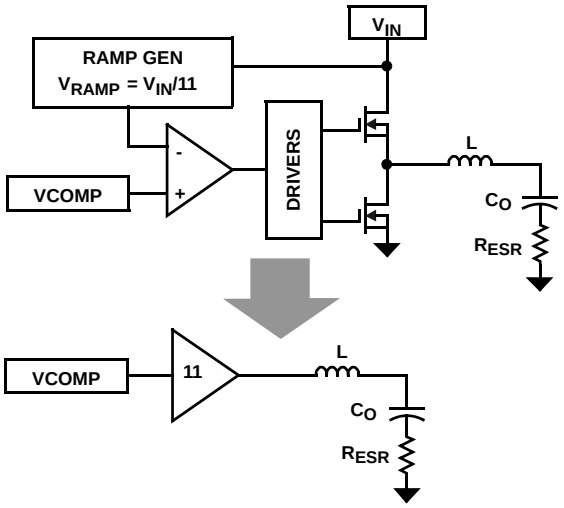


FIGURE 22. FOR SMALL SIGNAL AC ANALYSIS, THE PWM AND POWER STAGE CAN BE MODELED AS A SIMPLE GAIN OF 11

Output LC Filter Transfer Functions

The gain from the phase node to the system output and battery depend entirely on external components. Transfer function $A_{LC}(s)$ is shown in Equations 9 and 10:

$$A_{LC} = \frac{\left(1 - \frac{s}{\omega_{ESR}}\right)}{\left(\frac{s^2}{\omega_{DP}} + \frac{s}{(\omega_{DP} \cdot Q)} + 1\right)} \quad \text{(EQ. 9)}$$

$$\omega_{DP} = \frac{1}{(\sqrt{L \cdot C_o})}$$
$$\omega_{ESR} = \frac{1}{(R_{ESR} \cdot C_o)} \quad \text{(EQ. 10)}$$
$$Q = R_o \cdot \sqrt{\frac{L}{C_o}}$$

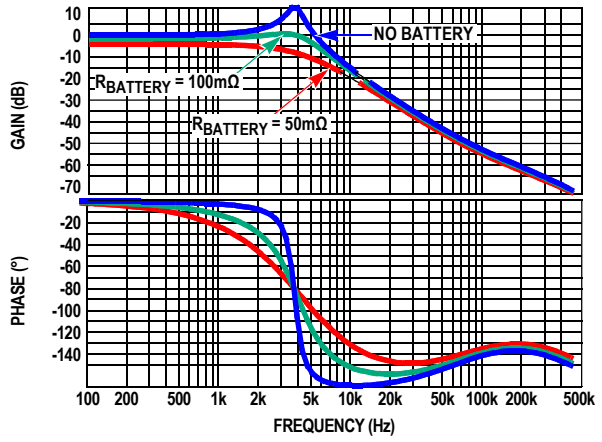


FIGURE 23. FREQUENCY RESPONSE OF THE LC OUTPUT FILTER

The load resistance R_0 is a combination of MOSFET $r_{DS(ON)}$, inductor DCR and the internal resistance of the battery (normally between 50mΩ and 200mΩ) in parallel with the system. The system load may be modeled as a current sink in parallel with a resistance. For AC analysis of the voltage control loop, this may be treated as a very high resistance or an open circuit. The worst case for voltage mode control is when the battery is absent. This results in the highest Q of the LC filter and the lowest phase margin.

When the battery is present, the Q is very low (typically 0.1). With very low Q the double pole from the LC filter split into two separate poles, one at frequency below ω_{DP} and one at a frequency above ω_{DP}.

Max System Voltage Control Loop

The max system voltage error amplifier controls the output when the input current is below the limit and the battery is charged to the value in the MaxSystemVoltage register. Under these conditions, VCOMP controls the charger's output because the 2 current error amplifiers (gm1 and gm3) output their maximum current and charge the capacitor on ICOMP to its maximum voltage (clamped to 0.3V above VCOMP). With ICOMP higher than VCOMP, the minimum voltage buffer output equals the voltage on VCOMP. The max system voltage control loop is shown in Figure 24.

The compensation network consists of the max system voltage error amplifier gm2 and the compensation network R_1, C_1, R_2 and C_2. Equations 11 through 16 relate to the compensation network's poles, zeros and gain to the components in Figure 24. Figure 25 shows an asymptotic Bode plot of the DC/DC converter's gain vs frequency. It is strongly recommended that F_{Z1} is approximately $1/4*F_{DP}$, and F_{Z2} is approximately $1/2*F_{DP}$.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{(2\pi \cdot C_1 \cdot (R_1 + R_3))} \quad \text{(EQ. 11)}$$

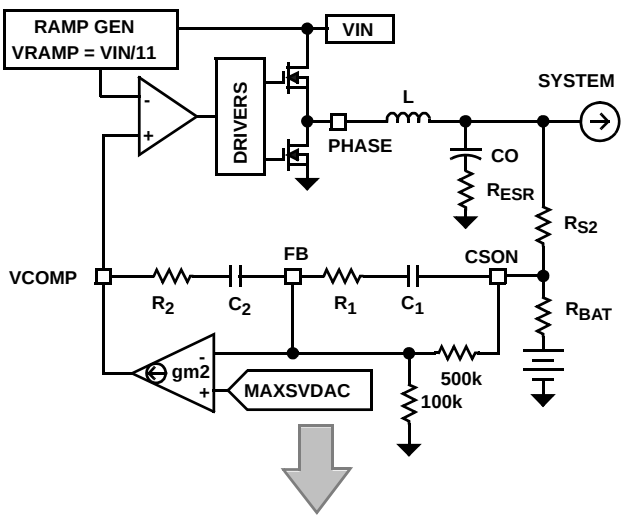
$$F_{Z2} = \frac{1}{\left(2\pi \cdot C_2 \cdot \left\{R_2 - \frac{1}{gm2}\right\}\right)} \quad \text{(EQ. 12)}$$

$$\frac{1}{gm2} = 4000\Omega \quad \text{(EQ. 13)}$$

$$F_{DP} = \frac{1}{(2\pi\sqrt{L \cdot C_o})} \quad \text{(EQ. 14)}$$

$$F_{P1} = \frac{1}{(2\pi \cdot R_1 \cdot C_1)} \quad \text{(EQ. 15)}$$

$$F_{ESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 16)}$$



FOR SMALL SIGNAL AC ANALYSIS, VOLTAGE SOURCES ARE SHORT CIRCUITS AND CURRENT SOURCES ARE OPEN CIRCUITS.

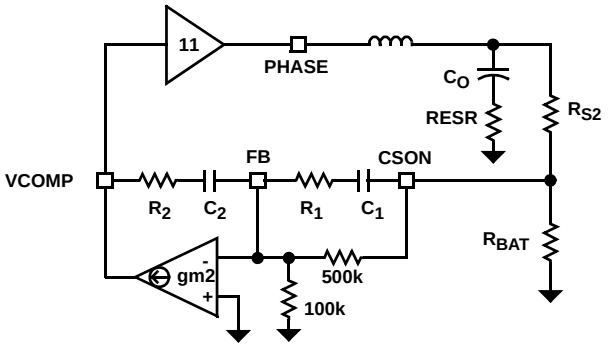


FIGURE 24. MAX SYSTEM VOLTAGE LOOP COMPENSATOR

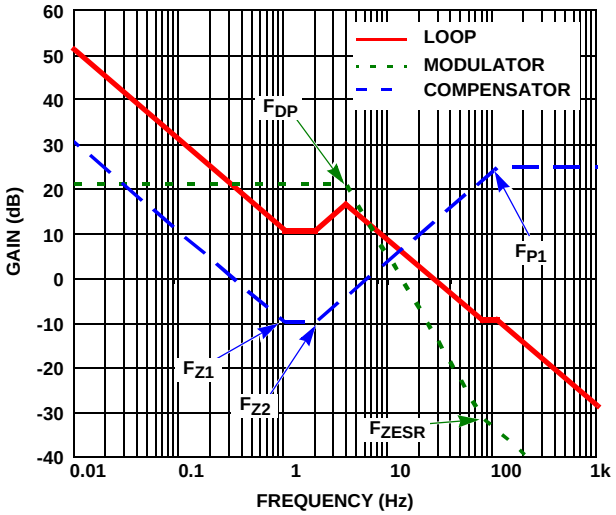


FIGURE 25. ASYMPTOTIC BODE PLOT OF THE MAX SYSTEM VOLTAGE CONTROL LOOP GAIN

Charge Current Control Loop

When the battery voltage is less than the programmed max system voltage, the max system voltage error amplifier goes to it's maximum output (limited to 0.3V above ICOMP) and the ICOMP voltage controls the loop through the minimum voltage buffer. Figure 26 shows the charge current control loop.

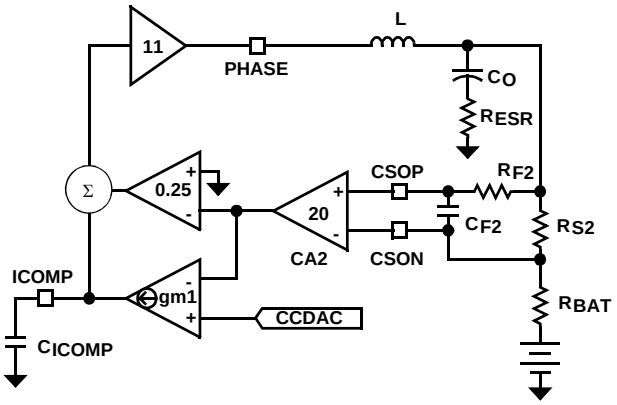


FIGURE 26. CHARGE CURRENT LIMIT LOOP

The compensation capacitor (C_{ICOMP}) gives the error amplifier (gm1) a pole at a very low frequency (<<1Hz) and a zero at F_{Z1}. F_{Z1} is created by the 0.25*CA2 output added to ICOMP. The loop response has another zero due to the output capacitor's ESR.

A filter should be added between R_{S2} and CSOP and CSON to reduce switching noise. The filter roll off frequency should be between the crossover frequency and the switching frequency (~100kHz). R_{F2} should be small (<2Ω) to minimize offsets due to leakage current into CSOP.

$$F_{DP} = \frac{1}{(2\pi\sqrt{L \cdot C_o})} \quad \text{(EQ. 17)}$$

$$F_{ZESR} = \frac{1}{(2\pi \cdot C_o \cdot R_{ESR})} \quad \text{(EQ. 18)}$$

$$F_{Z1} = \frac{4 \cdot gm1}{(2\pi \cdot C_{ICOMP})} \quad \text{(EQ. 19)}$$

$$gm1 = 50\mu A/V \quad \text{(EQ. 20)}$$

$$F_{FILTER} = \frac{1}{(2\pi \cdot C_{F2} \cdot R_{F2})} \quad \text{(EQ. 21)}$$

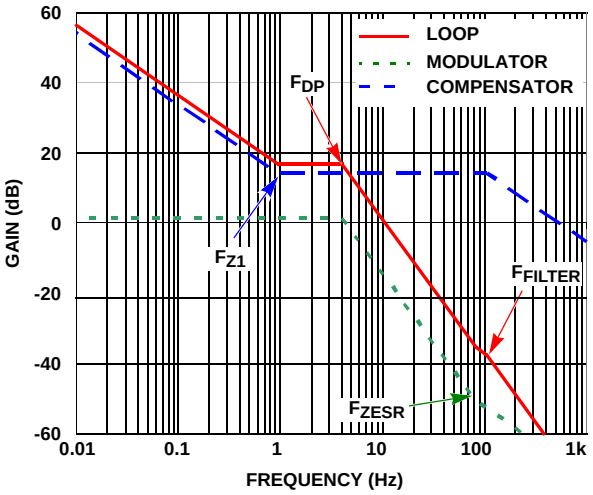


FIGURE 27. CHARGE CURRENT LOOP BODE PLOTS

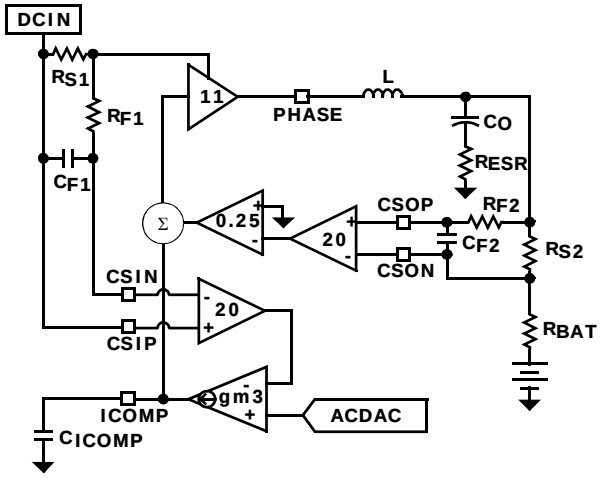


FIGURE 28. ADAPTER CURRENT LIMIT LOOP

C_{ICOMP} should be chosen using Equation 22 to set $F_{Z1} = F_{DP}/10$. The crossover frequency will be approximately $2.5*F_{DP}$. The phase margin will be between +10° and +40° depending on F_{ZESR}.

$$C_{ICOMP} = \frac{4 \cdot gm1}{2\pi \cdot F_{DP}/10} \quad \text{(EQ. 22)}$$

Adapter Current Limit Control Loop

If the combined battery charge current and system load current results in adapter current that equals the programmed adapter current limit, ISL9519C will reduce the current to the battery and/or reduce the output voltage to hold the adapter current at the limit. Above the adapter current limit, the minimum current buffer equals the output of gm3 and ICOMP controls the charger output.

A filter should be added between R_{S1} and CSIP and CSIN to reduce switching noise. The filter roll off frequency should be between the crossover frequency and the switching frequency (~100kHz).

The loop response equations, bode plots and the selection of C_{ICOMP} are the same as the charge current control loop with loop gain reduced by the duty cycle. In other words, if the duty cycle D = 50%, the loop gain will be 6dB lower than the loop gain in Figure 27. This gives lower crossover frequency and higher phase margin in this mode.

The current control loops can have the same gain if the Input current sense resistor is larger than the charge current sense resistor by the same ratio that input voltage is larger than output voltage.

Min System Voltage Control Loop

The min system voltage control loop is only active when a battery is connected that is discharged to a voltage below the voltage in the MinSystemVoltage register. When it is active, the ISL9519C reduces the charge current to 256mA and controls the BGATE FET in the linear range to hold the min system voltage on the system output. The reduced charge current and active BGATE control are referred to in this document as “Trickle Charge Mode”.

When the battery voltage is higher than min system voltage, BGATE goes approximately 7V below the system voltage (at CSON) to fully enhance the BGATE FET. In 1-cell systems BGATE will pull to ground. A BGATE FET should be selected that is fully enhanced with MinSystemVoltage between gate and source.

When the battery voltage is less than the min system voltage, the min system voltage loop controls the voltage on BGATE to hold the system voltage at the programmed min system voltage. The voltage difference between the min system voltage and the battery voltage drops across the BGATE FET.

Guidelines for Layout and Component Placement

Signal Ground (AGND) and Power Ground (PGND) Connection

The ISL9519C has 2 ground connections; AGND and PGND. AGND should connect to all low power and sensitive circuits, such as compensation and current sensing. PGND should be connected to all high power circuits, such as the switching FETs and bypass caps. AGND should be connected to PGND at a single point at the ISL9519C. PGND should connect to the main system ground plane at a single point very near the ISL9519C.

PGND is connected internally to the source of the lower FET and the FET driver circuits. It should be connected externally to the bypass capacitors on the output power (Vsystem caps and Vbattery caps) and input power (VDDP cap and the caps at VIN. The PGND pin should be connected to the main system ground plane at one point very close to the ISL9519C.

AGND is internally connected to the IC substrate and all of the small signal circuits in the IC. All connections to ground from the following list of pins should connect to an area of copper that is separate from the main ground plane and PGND (DCIN, ADET, ICOMP, VCOMP, CELL, AMON, VSMB, VDD, CSIN, CSIP). Please refer to Figure 4 for details of the connections to AGND and PGND. This separate area of ground should be connected to both the AGND and PGND pins at (under) the ISL9519C.

The thermal pads on the IC have the lowest thermal resistance path to the conduct heat away from the IC and FETs. Pad 51 (AGND) should be connected to other AGND pins. Pad 52 (PHASE) is the Thermal pad for the lower FET. Pad 53 is the thermal Pad for the upper FET. Pads 52 and 51 should be connected with several vias to areas of copper to minimize the thermal resistance from the IC to the ambient air. See Figure 29 for an example of the pattern of vias in the thermal pad.

VIN (Input Power) Capacitors

It is recommended that ceramic capacitors be used closely connected to VIN and PGND. This capacitor reduces the noise and the power loss of the MOSFET. The capacitors should be on the same layer as ISL9519C to avoid vias between ISL9519C and bypass caps.

VDDP

At least one high quality ceramic decoupling cap should be connected from VDDP to PGND. The decoupling cap should be put close to the IC. VDDP is the power input to the gate drivers. The decoupling cap should be placed close to ISL9519C on the same layer.

UGATE

This pin connects the upper FET gate to the driver. A 4700pF cap should be connected to reduce dV/dt.

PHASE

This trace should be short, and positioned away from other weak signal traces. This node has a very high di/dt and dv/dt with a voltage swing from the input voltage to ground. It is the return path for upper FET gate drive currents.

Copper Size for the Phase Node

The capacitance of PHASE should be kept very low to minimize ringing. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

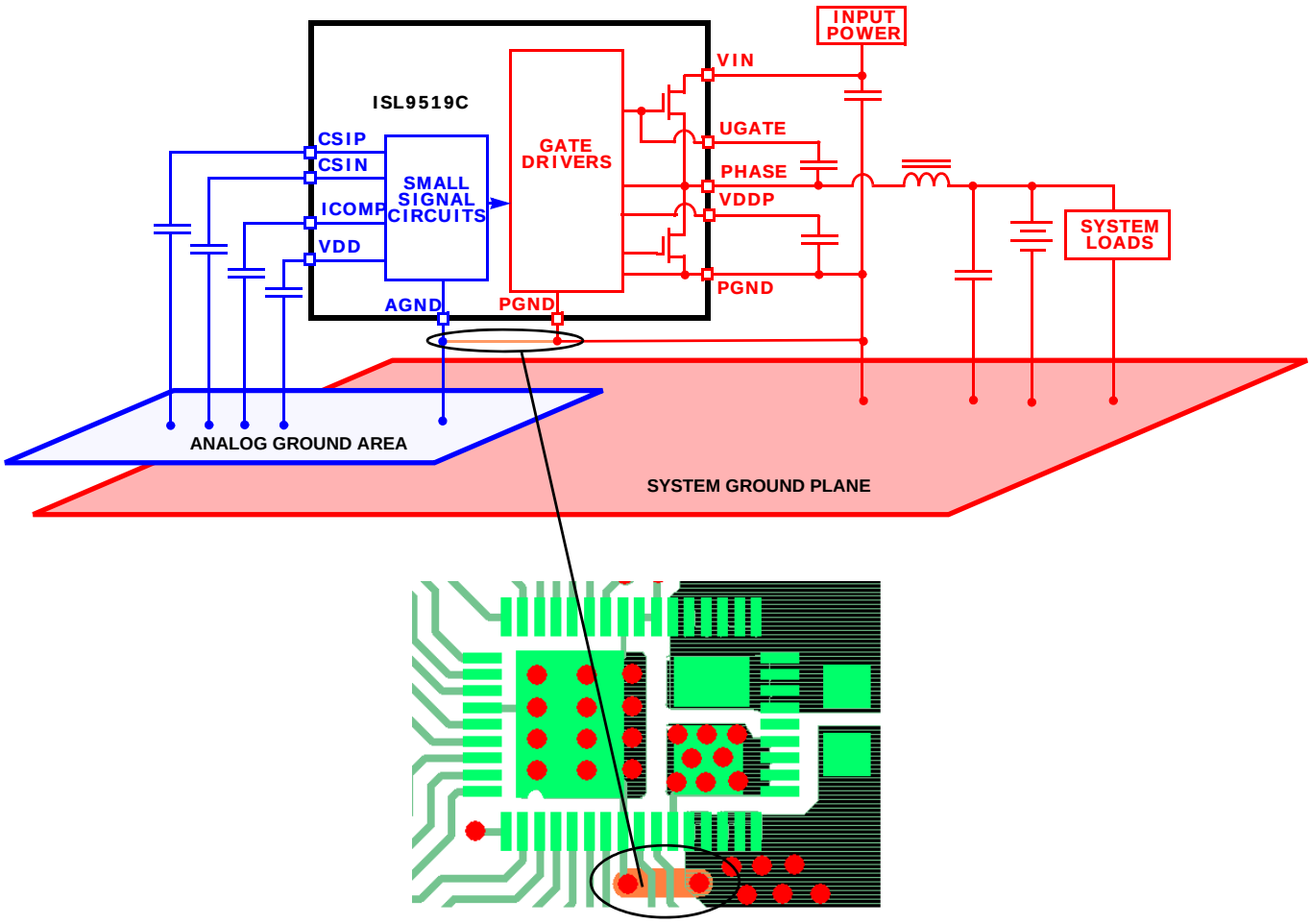


FIGURE 29. AGND AND PGND

BOOT

This pin's di/dt is as high as the UGATE; therefore, this trace should be as short as possible.

VDD

At least one high quality ceramic decoupling cap should be connected from VDD to AGND. The decoupling cap should be placed close to the IC. VDD is the output of an internal regulator and the supply for most of the small signal circuits in the IC. The VDD decoupling cap should be placed close to the ISL9519C and on the same layer. The ground end of the VDD decoupling cap should connect through a via to the separate AGND area on the layer adjacent to the ISL9519C.

CSOP, CSON, CSIP and CSIN

Accurate charge current and adapter current sensing is critical for good performance. The current sense resistor connects to the CSON and the CSOP pins through a low pass filter with the filter capacitor very near the IC (see Figure 4). Traces from the sense resistor should start at the pads of the sense resistor and should be routed close together through the low pass filter and to the CSOP and CSON pins (see Figure 30). The CSON pin is also used as the system voltage feedback. The traces should be routed away from the high dv/dt and di/dt pins like PHASE, BOOT pins. In general, the current sense resistor should be close to the IC. These guidelines should also be followed for the adapter current sense resistor and CSIP and CSIN. Other layout arrangements should be adjusted accordingly.

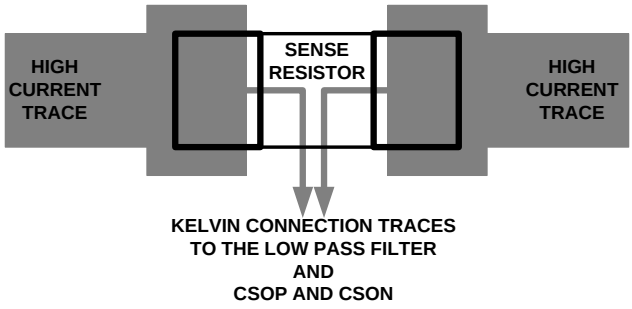


FIGURE 30. CURRENT SENSE RESISTOR LAYOUT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 30, 2011	FN7823.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL9519C

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

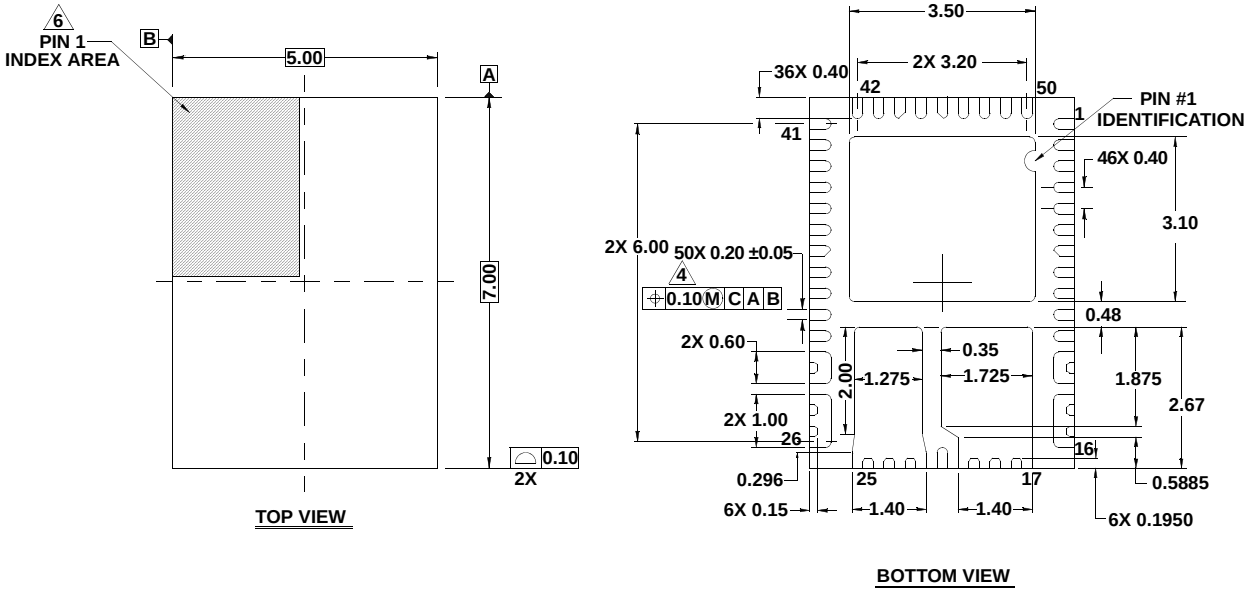
FITs are available from our website at: http://rel.intersil.com/reports/search.php

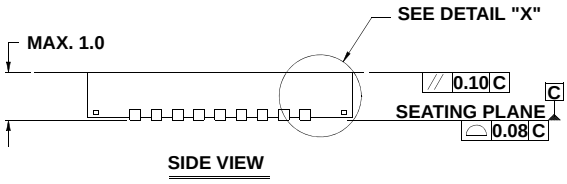
Package Outline Drawing

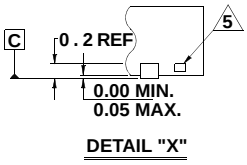
L50.5x7B

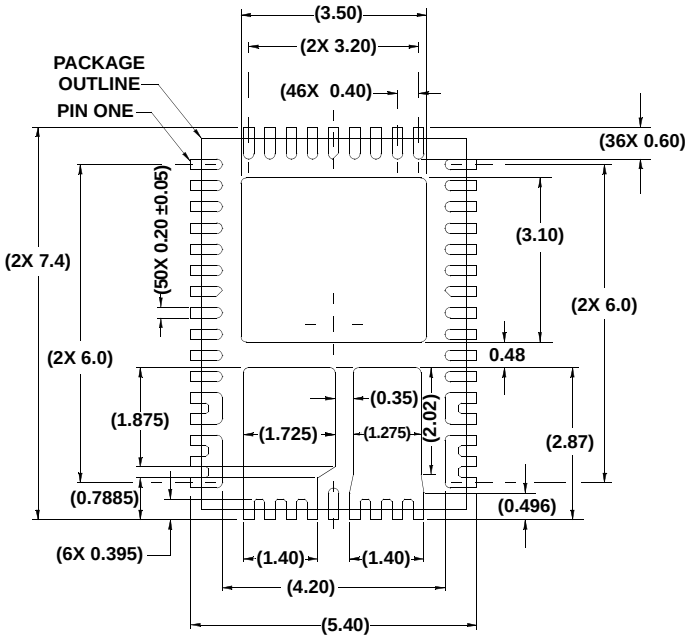
50 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 12/10









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.10
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.