NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT:
ISL95810

ISL95811

I²C Bus, 256 Taps, 5 Bytes General Purpose Memory, Low Noise, Low Power

FN6759
Rev 1.00
October 6, 2008

Single Digitally Controlled Potentiometer (XDCP™)

The ISL95811 integrates a digitally controlled potentiometer (XDCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR), that can be directly written to and read by the user. The content of the WR controls the position of the wiper. At power-up the device recalls the contents of the DCP's IVR to the WR.

The DCP can be used as three-terminal potentiometer or as two-terminal variable resistor in a wide variety of applications including control, parameter adjustments and signal processing.

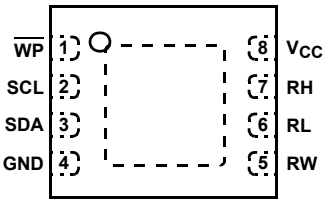
Features

- 256 Resistor Taps - 0.4% Resolution
- I²C Serial Interface
- 5 General Purpose Non-Volatile Bytes
- Non-volatile Storage of Wiper Position
- Write Protection
- Wiper Resistance: 70Ω Typical @ V_{CC} = 3.3V
- Standby Current 10µA Max
- Power Supply: 2.7V to 5.5V
- 50kΩ, 10kΩ Total Resistance
- High Reliability
  - Endurance: 1,000,000 Data Changes per Bit per Register
  - Register Data Retention: 50 Years @ T ≤ +55°C
- 8 Ld MSOP and 8 Ld TDFN Packaging
- Pb-Free (RoHS compliant)

Pinouts

ISL95811
(8 LD MSOP)
TOP VIEW

ISL95811
(8 LD TDFN)
TOP VIEW



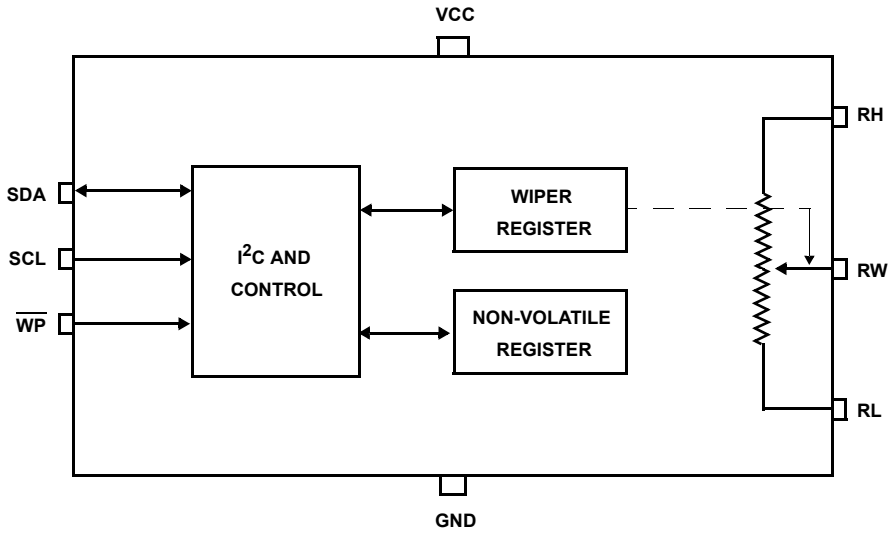
Ordering Information

PART NUMBER (Note)	PART MARKING	R_{TOTAL} (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95811WFUZ	5811W	10	-40 to +125	8 Ld MSOP	MDP0043
ISL95811WFUZ-T*	5811W	10	-40 to +125	8 Ld MSOP	MDP0043
ISL95811WFUZ-TK*	5811W	10	-40 to +125	8 Ld MSOP	MDP0043
ISL95811WFRTZ	811W	10	-40 to +125	8 Ld 3x3 TDFN	L8.3x3A
ISL95811WFRTZ-TK*	811W	10	-40 to +125	8 Ld 3x3 TDFN	L8.3x3A
ISL95811UFUZ	5811U	50	-40 to +125	8 Ld MSOP	MDP0043
ISL95811UFUZ-T*	5811U	50	-40 to +125	8 Ld MSOP	MDP0043
ISL95811UFUZ-TK*	5811U	50	-40 to +125	8 Ld MSOP	MDP0043
ISL95811UFRTZ	811U	50	-40 to +125	8 Ld 3x3 TDFN	L8.3x3A
ISL95811UFRTZ-TK*	811U	50	-40 to +125	8 Ld 3x3 TDFN	L8.3x3A

*Please refer to TB347 for details on reel specifications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

MSOP PIN NUMBER	TDFN PIN NUMBER	SYMBOL	DESCRIPTION
1	1	$\overline{WP}$	Hardware write protection. Active low. Prevents any “Write” operation of the I^2C interface.
2	2	SCL	I^2C interface input clock
3	3	SDA	Open Drain Serial Data I/O for the I^2C interface
4	4	GND	Ground
5	5	RW	“Wiper” terminal of the DCP
6	6	RL	“Low” terminal of the DCP
7	7	RH	“High” terminal of the DCP
8	8	V_{CC}	Power supply
		EPAD*	Exposed Die Pad internally connected to GND

*NOTE: PCB thermal land for QFN/TDFN EPAD should be connected to GND plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf.

Absolute Maximum Ratings

Voltage at any Digital Interface Pin with respect to GND . . . . . -0.3V to V_{CC} + 0.3V
V_{CC} . . . . . -0.3V to +6.0V
Voltage at any DCP Pin with respect to GND . . . . . 0V to V_{CC}
I_W (10s) . . . . . ±6mA
ESD Rating
Human Body Model 3kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN (Notes 1, 2)	52	9
8 Ld MSOP (Note 1)	160	N/A

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Latchup (Note 3) . . . . . Class II, Level B @ +125°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Extended Industrial) . . . . . -40°C to +125°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating 15mW
Wiper Current . . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Jedec Class II pulse conditions and failure criterion used. Level B exceptions is using a max positive pulse of 6.5V on the $\overline{WP}$ pin.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
R_{TOTAL}	R_H to R_L Resistance	$R_{TOTAL} = (V_{RH} - V_{RL})/I_{DCP}$	W option		10		kΩ
			U option		50		kΩ
	R_H to R_L Resistance Tolerance			-20		+20	%
R_W	Wiper Resistance	V_{CC} = 3.3V @ +25°C Wiper current = V_{CC}/R_{TOTAL}			70	200	Ω
R_{Wnoise} (Note 16)	Noise Level	Wiper at the middle scale, 1kHz 1V_{RMS} input to RH pin			-110		dBV
$C_H/C_L/C_W$ (Note 16)	Potentiometer Capacitance				10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}			0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ RL; V_{CC} @ RH; measured at RW, unloaded)							
INL (Note 9)	Integral Non-Linearity	DCP register set between 1 hex and FFhex. Monotonic over all tap positions. W and U options		-1		1	LSB (Note 5)
DNL (Note 8)	Differential Non-Linearity	DCP register set between 1 hex and FF hex. Monotonic over all tap positions	W option	-0.75		0.75	LSB (Note 5)
			U option	-0.5		0.5	
ZSerror (Note 6)	Zero-Scale Error	W option		0	1	5	LSB (Note 5)
		U option		0	0.5	2	
FSerror (Note 7)	Full-Scale Error	W option		-5	-1	0	LSB (Note 5)
		U option		-2	-0.5	0	
TC_V (Note 10, 16)	Ratiometric Temperature Coefficient	DCP Register set to 80 hex			±4		ppm/°C
f_{CUTOFF} (Note 16)	3dB Cut-Off Frequency	Wiper at the middle scale	W option		1250		kHz
			U option		250		kHz

Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS		MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNIT
RESISTOR MODE (Measurements between RW and RL with RH not connected, or between RW and RH with RL not connected)							
RINL (Note 14)	Integral Non-Linearity	DCP register set between 1 hex and FF hex. Monotonic over all tap positions.	W option	-3		3	MI (Note 11)
			U option	-1		1	MI (Note 11)
RDNL (Note 13)	Differential Non-Linearity	DCP register set between 1 hex and FF hex. Monotonic over all tap positions	W option	-0.75		0.75	MI (Note 11)
			U option	-0.5		0.5	MI (Note 11)
R_{offset} (Note 12)	Offset	W option		0	1	5	MI (Note 11)
		U option		0	0.5	2	MI (Note 11)
TC_R (Note 15, 16)	Resistance Temperature Coefficient	DCP register set between 20 hex and FF hex			±45		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNITS
I_{CC1}	V_{CC} Supply Current (Volatile Write/Read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			100	µA
I_{CC2}	V_{CC} Supply Current (Non-volatile Write)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Non-volatile Write State only)			2	mA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			10	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			5	µA
I_{LkgDig}	Leakage Current, at Pins SDA, SCL, and $\overline{WP}$ Pins	Voltage at pin from GND to V_{CC}	-1		1	µA
t_{DCP}	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change			1	µs
Vpor	Power-On Recall Voltage	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V
V_{CC}Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-Up Delay	V_{CC} above V_{POR}, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
EEPROM SPECIFICATIONS						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature ≤ +55°C	50			Years
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	$\overline{WP}$, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	$\overline{WP}$, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC} + 0.3	V
Hysteresis (Note 16)	SDA and SCL Input Buffer Hysteresis		0.05*V_{CC}			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 16)	$\overline{WP}$, SDA, and SCL Pin Capacitance				10	pF

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 18)	TYP (Note 4)	MAX (Note 18)	UNITS
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STO:NV}$	STOP Condition Hold Time for Non-Volatile Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	2			µs
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 16)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 16)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 16)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 16)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ
t_{WC} (Note 17)	Non-Volatile Write Cycle Time			12	20	ms
$t_{SU:WP}$	$\overline{WP}$ Setup Time	Before START condition	600			ns
$t_{HD:WP}$	$\overline{WP}$ Hold Time	After STOP condition	600			ns

NOTES:

4. Typical values are for T_A = +25°C and 3.3V supply voltage.
5. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
6. ZS error = $V(RW)_0$/LSB.
7. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
8. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.

NOTES: (continued)

9. INL = $[V(RW)_i – (i • LSB – V(RW)_0)]/LSB$ for i = 1 to 255.

10. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.

11. $MI = |R_{255} – R_0|/255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively. $R_{offset} = R_0/MI$, when measuring between RW and RL.

12. $R_{offset} = R_{255}/MI$, when measuring between RW and RH.

13. $RDNL = (R_i – R_{i-1})/MI$, for i = 16 to 255.

14. $RINL = [R_i – (MI • i) – R_0]/MI$, for i = 16 to 255.

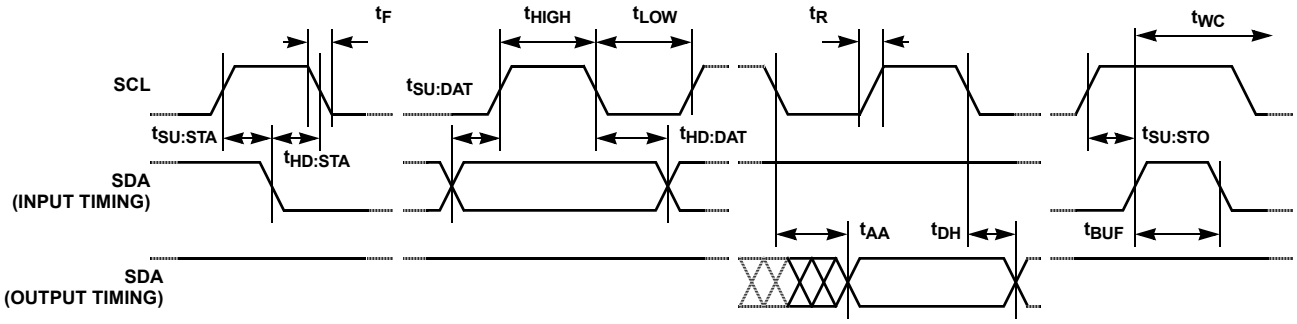
15. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 32 to 255, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.

16. Limits established by characterization and are not production tested.

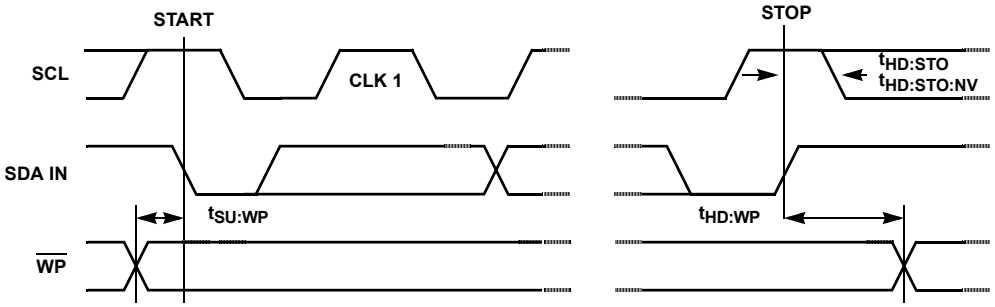
17. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of a I^2C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle. The Acknowledge Polling method can be used to determine the end of the non-volatile write cycle.

18. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



$\overline{WP}$ Pin Timing



Typical Performance Curves

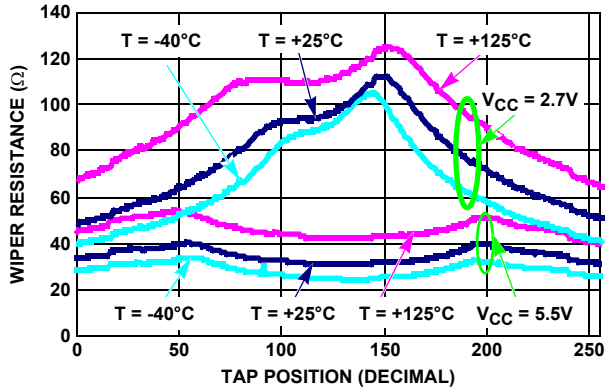


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

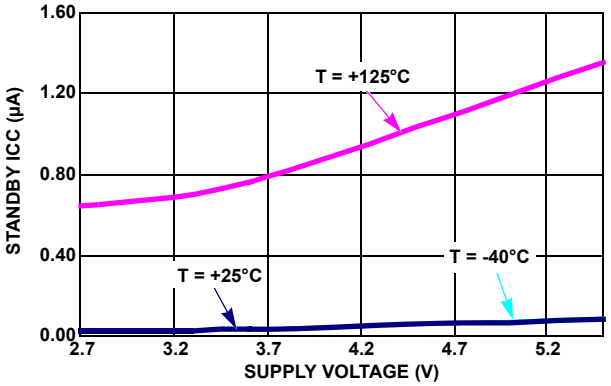


FIGURE 2. STANDBY I_{CC} vs V_{CC}

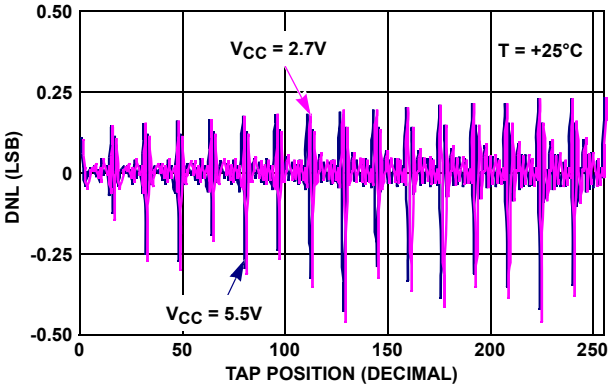


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

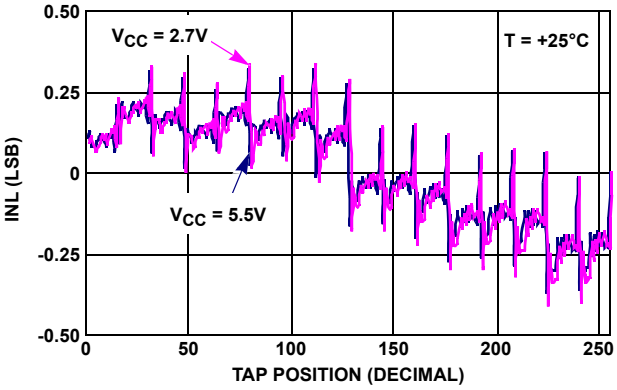


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

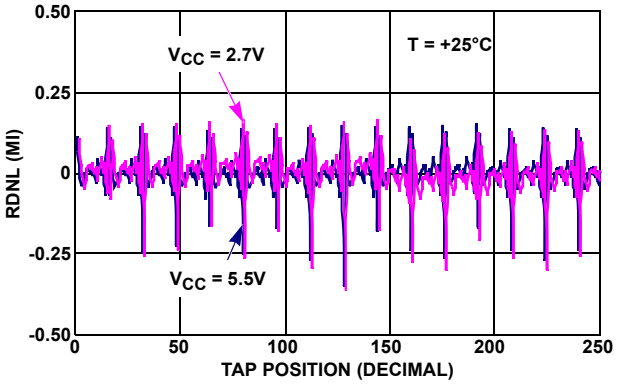


FIGURE 5. RDNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

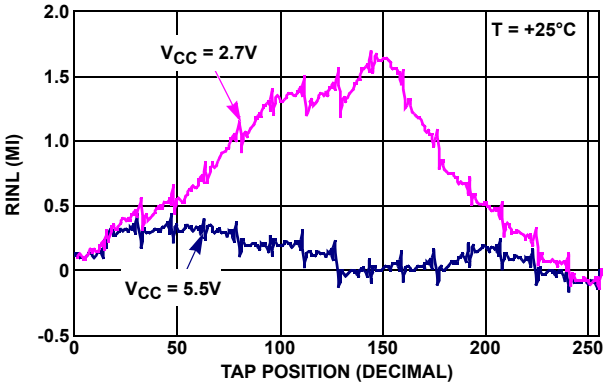


FIGURE 6. RINL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

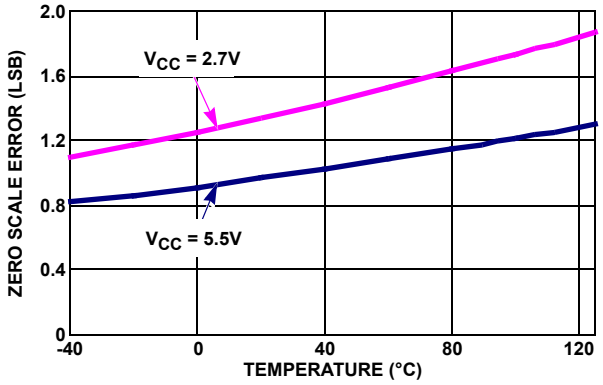


FIGURE 7. ZSerror vs TEMPERATURE

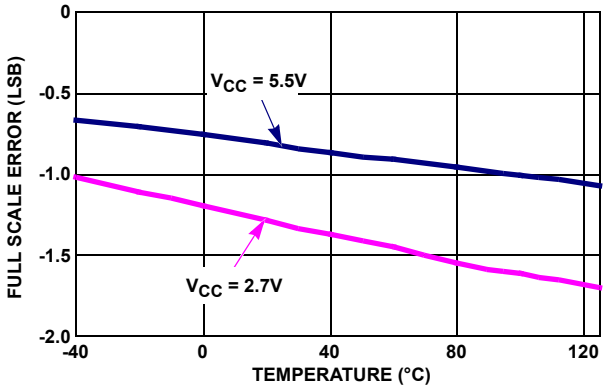


FIGURE 8. FSerror vs TEMPERATURE

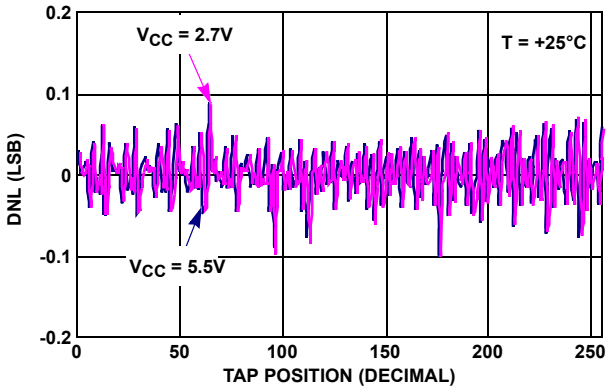


FIGURE 9. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

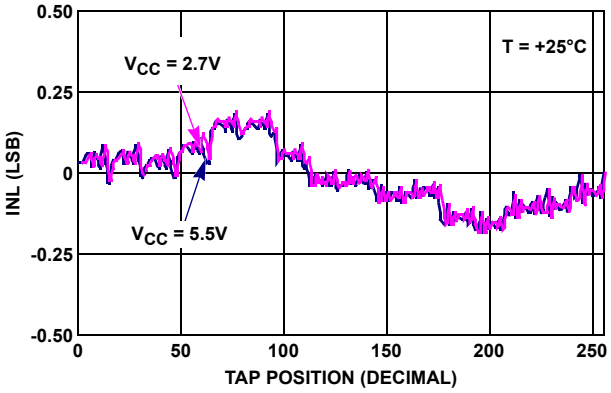


FIGURE 10. INL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

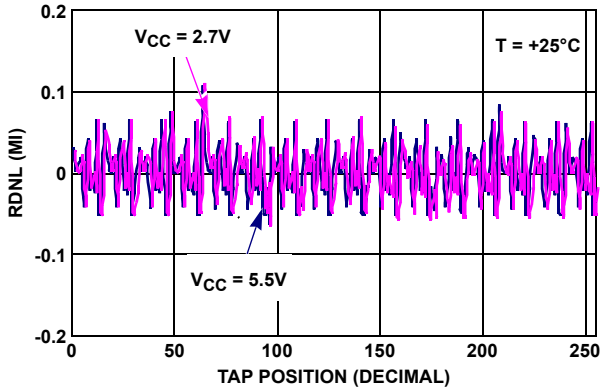


FIGURE 11. RDNL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

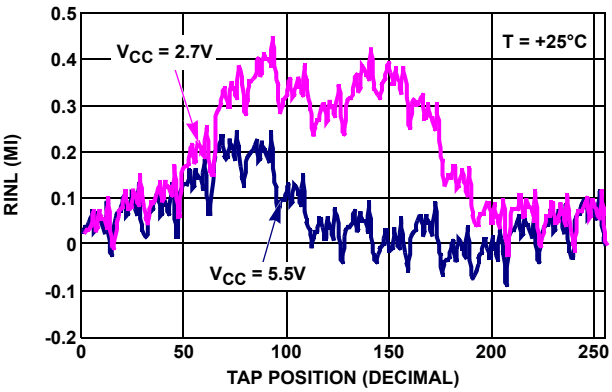


FIGURE 12. RINL vs TAP POSITION IN RHEOSTAT MODE FOR 50kΩ (U)

Typical Performance Curves (Continued)

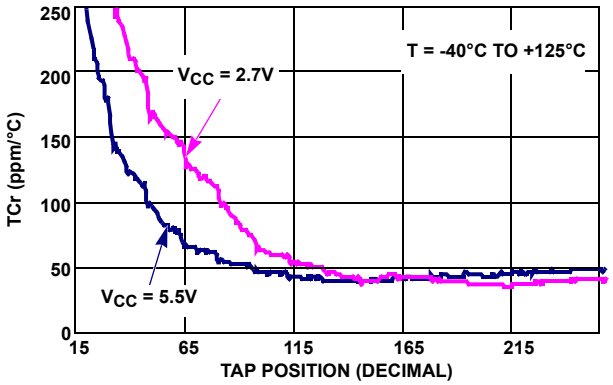


FIGURE 13. TCr FOR RHEOSTAT MODE 10k (W) IN ppm

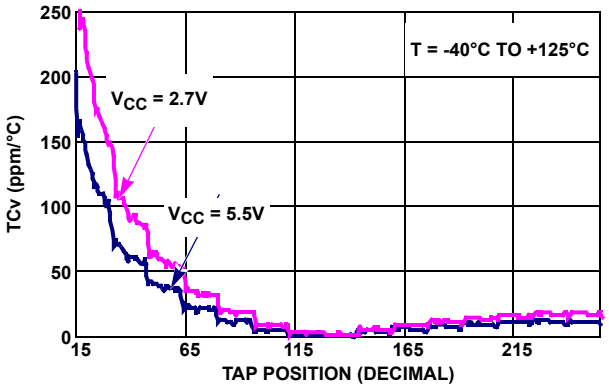


FIGURE 14. TCv FOR VOLTAGE DIVIDER MODE 10k (W) IN ppm

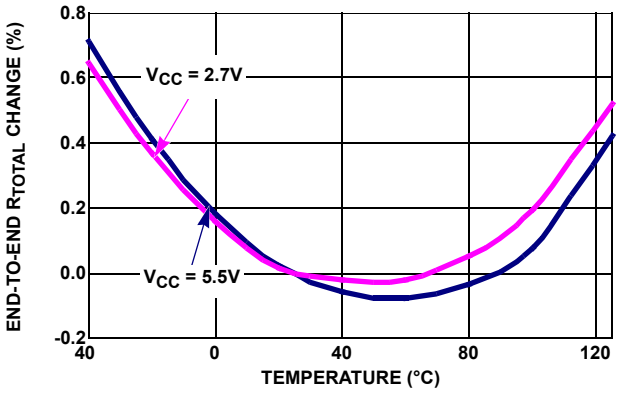


FIGURE 15. END-TO-END R_{TOTAL} % CHANGE vs TEMPERATURE, 10k (W)

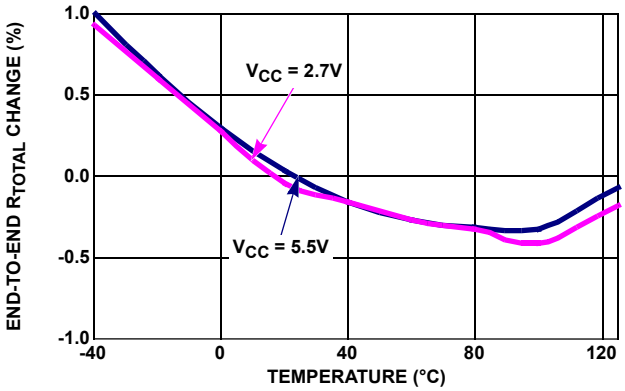


FIGURE 16. END-TO-END R_{TOTAL} % CHANGE vs TEMPERATURE, 50k (U)

Pin Description

Potentiometers Pins

RH AND RL

The high (RH) and low (RL) terminals of the ISL95811 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 255 decimal, the wiper will be closest to RH, and with the WR set to 0, the wiper is closest to RL.

RW

RW is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface. SCL requires an external pull-up resistor.

WRITE PROTECT ($\overline{WP}$)

When this pin is kept LOW, the data is written to the device will be ignored. This pin protectS the non-volatile memory from being overwritten.

Principles of Operation

The ISL95811 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At

either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR are recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR[7:0] = 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR[7:0] = FFh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the position closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL95811 is being powered up, the WR is reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reloaded with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I^2C serial interface, as described in the following sections.

Memory Description

The ISL95811 contains one non-volatile 8-bit Initial Value Register (IVR), five General Purpose non-volatile 8-bit registers and two volatile 8-bit registers: Wiper Register (WR) and Access Control Register (ACR). The Memory map of the ISL95811 is shown in Table 1. The non-volatile register (IVR) at address 0 contains the initial wiper position and the volatile register (WR) contains the current wiper position.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
8	NA	ACR
7	Reserved	
6	General Purpose	N/A
5	General Purpose	N/A
4	General Purpose	N/A
3	General Purpose	N/A
2	General Purpose	N/A
1	Device ID (read only)	N/A
0	IVR	WR

The ISL95811 is pre-programed with 80h in the IVR.

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
NAME	VOL	0	0	0	0	0	0	0

If VOL bit is 0, the non-volatile IVR register and General Purpose registers are accessible. If VOL bit is 1, only the volatile WR is accessible. Note: Value written to the IVR register is also written to the WR. The default value of this bit is 0.

The Device ID register is read only and it contains chip revision information, as shown in Table 3.

TABLE 3. DEVICE ID REGISTER

BIT #	7	6	5	4	3	2	1	0
VALUE	1	0	0	0	0	0	0	0

I^2C Serial Interface

The ISL95811 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL95811 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 17). On power-up of the ISL95811, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL95811 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 17). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 17). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the 8 bits of data (see Figure 18).

The ISL95811 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL95811 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 as the seven MSBs. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation and “0” for a Write operation (see Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

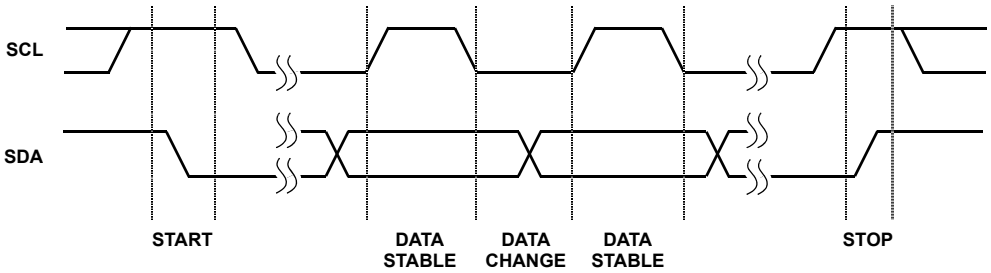


FIGURE 17. VALID DATA CHANGES, START, AND STOP CONDITIONS

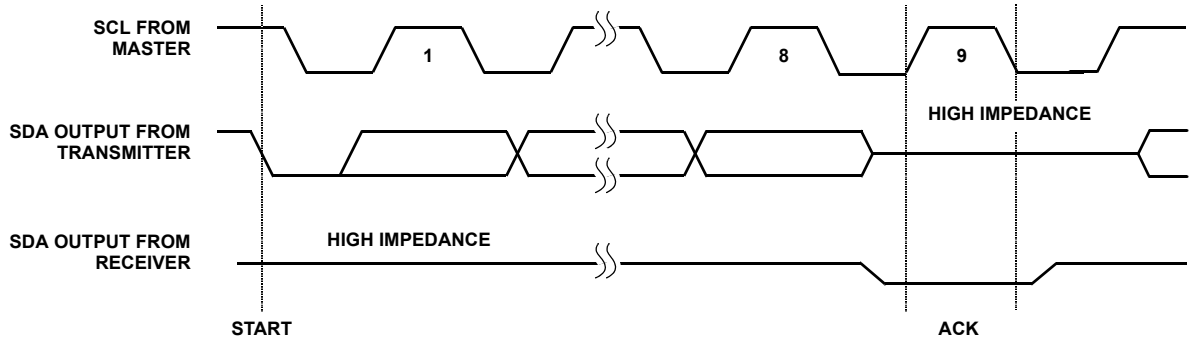


FIGURE 18. ACKNOWLEDGE RESPONSE FROM RECEIVER

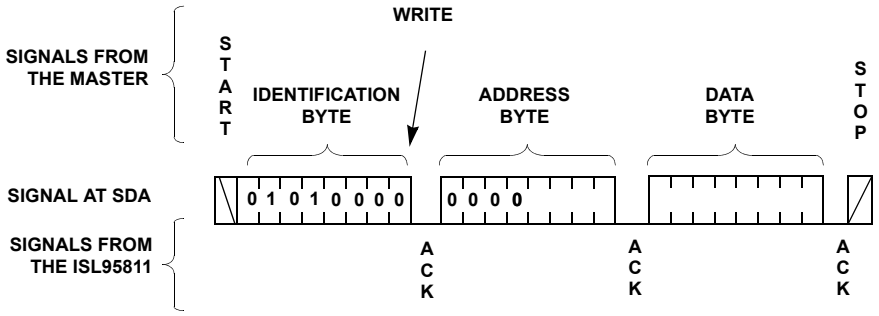


FIGURE 19. BYTE WRITE SEQUENCE

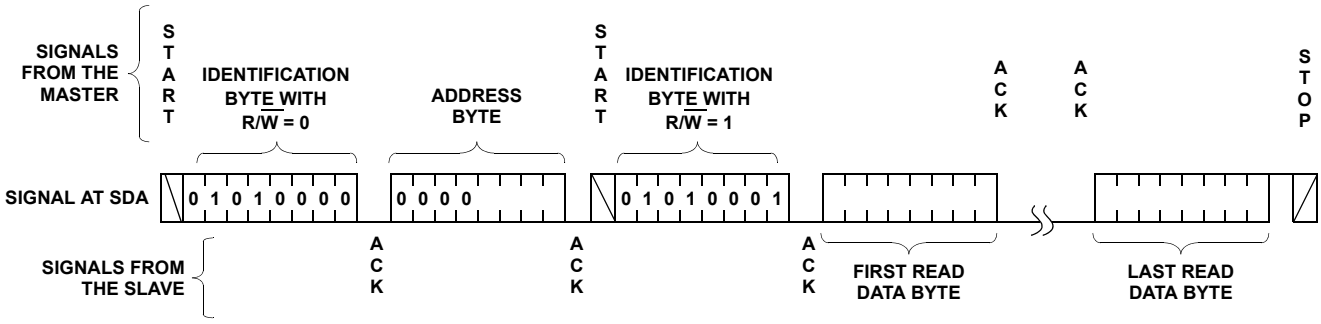


FIGURE 20. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL95811 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95811 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95811 enters its standby state (see Figure 19).

The byte at address 08h determines if the Data Byte is to be written to volatile and/or non-volatile memory (see “Memory Description” on page 10).

Data Protection

The $\overline{WP}$ pin has to be at logic HIGH to perform any Write operation to the device. When the $\overline{WP}$ is active (LOW), the device ignores Data Bytes of a Write Operation and does not respond to the Data Bytes with an ACK; rather it goes into standby state waiting for a new START condition.

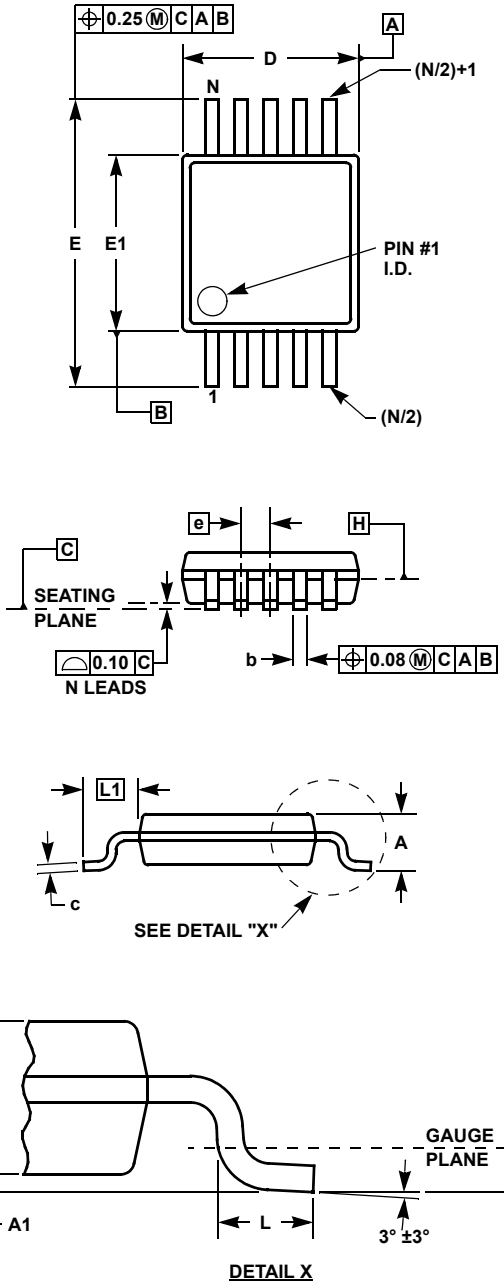
A STOP condition also acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 8, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 20). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL95811 responds with an ACK. The ISL95811 then transmits the Data Byte and the master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte.

The byte at address 08h determines if the Data Bytes being read are from volatile or non-volatile memory (see “Memory Description” on page 10).

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

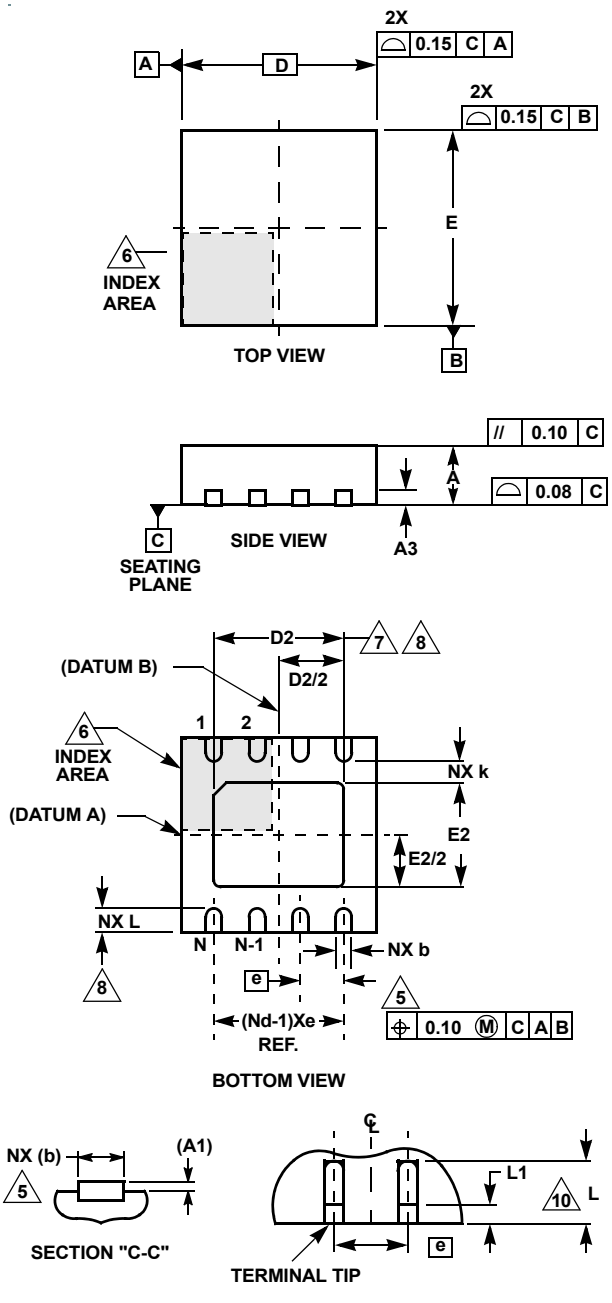
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L8.3x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A3		0.20 REF		-
b	0.25	0.30	0.35	5, 8
D		3.00 BSC		-
D2	2.20	2.30	2.40	7, 8, 9
E		3.00 BSC		-
E2	1.40	1.50	1.60	7, 8, 9
e		0.65 BSC		-
k	0.25	-	-	-
L	0.20	0.30	0.40	8
N		8		2
Nd		4		3

Rev. 3 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-WEEC-2 except for the “L” min dimension.