ISL97634

White LED Driver with Wide PWM Dimming Range

FN6264
Rev 4.00
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The ISL97634 represents an efficient and highly integrated PWM boost LED driver that is suitable for LED backlighting in small size LCD panels. With integrated Schottky diode, OVP, and wide range of PWM dimming capability, the ISL97634 provides a simple, reliable, and flexible solution to the backlight designers.

The ISL97634 features a wide range of PWM dimming control capability. It allows dimming frequency as low as DC to 32kHz beyond audible spectrum. The ISL97634 also features a feedback disconnect switch to prevent the output from being modulated by the PWM dimming signal that minimizes system disturbance.

The ISL97634 is available in the 8 Ld TDFN (2mmx3mm) package. There are 14V, 18V, and 26V OVP options that are suitable for various number of LEDs in series. The ISL97634 is specified for operation over the -40°C to +85°C ambient temperature at input voltage from 2.4V to 5.5V.

Related Literature

- See TB470, “Using the ISL97634 White LED Driver Demo Board”

Features

- Drives Up to 26V Output
- Integrated over-voltage protection (OVP) of 14V, 18V, and 26V for various number of LEDs in series
- PWM Dimming Control From DC to 32kHz
- Output Disconnect Switch
- Integrated Schottky Diode
- 2.4V to 5.5V Input
- 85% Efficiency
- 1.4MHz Switching Frequency Allows Small LC
- 1µA Shutdown Current
- Internally Compensated
- 8 Ld TDFN (2mmx3mm)
- Pb-Free (RoHS Compliant)

Applications

- LED Backlighting for:
  - Cell phones
  - Smartphones
  - MP3
  - PMP
  - Automotive Navigation Panel
  - Portable GPS

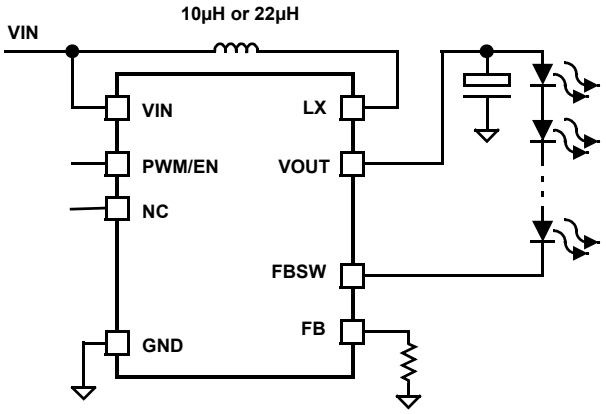
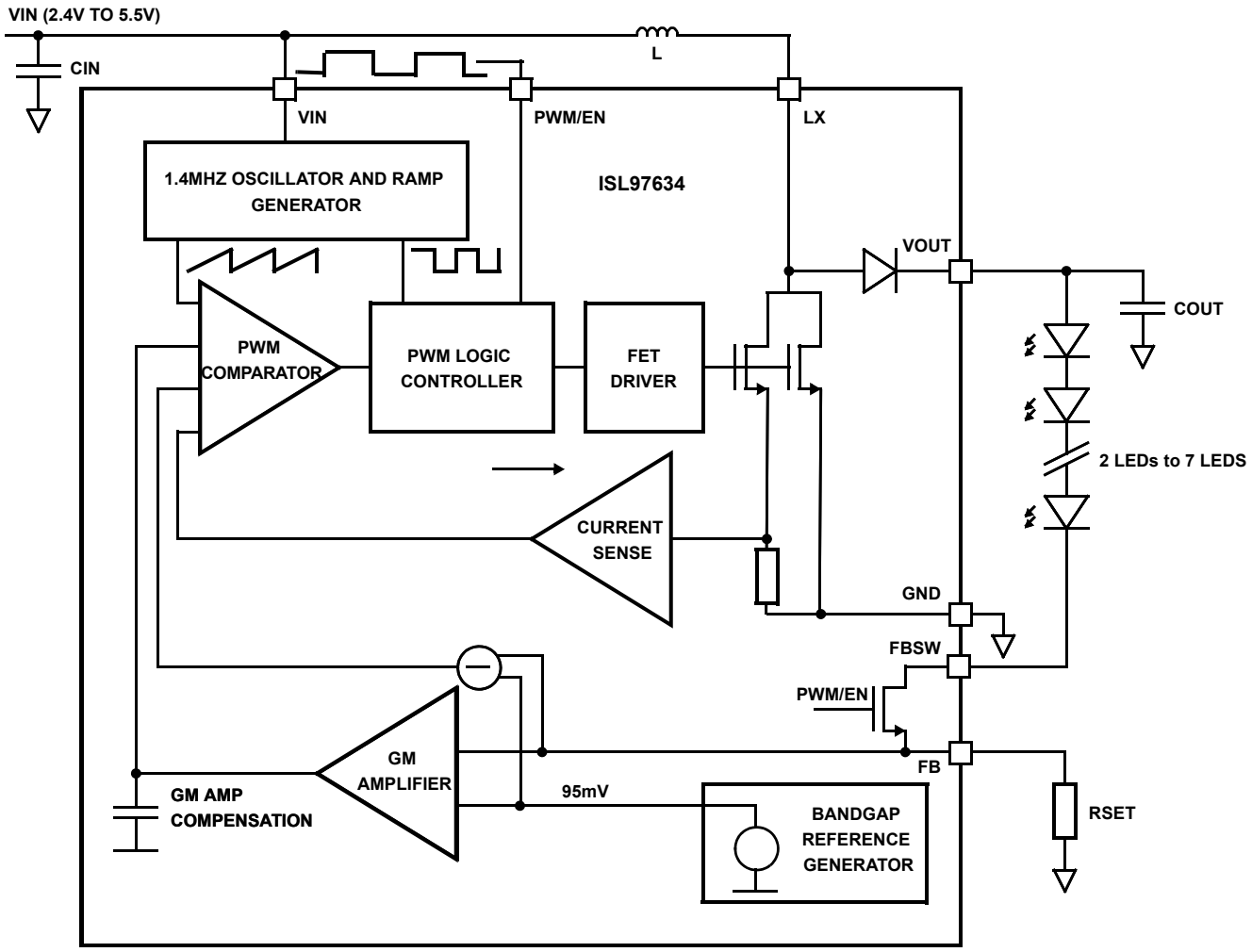
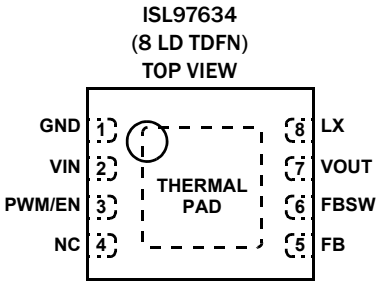


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Block Diagram



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	GND	Ground Pin. Connect to local ground.
2	VIN	Input Supply Pin. Connect to the input supply voltage, the inductor and the input supply decoupling capacitor.
3	PWM/EN	PWM or Enable Pin. Connect external PWM signal allows pulse width modulation current operation. Enable signal allows peak current operation or disable signal shuts down the device.
4	NC	No Connect
5	FB	Feedback Pin. Connect the sense resistor between FB and ground. The cathode of bottom LED can also be connected at this pin if the output current is not to be PWMed.
6	FBSW	FB Disconnect Switch. Connect to the cathode of the bottom LED if the output current to be PWMed.
7	VOUT	Output Pin. Connect to the anode of the top LED and the output filter capacitor.
8	LX	Switching Pin. Connect to inductor.
	PAD	Connect to ground plane on the PCB to maximize thermal performance.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OVP OPTIONS (V)	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL97634IRT14Z-T	ELE	14	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97634IRT14Z-TK	ELE	14	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97634IRT18Z-T	ELF	18	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97634IRT18Z-TK	ELF	18	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97634IRT26Z-T	ELG	26	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A
ISL97634IRT26Z-TK	ELG	26	-40 to +85	8 Ld 2x3 TDFN	L8.2x3A

NOTES:

1. Please refer to TB347 for details on reel specifications
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97634. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Input Voltage (V_{IN}) . . . . . -0.3V to 6V
LX Voltage . . . . . -0.3V to 28V
FBSW Voltage . . . . . -0.3V to 28V
All Other Pins . . . . . -0.3V to 6V

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld TDFN Package (Notes 4, 5).	77	12

Maximum Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed over temperature of -40°C to +85°C unless otherwise stated. Typ values are for information purposes only at TJ = TC = TA = +25°C.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications V_{IN} = $V_{PWM/EN}$ = 3V. Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{IN}	Supply Voltage		**2.4**		**5.5**	V
I_{IN}	Supply Current	PWM/EN = 3V, enabled, not switching		0.8	**1.5**	mA
		PWM/EN = 0V, disabled			**1**	µA
f_{SW}	Switching Frequency		**1,300**	1,450	**1,600**	kHz
DMAX	Maximum Switching Duty Cycle		**90**	95		%
I_{LIM}	LX Current		**400**	470		mA
$R_{SW(LX)}$	LX Switch ON-Resistance	ILX = 100mA		900		mΩ
ILEAK	LX Switch Leakage Current	VLX = 28V		0.01	**1**	µA
VFB	Feedback Voltage		**90**	95	**100**	mV
IFB	FB Pin Bias Current	VFB = 95mV			**1**	µA
$R_{SW(FBSW)}$	FBSW Switch ON-Resistance			10		Ω
V_{DIODE}	Schottky Diode Forward Voltage	IDIODE = 100mA, T_A = +25°C	600		850	mV
OVP	Overvoltage Protection	ISL97634IRT14Z	**14**			V
		ISL97634IRT18Z	**18**			V
		ISL97634IRT26Z	**26**		**28**	V
VIL	Logic Low Voltage of PWM/EN				**0.6**	V
VIH	Logic High Voltage of PWM/EN		**1.5**			V
PWM_on	Minimum PWM On-Time			1.5		µs
EN_delay	EN to Vout Delay			200		µs

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

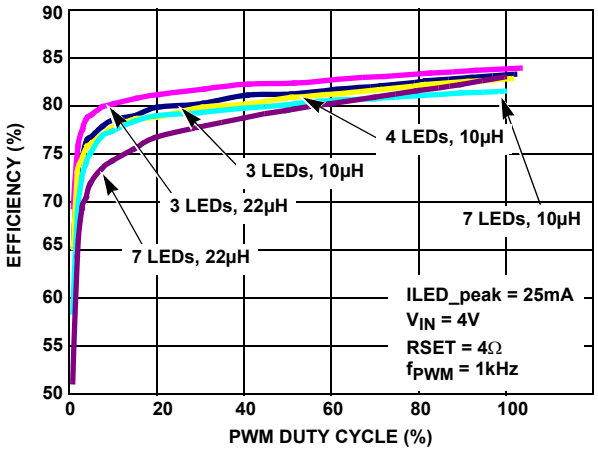


FIGURE 2. EFFICIENCY vs PWM DUTY CYCLE

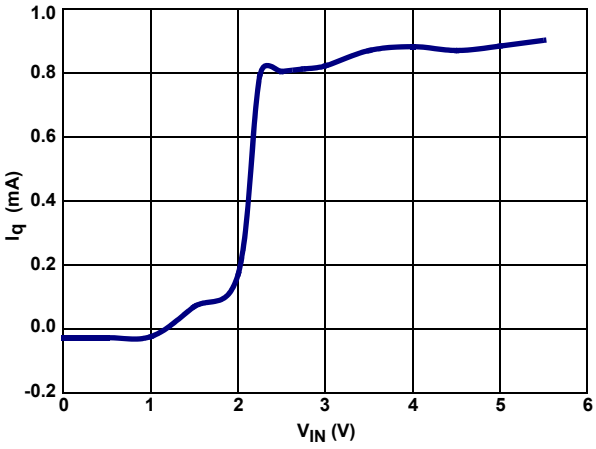


FIGURE 3. QUIESCENT CURRENT vs V_{IN} (PWM/EN = HI)

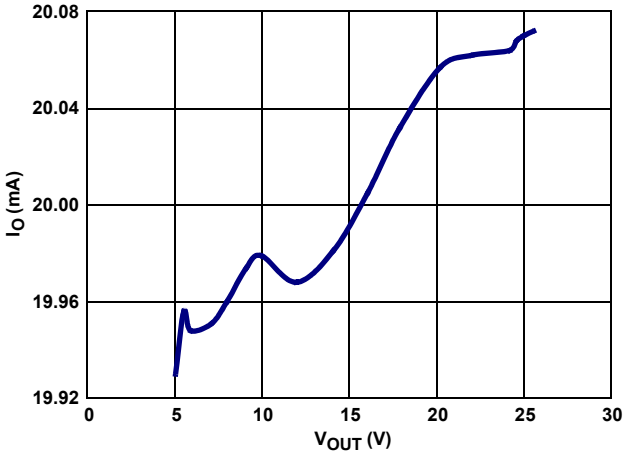


FIGURE 4. LOAD REGULATION (V_{IN} = 4V)

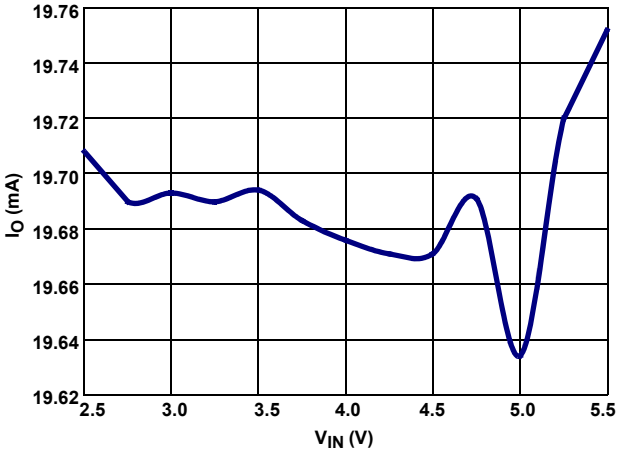


FIGURE 5. LINE REGULATION

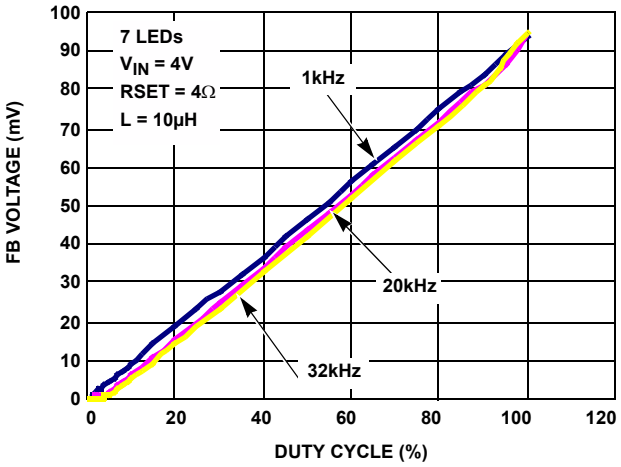


FIGURE 6. DIMMNG LINEARITY (FB VOLTAGE) vs DUTY CYCLE

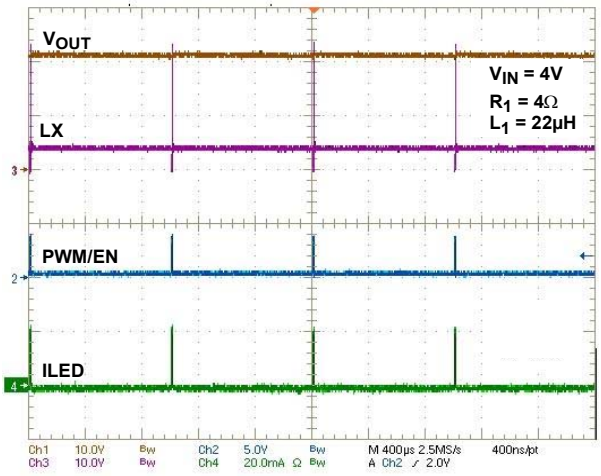


FIGURE 7. PWM DIMMING AT 1kHz, D = 1%

Typical Performance Curves (Continued)

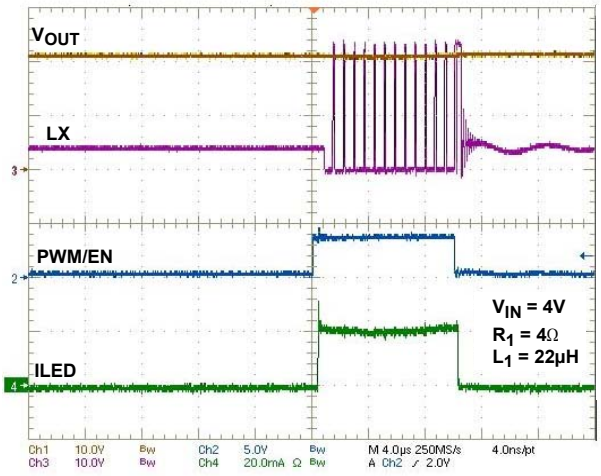


FIGURE 8. PWM DIMMING AT 1kHz, D = 1% ZOOM IN

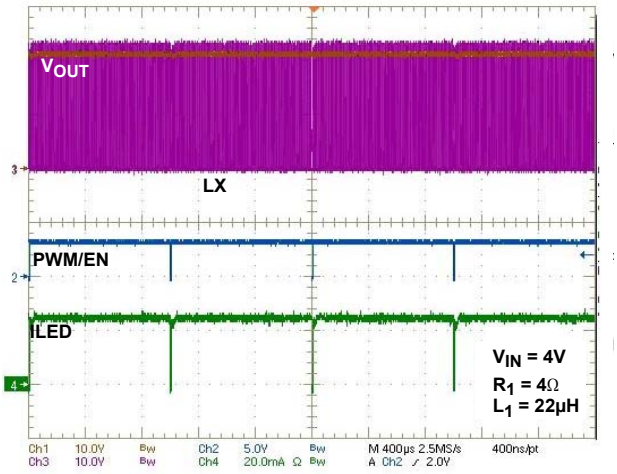


FIGURE 9. PWM DIMMING AT 1kHz, D = 99%

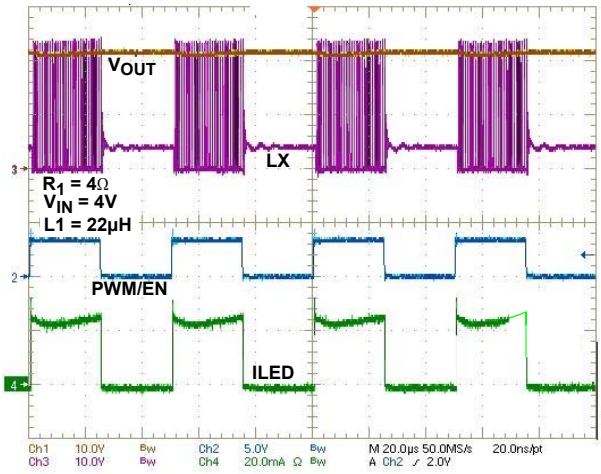


FIGURE 10. PWM DIMMING AT 20kHz, D = 50%

Detailed Description

The ISL97634 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. There are three OVP thresholds set at 14V, 18V and 26V respectively. The ISL97634 operates from an input voltage of 2.4V to 5.5V and ambient temperature from -40°C to +85°C. The switching frequency is around 1.45MHz and allows the driver circuit to employ small LC components. The peak forward current of the LED is set using the R_{SET} resistor. In the steady state mode, the LED peak current is given by Equation 1:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad \text{(EQ. 1)}$$

PWM Dimming

The ISL97634's PWM/EN pin can be tied permanently to high for a fixed current operation. On the other hand, the ISL97634 can be applied with an external PWM signal to pulse width modulated output current. It is well understood that the LED brightness is a linear function of the LED current. In addition, the average LED current corresponds to the duty cycle "D" of the PWM signal as shown in Equation 2:

$$I_{LED\text{-}AVG} = \frac{V_{FB}}{R_{SET}} \cdot D \quad \text{(EQ. 2)}$$

As a result, PWM signal provides a means to dim the LED brightness. PWM dimming offers the best LEDs matching over DC dimming. It is because the LED peak current operating point is far away from the knee of the diode I-V curve where part to part variations are high. The PWM dimming test results are shown in Figure 7 with two PWM frequencies, 1kHz and 20kHz. The vertical scale parameter FB is proportional to the current and therefore the brightness.

For the ISL97634, PWM dimming provides linear dimming adjustment with low frequency signal, such as 1kHz and below. The applied PWM dimming signal can be up to 32kHz;

however, the dimming linearity is compromised at low duty cycles as their durations are too short for the ISL97634's control loop to respond properly. This non-ideality behavior does not cause any functional problem. The PWM dimming linear responses in Figure 6 are expanded in Figure 11. At 1kHz PWM dimming, the duty cycle can virtually vary from below 1% to DC. On the other hand, at 20kHz PWM dimming, the linearity range is from 5% to DC only.

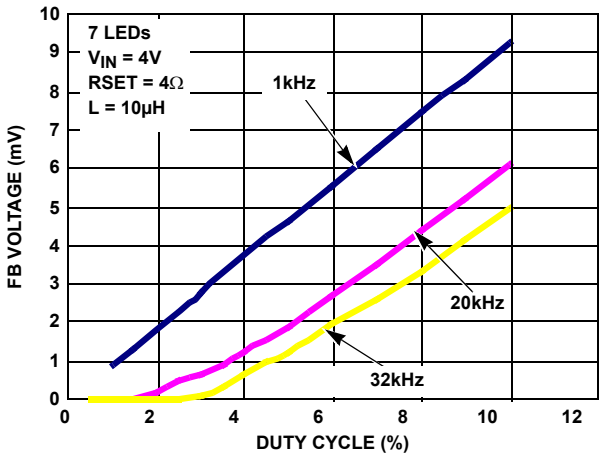


FIGURE 11. DIMMING LINEARITY vs DUTY CYCLES ZOOM IN

The low level non-linearity effects at high frequency PWM dimming is also reflected in the efficiency measurements in Figure 12.

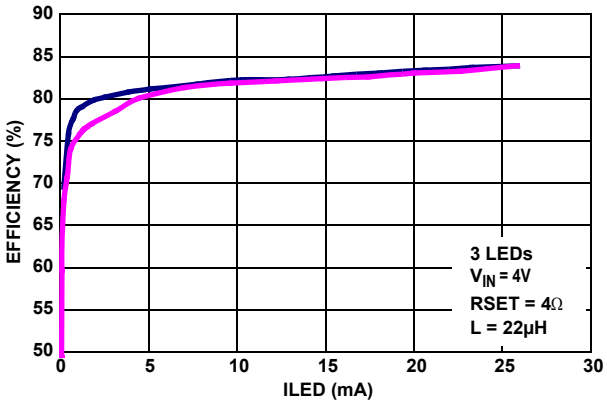


FIGURE 12. EFFICIENCY vs PWM DIMMING FREQUENCIES

Feedback Disconnect Switch

The ISL97634 functions properly without using the FBSW. However, the output capacitor will discharge during the PWM off time resulting in poor dimming linearity at low duty cycles. The output discharge effect can be seen in Figure 13. Moreover, the output is modulated by the PWM signal that may create interference to other systems.

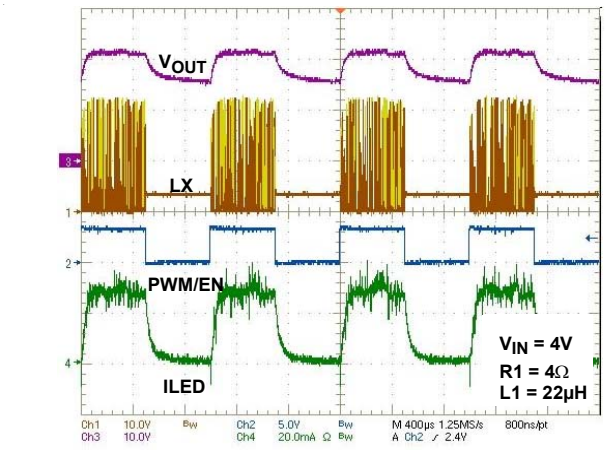


FIGURE 13. PWM DIMMING AT 1kHz WITHOUT USING FBSW

The FBSW should be used for PWM dimming as illustrated in the "Typical Application Circuit" on page 1. During the PWM off time, the FBSW is opened. The LEDs are floating and therefore the output capacitor has no path to discharge. The LED current responds accurately with the PWM signal (see Figure 14). The output switches very quickly to the target current with minimal settling ringing and without being modulated by the PWM signal, and therefore minimizes any system disturbance.

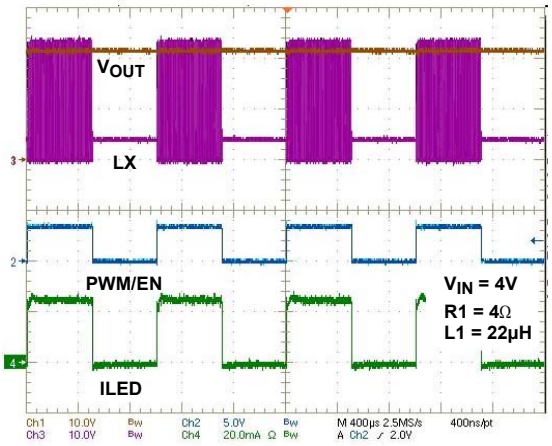


FIGURE 14. PWM DIMMING AT 1kHz USING FBSW

Overvoltage Protection

The ISL97634 comes with overvoltage protection. The OVP trip points are at 14V, 18V and 26V for ISL97634IRT14Z, ISL97634IRT18Z and ISL97634IRT26Z respectively. The maximum LED current and OVP threshold are shown in Table 1. When the device reaches the OVP, the LX stops switching, disabling the boost circuit until V_{OUT} falls about 7% below the OVP threshold. At this point, LX will be allowed to switch again. The OVP event will not cause the device to shutdown.

An output capacitor that is only rated for the required voltage range can therefore be used, which will optimize the component costs in some cases.

TABLE 1.

PART NO.	OVP	MAX ILED
ISL97634IRT14Z	14V	70mA
ISL97634IRT18Z	18V	50mA
ISL97634IRT26Z	26V	30mA

Shutdown

When PWM/EN is taken low the ISL97634 enters into the power-down mode where the supply current is reduced to less than 1µA. The device resumes normal when the PWM/EN goes high.

Components Selection

The input capacitance is typically 0.22µF. The output capacitor should be in the range of 0.22µF to 1µF. X5R or X7R type of ceramic capacitors of the appropriate voltage rating are recommended.

When choosing an inductor, make sure the average and peak current ratings are adequate by using Equations 3, 4 and 5 (80% efficiency assumed):

$$I_{LAVG} = \frac{I_{LED} \cdot V_{OUT}}{0.8 \cdot V_{IN}} \quad \text{(EQ. 3)}$$

$$I_{LPK} = I_{LAVG} + \frac{1}{2} \cdot \Delta I_L \quad \text{(EQ. 4)}$$

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{L \cdot V_{OUT} \cdot f_{OSC}} \quad \text{(EQ. 5)}$$

Where:

- ΔI_L is the peak-to-peak inductor current ripple in Amps
- L is the inductance in H
- f_{OSC} is the switching frequency, typically 1.45MHz

The ISL97634 supports a wide range of inductance values (10µH to ~82µH). For lower inductor values or lighter loads, the boost inductor current may become discontinuous. For high boost inductor values, the boost inductor current will be in continuous mode.

In addition to the inductor value and switching frequency, the input voltage, number of LEDs and the LED current also affects whether the converter operates in continuous conduction or discontinuous conduction mode. Both operating modes are allowed and normal. The discontinuous conduction mode yields lower efficiency due to higher peak current.

Compensation

The product of the output capacitor and the load create a pole while the inductor creates a right half plane zero. Both of these attributes degrade the phase margin but the ISL97634 has internal compensation network that ensures the device operates reliably under the specified conditions. The internal compensation and the highly integrated functions of the ISL97634 make it a design friendly device to be used in high volume, high reliability applications.

Applications

Analog Dimming

Analog dimming is usually not recommended because of the brightness non-linearity at low levels dimming. However, some systems are EMI or noise sensitive that analog dimming may be more suitable than PWM dimming under those situations. The ISL97632 is part of the same family as the ISL97634 and has been designed with a serial interface to give access to 32 separate dimming levels. Alternatively analog dimming can be achieved by applying a variable DC voltage (V_{Dim}) at the FB pin (see Figure 15) to adjust the LED current. As the DC dimming signal voltage increases above VFB, the voltage drop on R_1 and R_2 increases and the voltage drop on RSET decreases. Thus, the LED current decreases as shown in Equation 6:

$$I_{LED} = \frac{V_{FB} \cdot (R_1 + R_2) - V_{Dim} \cdot R_1}{R_2 \cdot R_{SET}} \quad \text{(EQ. 6)}$$

If V_{DIM} is taken below FB, the inverse will happen and the brightness will increase.

The DC dimming signal voltage can be a variable DC voltage from a POT, a DCP (Digitally Controlled Potentiometer), or a DC voltage generated by filtering a high frequency PWM control signal.

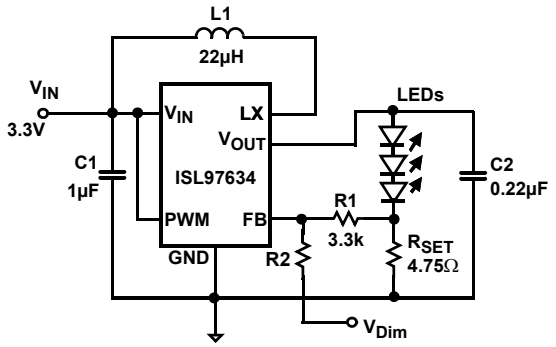


FIGURE 15. ANALOG DIMMING CONTROL APPLICATION CIRCUIT

As brightness is directly proportional to LED currents, V_{Dim} may be calculated for any desired "relative brightness" (F) using Equation 7:

$$V_{Dim} = \frac{R_2}{R_1} \cdot V_{FB} \cdot \left(1 + \frac{R_1}{R_2} - F\right) \quad \text{(EQ. 7)}$$

Where F = I_{LED} (dimmed)/I_{LED} (undimmed).

These equations are valid for values of R_1 and R_2 such that both R_1>>RSET and R_2>>RSET.

The analog dimming circuit can be tailored to a desired relative brightness for different V_{Dim} ranges using Equation 8.

$$R_2 = \frac{[(V_{Dim\_max} - V_{FB}) \bullet R_1]}{[V_{FB} \bullet (1 - F_{min})]} \quad \text{(EQ. 8)}$$

Where V_{Dim_max} is the maximum V_{Dim} voltage and F_{min} is the minimum relative brightness (i.e., the brightness with V_{Dim_max} applied).

i.e., V_{Dim_max} = 5V, F_{min} = 10% (i.e., 0.1), R_2 = 189k
i.e., V_{Dim_max} = 1V, F_{min} = 10% (i.e., 0.1), R_2 = 35k

Efficiency Improvement

Figure 2 shows the efficiency measurements during PWM operation. The choice of the inductor has a significant impact on the power efficiency. Equation 4 shows the higher the inductance, the lower the peak current, therefore, the lower the conduction and switching losses. On the other hand, it has also a higher series resistance. Nevertheless, the efficiency improvement effect by lowering the peak current is greater than the resistance increases with larger value of inductor. Efficiency can also be improved for systems that have high supply voltages. Since the ISL97634 can only supply from 2.4V to 5.5V, V_{IN} must be separated from the high supply voltage for the boost circuit as shown in Figure 16 and the efficiency improvement is shown in Figure 17.

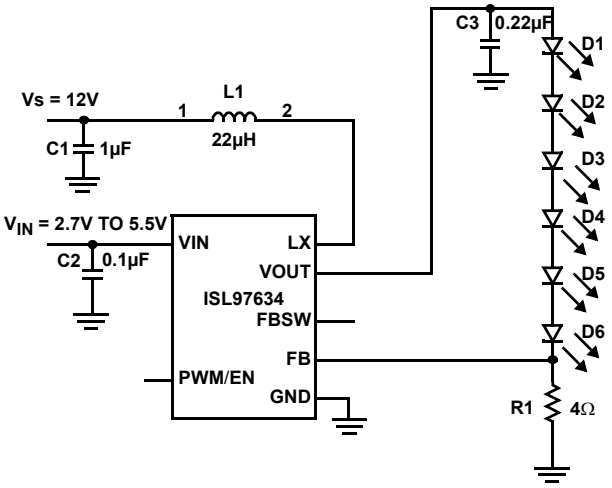


FIGURE 16. SEPARATE HIGH INPUT VOLTAGE FOR HIGHER EFFICIENCY OPERATION

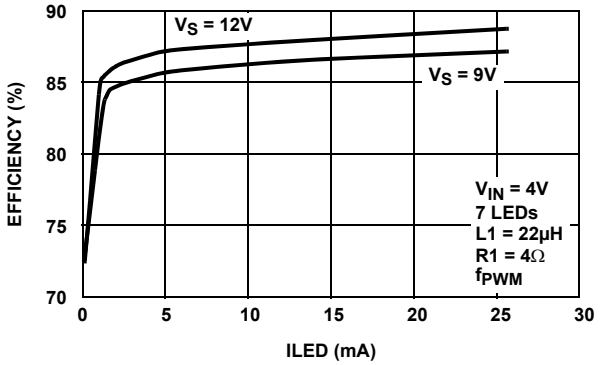


FIGURE 17. EFFICIENCY IMPROVEMENT WITH 9 AND 12V INPUTS

Operation with VOUT above 26V

For LED backlighting applications that need an output voltage above 26V, the voltage range of the ISL97634 is not sufficient. However, the ISL97634 can be used as an LED controller with an external protection MOSFET connected in cascode fashion to achieve higher output voltage as shown in Figure 18. A 60V logic level N-Channel MOSFET is configured such that its drain ties between the inductor and the anode of Schottky diode, its gate ties to the input, and its source ties to the ISL97634 LX node connecting to the drain of the internal switch. When the internal switch turns on, it pulls the source of M1 down to ground and LX conducts as normal. When the internal switch turns off, the source of M1 will be pulled up by the follower action of M1, limiting the maximum voltage on the ISL97634 LX pin to below V_{IN}, but allowing the output voltage to go much higher than the breakdown limit on the LX pin. The switch current limit and maximum duty cycle will not be changed by this setup, so input voltage will need to be carefully considered to make sure that the required output voltage and current levels are achievable. Because the source of M1 is effectively floating when the internal LX switch is off, the drain-to-source capacitance of M1 may be sufficient to capacitively pull the node high enough to break down the gate oxide of M1. To prevent this, V_{OUT} should be connected to V_{IN}, allowing the internal Schottky diode to limit the peak voltage. This will also hold the VOUT pin at a known low voltage, preventing the built in OVP function from causing problems. This OVP function is effectively useless in this mode as the real output voltage is outside its intended range. If the user wants to implement their own OVP protection (to prevent damage to the output capacitor), they should insert a zener diode from VOUT to the FB pin. In this setup, it would be wise not to use the FBSW to FB switch, as otherwise, the zener diode will have to be a high power one capable of dissipating the entire LED load power. Then the LED stack can then be connected directly to the sense resistor via a 10kΩ resistor to FB. A zener can be placed from VOUT to the FB pin allowing an overvoltage event to pull-up on FB with a low breakdown current (and thus low power zener diode) as a result of the 10kΩ resistor.

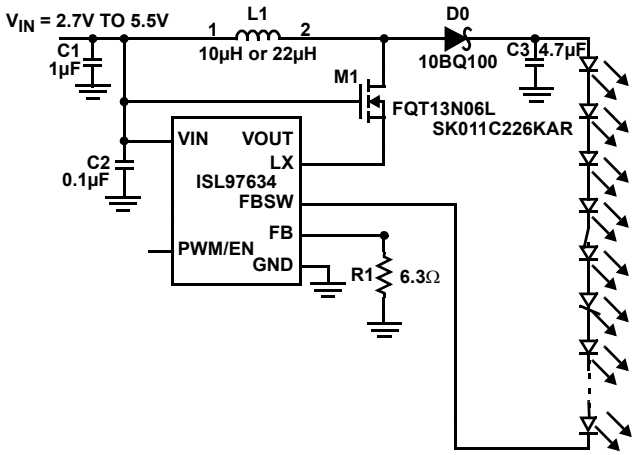


FIGURE 18. HIGH VOLTAGE LED DRIVER USING A CASCODE

SEPIC Operation

For applications where the output voltage is not always above the input voltage, a buck or boost regulation is needed. A SEPIC (Single-Ended Primary Inductance Converter) topology, shown in Figure 19, can be considered for such an application. A single cell Li-ion battery operating a cellular phone backlight or flashlight is one example. The battery voltage is between 2.5V and 4.2V, depending on the state of charge. On the other hand, the output may require only one 3V to 4V medium power LED for illumination because the light guard of the backlight assembly is optimized for cost efficiency trade-off reason.

In fact, a SEPIC configured LED driver is flexible enough to allow the output to be well above or below the input voltage, unlike the previous example. Another example is when the number of LEDs and input requirements are different from platform to platform, a common circuit and PCB that fit all the platforms in some cases

may be beneficial enough that it outweighs the disadvantage of adding additional component cost. L_1 and L_2 can be a coupled inductor in one package.

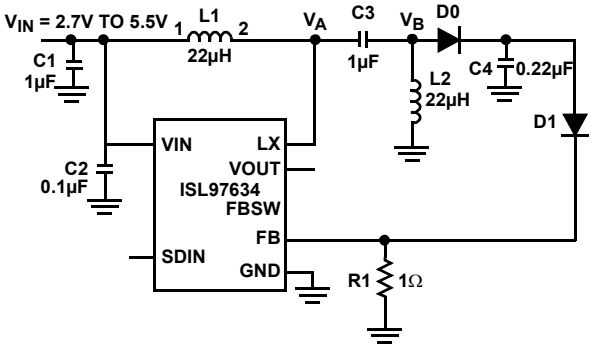


FIGURE 19. SEPIC LED DRIVER

The simplest way to understand SEPIC topology is to think about it as a boost regulator where the input voltage is level shifted downward at the same magnitude and the lowest reference level starts at $-V_{IN}$ rather than 0V.

The SEPIC works as follows; assume the circuit in Figure 19 operates normally when the ISL97634 internal switch opens and it is in the PWM off state. After a short duration where few LC time constants elapsed, the circuit is considered in the steady-state within the PWM off period that L_1 and L_2 are shorted. V_B is therefore shorted to the ground and C_3 is charged to V_{IN} with $V_A = V_{IN}$. When the ISL97634 internal switch closes and the circuit is in the PWM on-state, V_A is now pulled to ground. Since the voltage in C_3 cannot be changed instantaneously, V_B is shifted downward and becomes $-V_{IN}$. The next cycle when the ISL97634 switch opens, V_B boosts up to the targeted output like the standard boost regulator operation, except the lowest reference point is at $-V_{IN}$. The output is approximated in Equation 9:

$$V_{OUT} = V_{IN}\frac{D}{(1-D)} \quad \text{(EQ. 9)}$$

where D is the on-time of the PWM duty cycle.

The convenience of SEPIC comes with some trade-off in addition to the additional L and C costs. The efficiency is usually lowered because of the relatively large efficiency loss through the Schottky diode if the output voltage is low. The L_2 series resistance also contributes additional loss. Figure 20 shows the efficiency measurement of a single LED application as the input varies between 2.7V and 4.2V.

Note V_B is considered the level-shifted LX node of a standard boost regulator. The higher the input voltage, the lower the V_B voltage will be during PWM on period. The result is that the efficiency will be lower at higher input voltages because the SEPIC has to work harder to boost up to the required level. This behavior is the opposite to the standard boost regulator's and the comparison is shown in Figure 20.

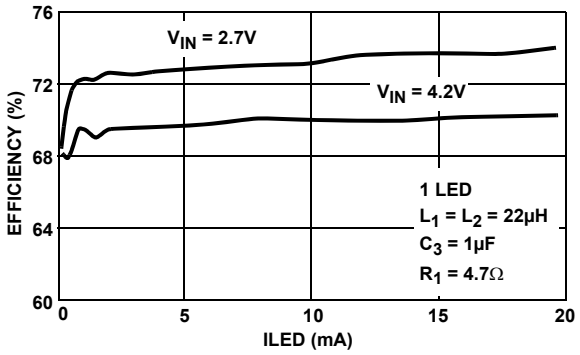


FIGURE 20. EFFICIENCY MEASUREMENT OF A SINGLE LED SEPIC DRIVER

PCB Layout Considerations

The layout is very important for the converter to function properly. R_{SET} must be located as close as possible to the FB and GND pins. Longer traces to the LEDs are acceptable. Similarly, the supply decoupling cap and the output filter cap should be as close as possible to the VIN and VOUT pins.

The heat of the IC is mainly dissipated through the thermal pad of the package. Maximizing the copper area connected to this pad if possible and connect to ground plane on the PCB. Connect all vias to the correct voltage potential (power plane) indicated in the datasheet. In addition, a solid ground plane is always helpful for the EMI performance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 27, 2013	FN6264.4	Changed the information of "max 7 LED in series" to "up to 26V" for more accuracy. Page 1: In first paragraph, changed "PWM boost LED driver that is suitable for 1.8" to 3.5" LCDs that employ 2 to 7 white LEDs for backlighting." to " PWM boost LED driver that is suitable for LED backlighting in small size LCD panels." Added “Related Literature” In “Features”, changed "OVP (14V, 18V, and 26V for 3, 4 and 7 LEDs Applications)" to "Integrated over-voltage protection (OVP) of 14V, 18V, and 26V for various number of LEDs in series". Changed "Drives Up to 7 LEDs in Series (3.5V/20mA type)" to "Drives Up to 26V Output" Ordering Information on page 3 Added OVP Options column. Updated Pb-free note to new verbiage based on lead finish. Added note to Min Max column of spec table "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." Added "Boldface limits apply" verbiage to common conditions of spec table. Bolded applicable specs. “Overvoltage Protection” on page 7, changed "The maximum numbers of LEDs.." to "The maximum LED current.." Page 8, Table 1, deleted "MAX NO.OF LEDS" column Page 9: Changed section title from "8 LEDs Operation" to “Operation with VOUT above 26V” In same section, changed first sentence from "For medium size LCDs that need more than 7 low power LEDs for backlighting, such as a portable media player or automotive navigation panel displays, the voltage range.." to "For LED backlighting applications that need an output voltage above 26V, the voltage range.." Figure 17, changed inductance value from "2.2µH" to "10µH or 22µH" Figure 17, changed figure title from "conceptual 8 LEDs high voltage driver" to "high voltage LED driver using a cascode". Added “Revision History” and “About Intersil” on page 11. Page 12: Updated POD L8.2x3A to most recent rev. Updated format and added recommended land pattern

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

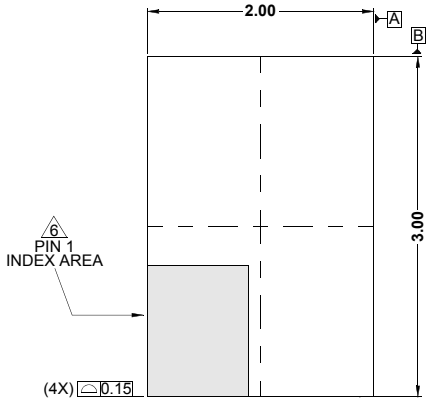
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

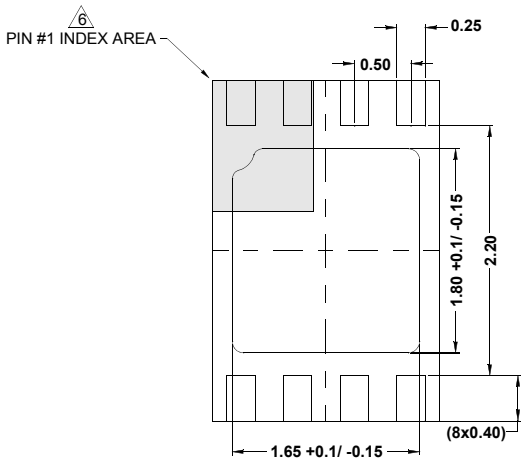
L8.2x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE WITH E-PAD

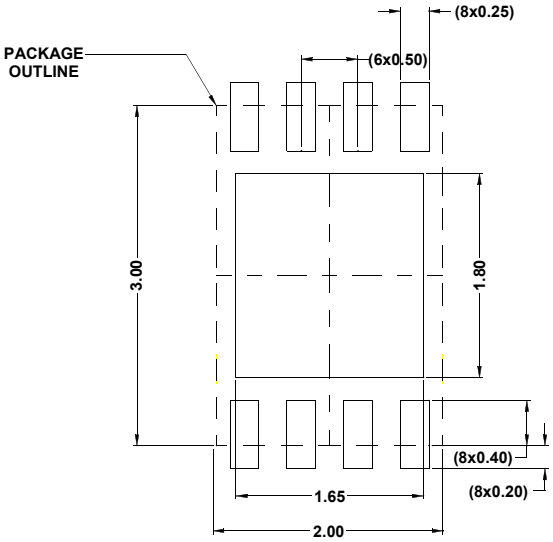
Rev 1, 06/09



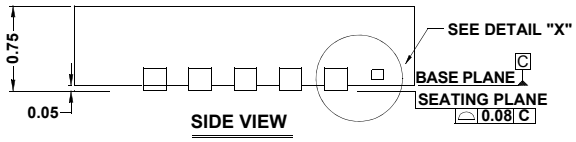
TOP VIEW



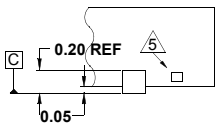
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.32mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.