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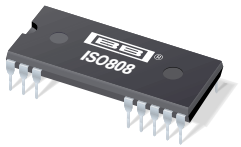


ISO808

Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10µS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

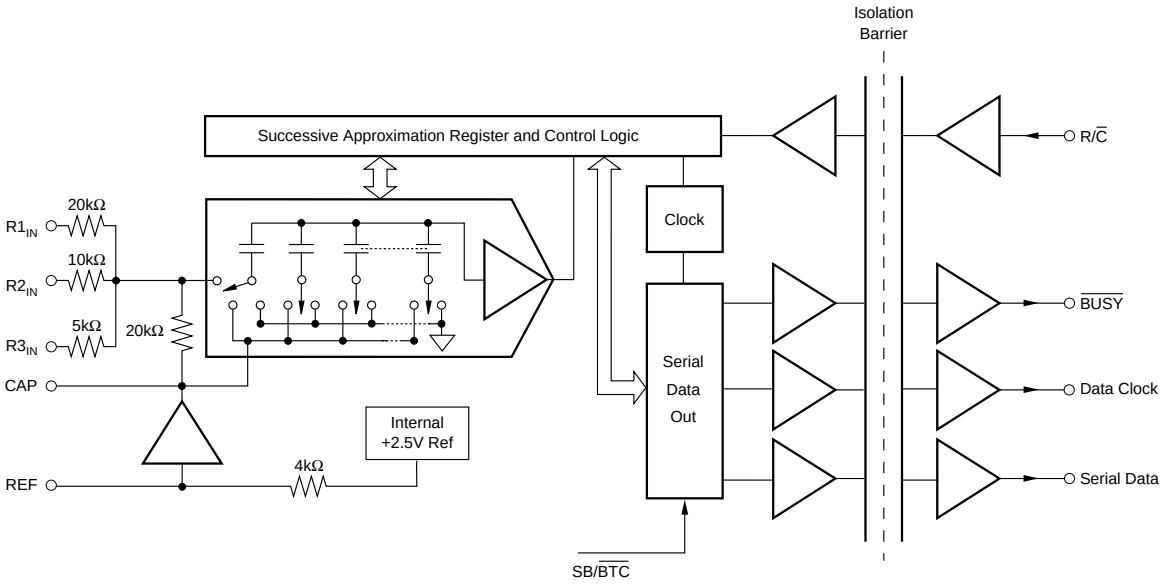
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO808 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO808 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, µP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



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SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P MIN	ISO808P TYP	ISO808P MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test[8]	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13}$ II 15		Ω II pF
Leakage Current[9]	240Vrms, 60Hz			1.7	µArms
	240Vrms, 50Hz			1.4	µArms
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Ranges			±10V, 0V to 5V, etc. (See Table I)		
Impedance			See Table I		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time			5.7	8	µs
Complete Cycle	Acquire and Convert			10	µs
Throughput Rate		100			kHz
DC ACCURACY					
Integral Linearity Error				±0.9	LSB[1]
Differential Linearity Error				±0.9	LSB
No Missing Codes			Guaranteed		
Transition Noise[2]			0.1		LSB
Full Scale Error[3,4]				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±2		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±5	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±0.5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 45kHz ±10V		90		dB[5]
Total Harmonic Distortion	f_{IN} = 45kHz ±10V		–90		dB
Signal-to-(Noise+Distortion)	f_{IN} = 45kHz ±10V		73		dB
Signal-to-Noise	f_{IN} = 45kHz ±10V		73		dB
Full-Power Bandwidth[6]			250		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			Sufficient to meet AC specs		ns
Overvoltage Recovery[7]			150		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use external buffer)			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –1.0		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			±0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			V

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SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P MIN	ISO808P TYP	ISO808P MAX	UNITS
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			16		mA
I_{DIG2}			10.8		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, f_S = 100kHz		175		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, ϕ_{JA}					
Plastic DIP			75		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO808P	28-Pin Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

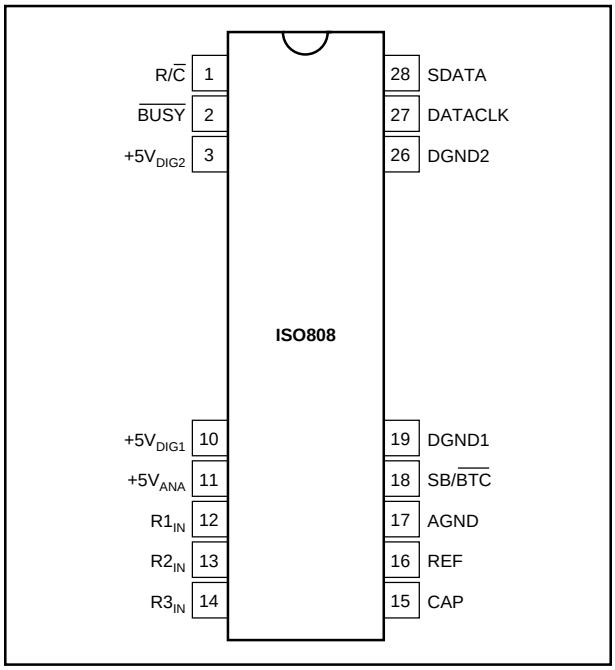
ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE (°C)	PACKAGE
ISO808P	±0.9	70	–40°C to +85°C	28-Pin Plastic DIP

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	R/$\overline{C}$	I	Read/$\overline{Convert}$. With $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion.
2	$\overline{BUSY}$	O	At the start of conversion $\overline{BUSY}$ goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	$R2_{N}$		Analog Input.
14	$R3_{N}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	SB/$\overline{BTC}$	I	Selects Straight Binary or Binary Two's Complement for output data format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 3 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{BUSY}$ Delay		120		ns
t_3	$\overline{BUSY}$ LOW			8	µs
t_4	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	R/$\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns

TABLE II. Conversion and Data Timing. T_A = –40°C to +85°C.

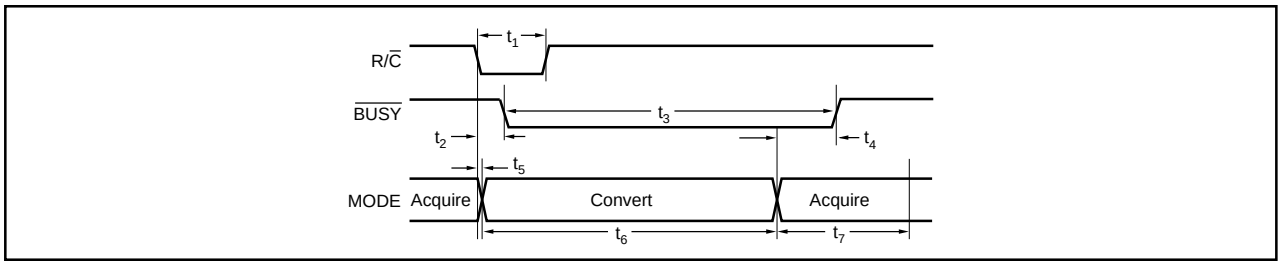


FIGURE 1. Basic Conversion Timing.

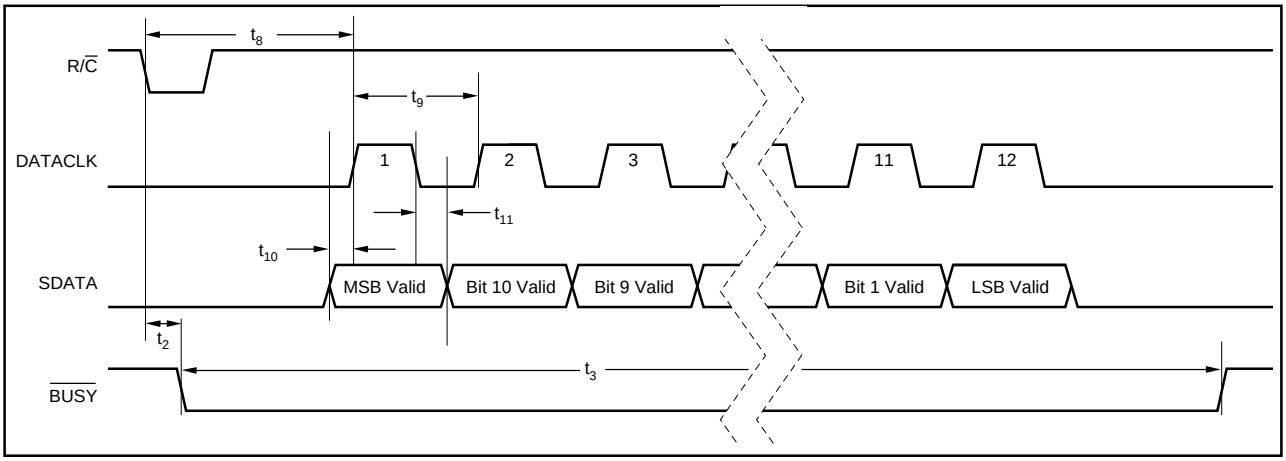


FIGURE 2. Serial Data Timing.

SPECIFIC FUNCTION	R/C	BUSY	DATACLK	SB/BTC	OPERATION
Initiate Conversion and Output Data	0	1	Output	X	Initiates Conversion “n”. Data from conversion “n–1” clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	1 > 0	1	Output	X	Initiates Conversion “n”. Data from conversion “n–1” clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Incorrect Conversions	0	0 > 1	X	X	R/C must be HIGH or a new conversion will be initiated without time for acquisition.
Selecting Output Format	X	X	X	0	Serial Data is output in Binary Two’s Complement format.
	X	X	X	1	Serial Data is output in Straight Binary format.

TABLE III. Control Truth Table.

							DIGITAL OUTPUT			
							BINARY TWO’S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
DESCRIPTION	ANALOG INPUT						HEX BINARY CODE	CODE	HEX BINARY CODE	CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS – 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	–2.44mV	–1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

TABLE IV. Output Codes and Ideal Input Voltages.

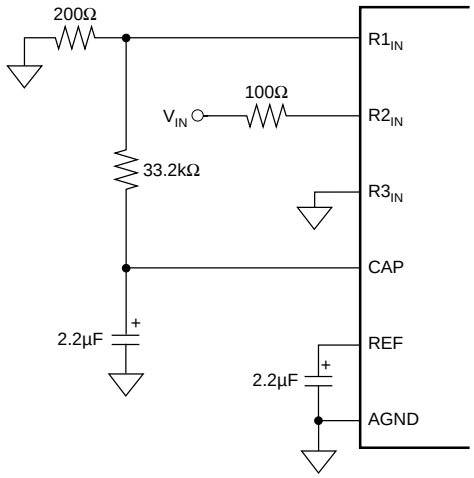
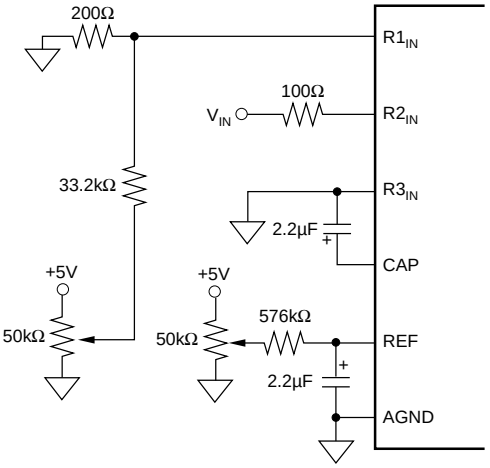
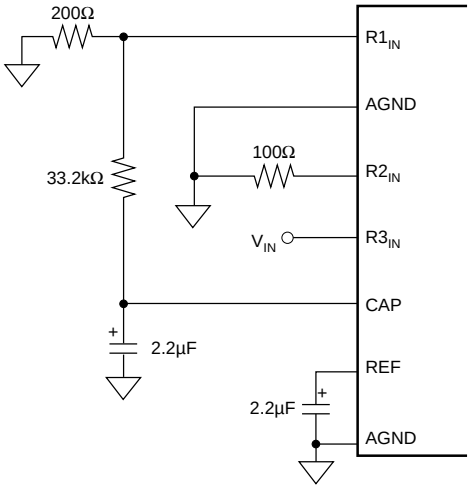
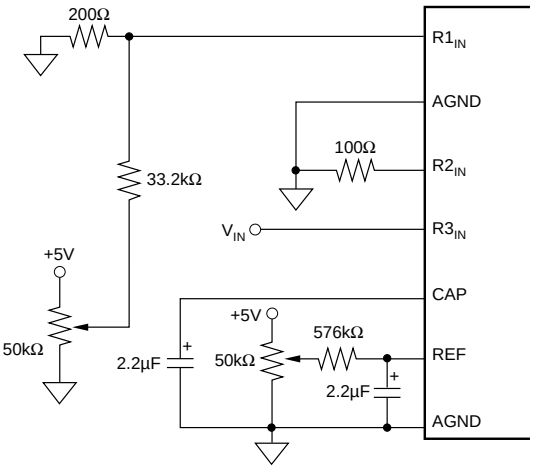
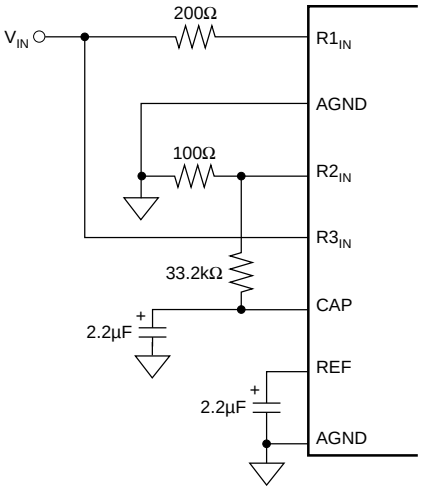
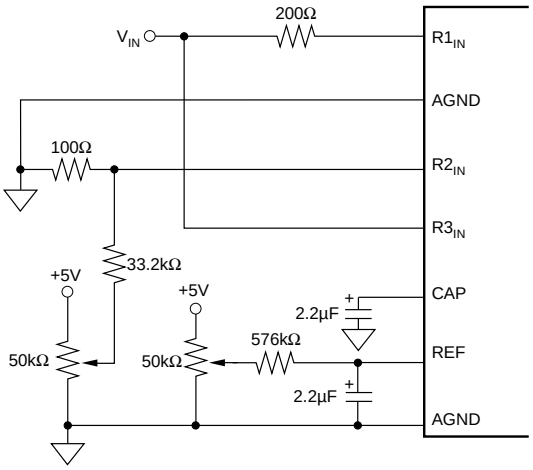
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

FIGURE 3a. Offset/Gain Circuits for Unipolar Input Ranges.

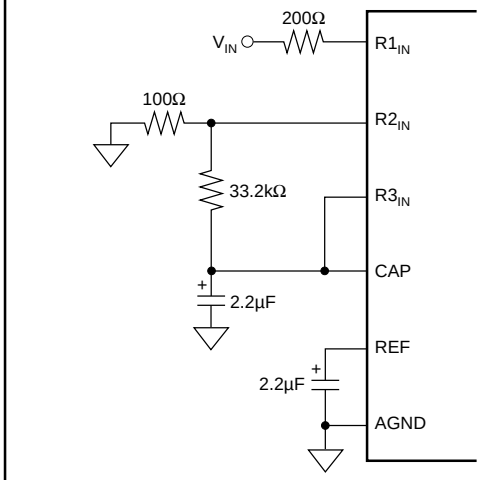
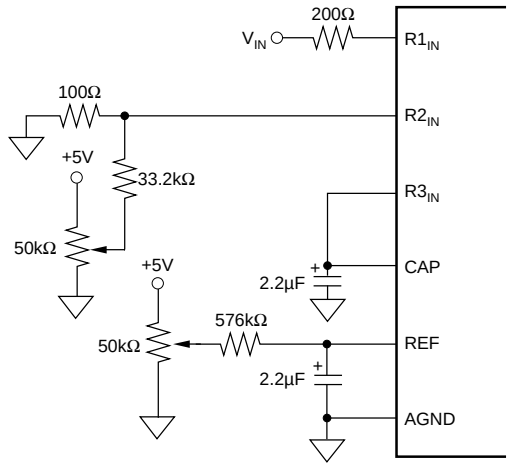
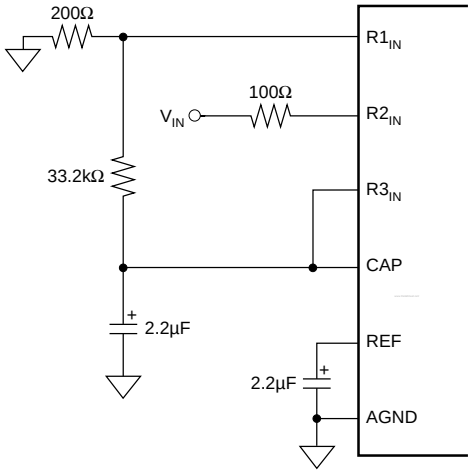
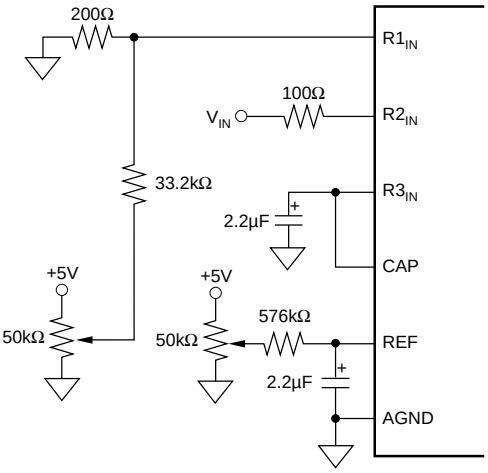
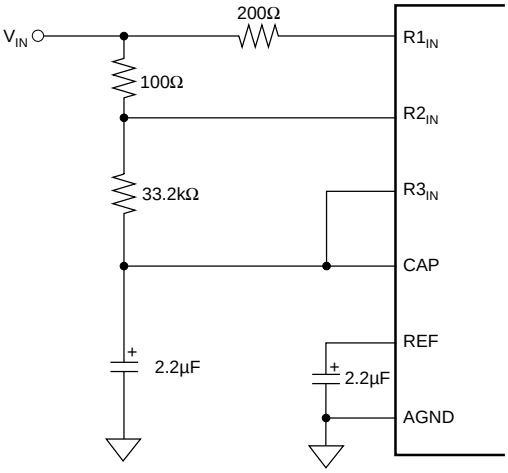
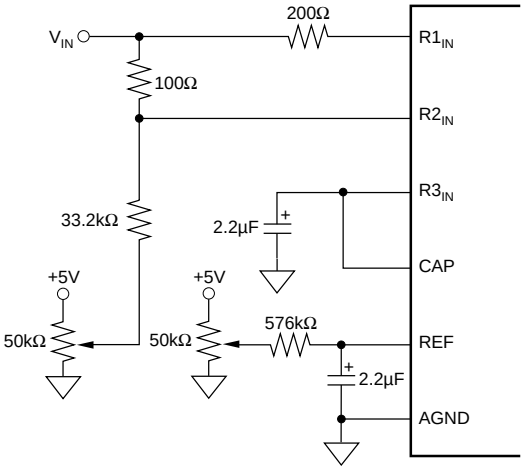
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

FIGURE 3b. Offset/Gain Circuits for Bipolar Input Ranges.