ISO8200B

Galvanic isolated octal high-side smart power solid state relay

Datasheet – target specification

Features

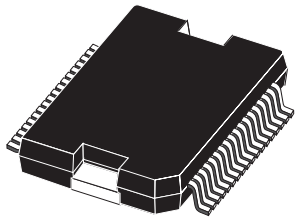
Type	V_{demag} (1)	$R_{DS(on)}$ (1)	I_{out} (1)	V_{cc}
ISO8200B	V_{cc}- 45 V	0.11 Ω	0.7 A	45 V

1. Per channel

- Parallel input interface
- Direct and synchronous control mode
- High common mode transient immunity
- Output current: 0.7 A per channel
- Short-circuit protection
- Channel overtemperature protection
- Thermal independence of separate channels
- Common output disable pin
- Case overtemperature protection
- Loss of GNDcc and V_{cc} protection
- Undervoltage shutdown with auto restart and hysteresis
- Overvoltage protection (V_{cc} clamping)
- Very low supply current
- Common fault open drain output
- 5 V and 3.3 V TTL/CMOS compatible I/Os
- Fast demagnetization of inductive loads
- Reset function for IC outputs disable
- ESD protection

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all types of loads (resistive, capacitive, inductive)



PowerSO36

Description

The ISO8200B is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{cc} for the power stage and V_{dd} for the digital stage). Additional embedded functions are: loss of GND protection, undervoltage shutdown with hysteresis, and reset function for immediate power output shutdown.

The IC is intended to drive any kind of load with one side connected to ground. Active channel current limitation combined with thermal shutdown, (independent for each channel), and automatic restart, protect the device against overload and short-circuit. In overload conditions, if junction temperature overtakes threshold, the channel involved is turned off and on again automatically after the IC temperature decreases below a reset threshold. If this condition causes case temperature to reach the limit threshold TCR, the overloaded channel is turned off and only restarts when case and junction temperature decrease down to the reset thresholds. Non-overloaded channels continue to operate normally. An internal circuit provides an OR-wired non latched common FAULT indicator signaling the channel OVT. The FAULT pin is an open drain active low fault indication pin.

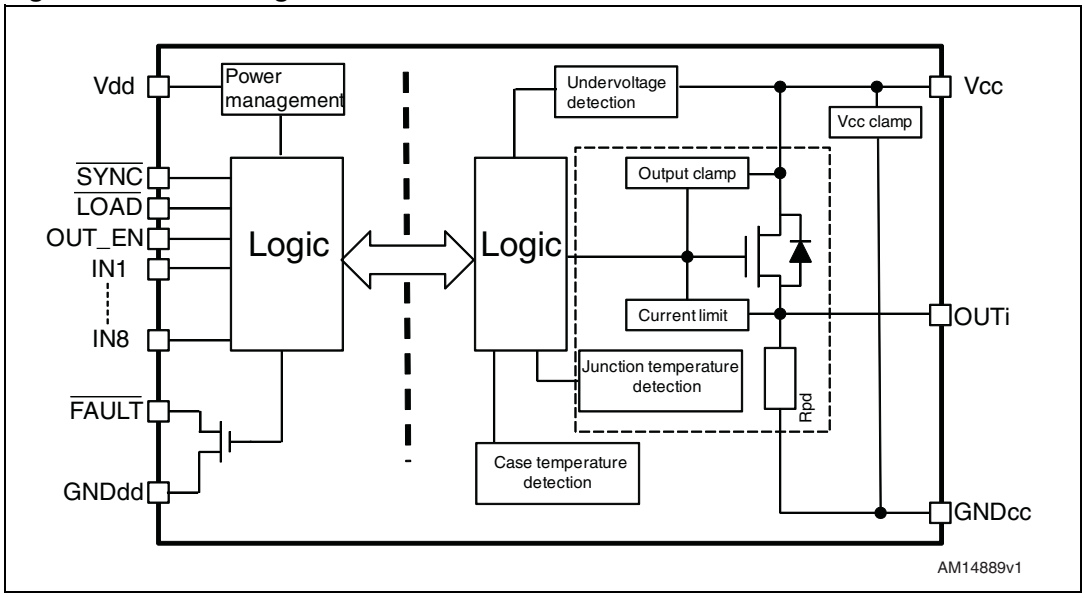
Table of contents

List of tables

List of figures

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

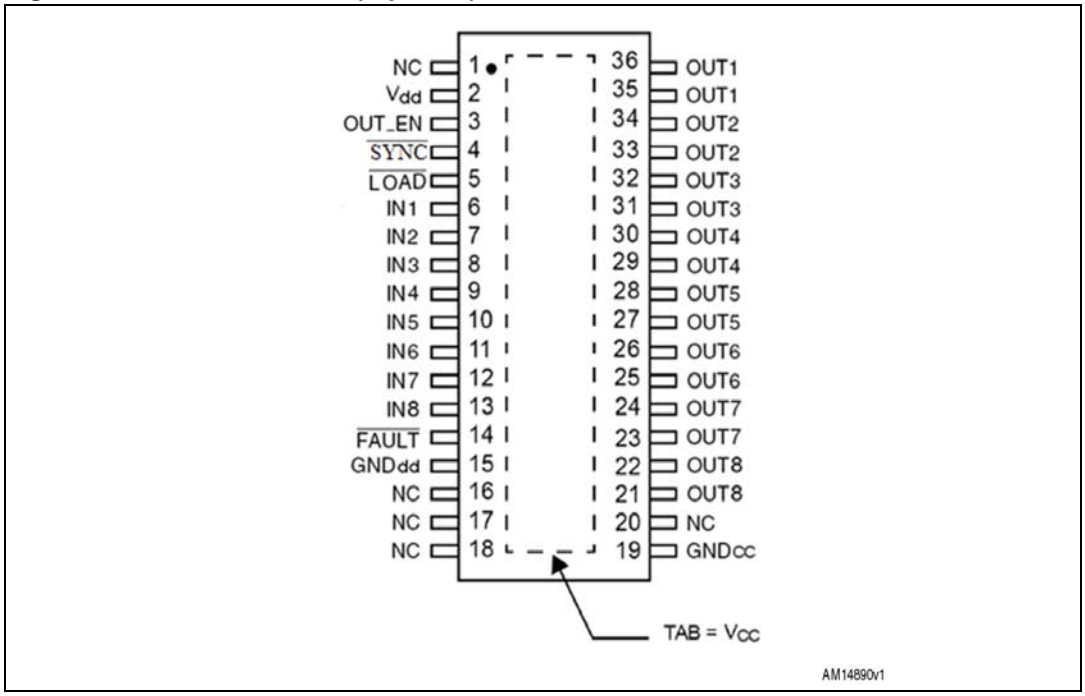


Table 1. Pin description

Pin	Name	Description
1	NC	Not connected
2	Vdd	Positive logic supply
3	OUT_EN	Output enable
4	$\overline{\text{SYNC}}$	Chip select
5	$\overline{\text{LOAD}}$	Load input data
6	IN1	Channel 1 input
7	IN2	Channel 2 input
8	IN3	Channel 3 input
9	IN4	Channel 4 input
10	IN5	Channel 5 input
11	IN6	Channel 6 input
12	IN7	Channel 7 input
13	IN8	Channel 8 input
14	$\overline{\text{FAULT}}$	Common fault indication - active low
15	GNDdd	Input logic ground, negative logic supply
16	NC	Not connected

Table 1. Pin description (continued)

Pin	Name	Description
17	NC	Not connected
18	NC	Not connected
19	GNDcc	Output power ground
20	NC	Not connected
21	OUT8	Channel 8 power output
22	OUT8	Channel 8 power output
23	OUT7	Channel 7 power output
24	OUT7	Channel 7 power output
25	OUT6	Channel 6 power output
26	OUT6	Channel 6 power output
27	OUT5	Channel 5 power output
28	OUT5	Channel 5 power output
29	OUT4	Channel 4 power output
30	OUT4	Channel 4 power output
31	OUT3	Channel 3 power output
32	OUT3	Channel 3 power output
33	OUT2	Channel 2 power output
34	OUT2	Channel 2 power output
35	OUT1	Channel 1 power output
36	OUT1	Channel 1 power output
TAB	TAB	Exposed tab internally connected to V_{cc}, positive power supply voltage

3 Absolute maximum rating

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power supply voltage	-0.3	45	V
Vdd	Digital supply voltage	-0.3	6.5	V
V_{IN}	DC input pins, Id & output enable voltage	-0.3	+6.5	V
V_{FAULT}	Fault voltage	-0.3	+6.5	V
I_{GNDdd}	DC digital ground reverse current		-25	mA
I_{OUT}	Channel output current (continuous)		Internally limited	A
I_{GNDcc}	DC power ground reverse current		-250	mA
I_R	Reverse output current (per channel)		-5	A
I_{IN}	DC input pins, Id & output enable current	-10	+ 10	mA
I_{FAULT}	Fault current	-10	+ 10	mA
V_{ESD}	Electrostatic discharge with human body model (R = 1.5 KΩ; C = 100 pF)		2000	V
EAS	Single pulse avalanche energy per channel not simultaneously		300	mJ
PTOT	Power dissipation at Tc = 25 °C		Internally limited(1)	W
TJ	Junction operating temperature		Internally limited(1)	°C
T_{STG}	Storage temperature		-55 to 150	°C
V_{ISO}	Dielectric isolation voltage		TBD	V_{RMS}

1. Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operation of protection functions may reduce the IC lifetime.

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction-to-case(1)	1.3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient	TBD	

1. For each channel

5 Electrical characteristics

(10.5 V < V_{CC} < 36 V; -25 °C < T_J < 125 °C, unless otherwise specified.)

Table 4. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{cc(under)_{THON}}$	V_{cc} undervoltage turn-ON threshold			9.5	10.5	V
$V_{cc(under)_{THOFF}}$	V_{cc} undervoltage turn-OFF threshold			9		V
$V_{cc(hys)}$	V_{cc} undervoltage hysteresis		0.4	0.5		V
V_{cclamp}	Clamp on V_{cc} pin	I_{clamp} = 20 mA	45	50	52	V
$R_{DS(ON)}$	On-state resistance (1)	I_{OUT} = 0.5 A, T_J = 25 °C I_{OUT} = 0.5 A		0.1	TBD 0.2	Ω Ω
Rpd	Output pull-down resistor			210		kΩ
Icc	Power supply current	All channels in OFF state All channels in ON state		5.5 10	TBD TBD	mA mA
I_{LGND}	Ground disconnection output current				500	µA
$V_{OUT(OFF)}$	Off-state output voltage	Channel OFF and I_{OUT} = 0 A			3	V
$I_{OUT(OFF)}$	Off-state output current	Channel OFF and V_{OUT} = 0 V			5	µA

1. See *Figure 3.*

Table 5. Digital supply voltage

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{dd(under)}$	Vdd undervoltage protection turn-OFF threshold		2.8	2.9	3	V
$V_{dd(hys)}$	Vdd undervoltage hysteresis		TBD	0.1		V
I_{dd}	Vdd supply current	Input channel with a steady logic level		5	TBD	mA

Table 6. Diagnostic pin and output protection function

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{FAULT}$ pin open drain voltage output low	I_{FAULT} = 10 mA			0.4	V
I_{LFAULT}	$\overline{FAULT}$ output leakage current	V_{FAULT} = 5 V		1	2	µA
I_{PEAK}	Maximum DC output current (1)			1.4		A
I_{LIM}	Short-circuit current limitation	R_{LOAD} = 0 Ω	0.7	1.1	1.7	A
H_{yst}	I_{LIM} tracking limits	R_{LOAD} = 0 Ω		0.3		A
T_{JSD}	Junction shutdown temperature		150	170		°C
T_{JR}	Junction reset temperature			150		°C
T_{HIST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	145	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis		TBD	20		°C
V_{demag}	Output voltage at turn-OFF	I_{OUT} = 0.5 A; I_{LOAD} > = 1 mH	Vcc-45	Vcc-50	Vcc-52	V

1. Current level from open load to short-circuit until thermal intervention.

Table 7. Power switching characteristics (V_{CC} = 24 V; -25 °C < T_J < 125 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-ON voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5.6	-	V/µs
dV/dt(OFF)	Turn-OFF voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω		2.81		V/µs
$t_{d(ON)DCM}$	Turn-ON delay time(1) in DCM mode	I_{OUT} = 0.5 A, resistive load 48 Ω		17		µs
$t_{d(OFF)DCM}$	Turn-OFF delay time (1) in DCM mode	I_{OUT} = 0.5 A, resistive load 48 Ω		22		µs
$t_{d(ON)SCM}$	Turn-ON delay time (1) in SCM mode	I_{OUT} = 0.5 A, resistive load 48 Ω		17		µs
$t_{d(OFF)SCM}$	Turn-OFF delay time (1) in SCM mode	I_{OUT} = 0.5 A, resistive load 48 Ω		22		µs
t_f	Fall time (1)	I_{OUT} = 0.5 A, resistive load		5		µs
t_r	Rise time (1)	I_{OUT} = 0.5 A, resistive load		5		µs

1. See *Figure 4*, *Figure 5*, and *Figure 6*.

Figure 3. $R_{DS(on)}$ measurement

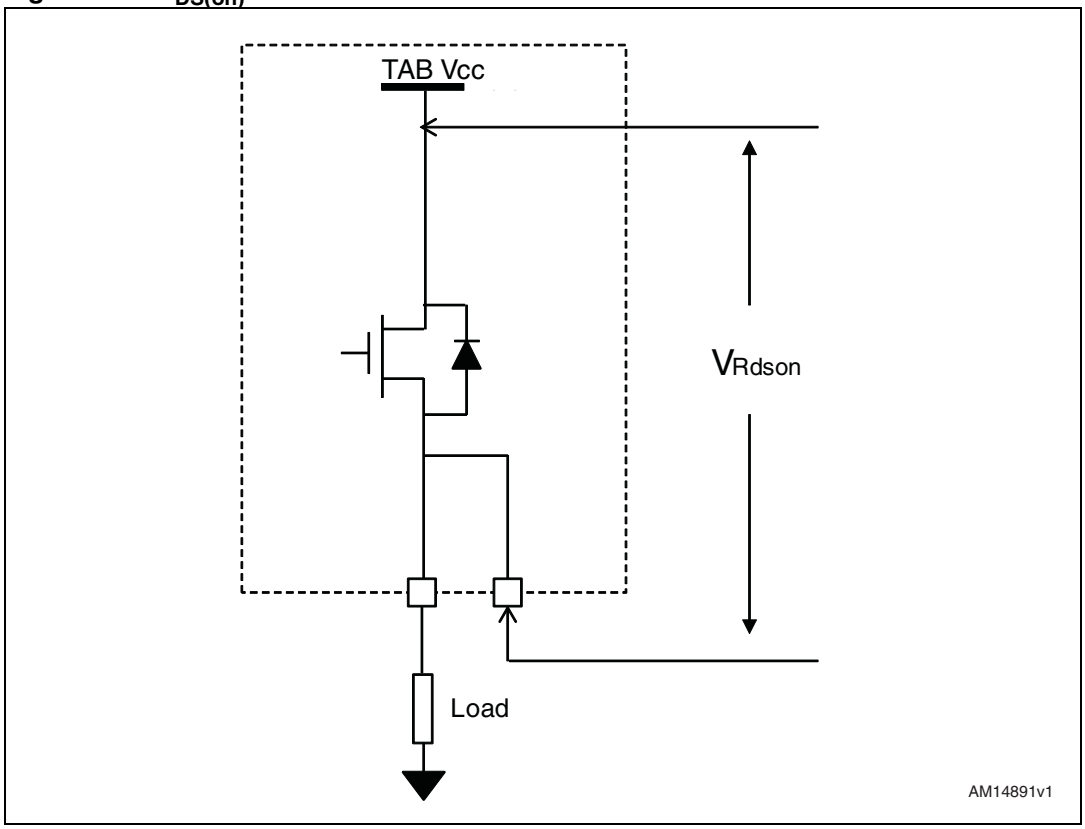


Figure 4. dV/dT

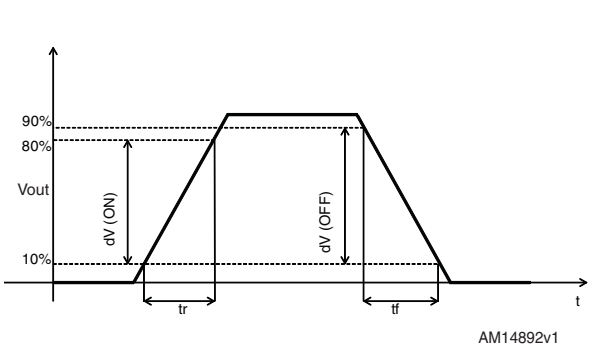


Figure 5. td(ON)-td(OFF) synchronous mode

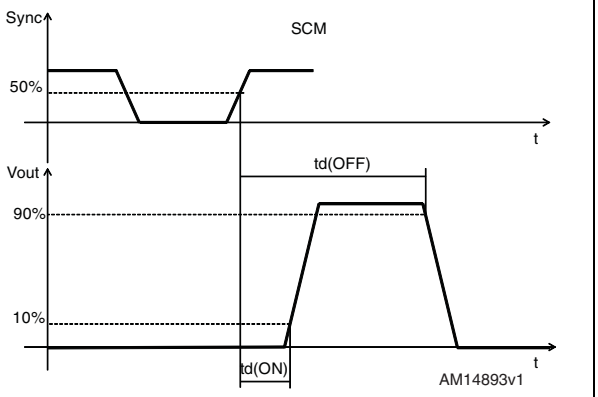


Figure 6. td(ON)-td(OFF) direct control mode

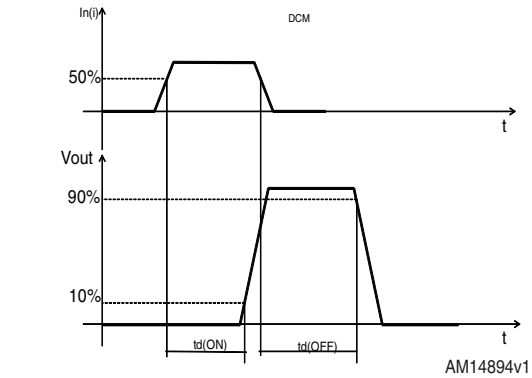


Table 8. Logic input and output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Logic input, $\overline{LOAD}$ and OUT_EN low level voltage		-0.3		0.3 x Vdd	V
V_{IH}	Logic input, $\overline{LOAD}$ and OUT_EN high level voltage		0.7 x Vdd		Vdd+0.3	V
$V_{I(HYST)}$	Logic input, $\overline{LOAD}$ and OUT_EN hysteresis voltage	Vdd = 5 V		100		mV
I_{IN}	Logic input, $\overline{LOAD}$ and OUT_EN current	V_{IN} = 5 V	10			µA
t_{WM}	Power side watchdog time		272	320	368	µs

Table 9. Parallel interface timings (V_{dd} = 5 V; V_{cc}= 24 V; -25 °C < T_J < 125 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{su(SYNC)}$	$\overline{SYNC}$ setup time	Sync. control mode	80			ns
$t_{h(SYNC)}$	$\overline{SYNC}$ hold time	Sync. control mode	80			ns
$t_{dis(SYNC)}$	$\overline{SYNC}$ disable time	Sync. control mode	10			µ
$t_{dis(DCM)}$	$\overline{SYNC}$ $\overline{LOAD}$ disable time	Direct control mode	80			ns
$t_{w(SYNC)}$	$\overline{SYNC}$ negative pulse width	Sync. control mode	20		195	µs
$t_{su(LOAD)}$	$\overline{LOAD}$ setup time	Sync. control mode	80			ns
$t_{h(LOAD)}$	$\overline{LOAD}$ hold time	Sync. control mode	400			ns
$t_{w(LOAD)}$	$\overline{LOAD}$ pulse width	Sync. control mode	240			ns
$t_{su(IN)}$	Input setup time		80			ns
$t_{h(IN)}$	Input hold time		10			ns
$t_{w(IN)}$	Input pulse width	Sync. control mode	160			ns
		Direct control mode	20			µs
t_{INLD}	IN to $\overline{LOAD}$ time	Direct control mode From IN variation to $\overline{LOAD}$ falling edge.	80			ns
t_{LDIN}	$\overline{LOAD}$ to IN time	Direct control mode. From $\overline{LOAD}$ falling edge to IN variation.	400			ns
$t_{w(OUT\_EN)}$	OUT_EN pulse width		150			ns
$t_{p(OUT\_EN)}$	OUT_EN propagation Delay				TBD	µs
$t_{jitter(SCM)}$	Jitter on single channel	Sync. mode			6	µs
$f_{refresh}$	Refresh delay		13.5	15	16.7	kHz

Table 10. Insulation and safety-related specifications

Symbol	Parameter	Condition	Value	Unit
CLR	Clearance (*) (minimum external air gap)	Measured from input terminals to output terminals, the shortest distance through air	TBD	mm
CPG	Creepage (*) (minimum external tracking)	Measured from input terminals to output terminals, the shortest distance path along body	TBD	mm
	Isolation group	Material group (DIN VDE 0110, 1/89, *Table 1.*)	III	

Table 11. IEC 60747-5-2 insulation characteristics

Symbol	Parameter	Test condition	Characteristic	Unit
	Installation classification (EN 60664-1, *Table 1*) (1)(2)			
	For rated mains voltage = 50 V RMS		I–IV	
	For rated mains voltage = 100 V RMS		I–III	
	Pollution degree (EN 60664-1)		2	
V_{IORM}	Maximum working insulation voltage		60	V_{PEAK}
V_{ini}	Input to output test voltage (3)	t_{ini} < 5 s	1644	V_{PEAK}
		Partial discharge < 5 pC		
V_p		t_m = 1 s	1315	V_{PEAK}
		Partial discharge < 5 pC		
V_{IOTM}	Transient overvoltage (3) (highest allowable overvoltage)	t_{ini} = 60 s	3500	V_{PEAK}
R_{IO}	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω

1. These ratings refer to reinforced insulation. If only basic insulation is needed, the installation categories of each mains voltage level can be scaled up one level.
2. For three-phase systems the values in the table refer to the line-to-neutral voltage.
3. Type and sample tests. A 3563 V DC test with TBD s duration is performed at production level.

Table 12. Device immunity specifications

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DV_{ISO}/dt	Common mode transient immunity	DV_{ISO} = 600V	-25		25	V/ns
BIM	Magnetic field immunity	IEC61000-4-8	TBD			mT
HF_I	Radiated immunity	According to IEC61000-4-3	10			V/m

6 Functional description

6.1 Parallel interface

The Smart parallel interface built into the ISO8200B offers three interfacing signals, which are easily manageable from a microcontroller.

The $\overline{\text{LOAD}}$ signal enables the input buffer to store the value of the channel inputs.

The $\overline{\text{SYNC}}$ signal copies the input buffer value into the transmission buffer and manages the synchronization between the low voltage side and the channel outputs on the isolated side.

The OUT_EN signal enables the channel outputs.

An internal refresh signal updates the configuration of the channel outputs with a $f_{refresh}$ frequency. This signal can be disabled forcing low the $\overline{\text{SYNC}}$ input when $\overline{\text{LOAD}}$ is high.

Managing $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ pins in direct control mode (DCM) or synchronous control mode (SCM) can be implemented.

The operation of these two signals is described by the following table:

Table 13. Interface signal operation (general)

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low (1)	The outputs are disabled (turned off).
High	High	High	The outputs are left unchanged.
Low	High	High	The input buffer is enabled. The outputs are left unchanged.
High	Low	High	The internal refresh signal is disabled. The transmission buffer is updated. The outputs are left unchanged.
Don't care		High	The outputs are updated according to current transmission buffer value.
Low	Low	High	The device operates in direct control mode as described in the respective paragraph.

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

6.1.1 Input signals (IN1 to IN8)

Inputs from IN1 to IN8 are the driving signals of the corresponding OUT1 to OUT8 outputs. The present data are directly loaded on related outputs if $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are low (DCM operation) or stored into input buffer when $\overline{\text{LOAD}}$ is low and SYNC is high.

6.1.2 Load input data ($\overline{\text{LOAD}}$)

The input is active low; it stores the present data of IN1 to IN8 into the input buffer.

6.1.3 Output synchronization ($\overline{SYNC}$)

The input is active low; it enables the ISO8200B transmission buffer to load the present data of the input buffer and manages the transmission between the two isolated sides of the device.

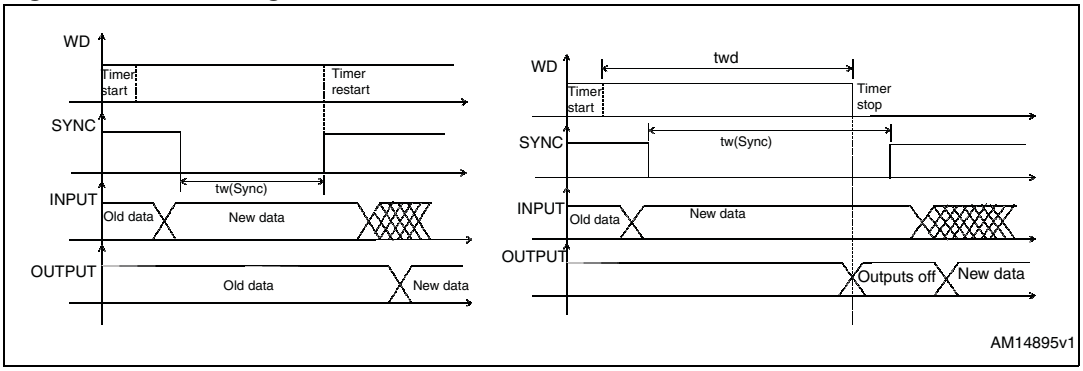
6.1.4 Watchdog

The isolated side of the device provides a watchdog function in order to guarantee a safe condition when Vdd supply voltage is missing.

If the logic side does not update the output status within t_{WD}, all the outputs are disabled until a new update request is received.

The refresh signal is also considered a valid update signal, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g. MCU freezing).

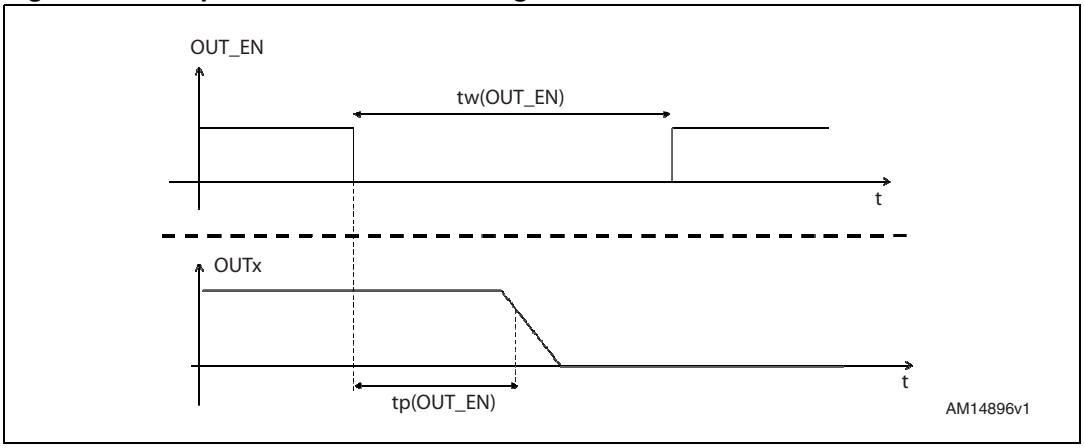
Figure 7. Watchdog behavior



6.1.5 Output enable (OUT_EN)

This pin provides a fast way to disable all the outputs simultaneously. When the OUT_EN pin is driven low the outputs are disabled. To enable the output stage, it is then necessary to raise the OUT_EN pin. This timing execution is compatible with an external reset push from the operator, safety requirement, and permits in a PLC system, a microcontroller polling to obtain all internal information during a reset procedure.

Figure 8. Output channel enable timing



6.2 Direct control mode (DCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are driven by the same signal, the device operates in direct control mode (DCM).

In DCM the $\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$ signal operates as an active low input enable:

- when the signal is high, the current output configuration is kept regardless of the input values
- when the signal is low, each channel input directly drives the respective output

This operation mode can also be set by shorting both the signals to the digital ground; in this case the channel outputs are always directly driven by the inputs except when OUT_EN is low (outputs disabled).

Table 14. Interface signal operation in direct control mode

$\overline{\text{SYNC}}$ / $\overline{\text{LOAD}}$	OUT_EN	Device behavior
Don't care	Low(1)	The outputs are disabled (turned off).
High	High	The outputs are left unchanged.
Low	High	The channel inputs drive the outputs.

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

Figure 9. Direct control mode IC configuration

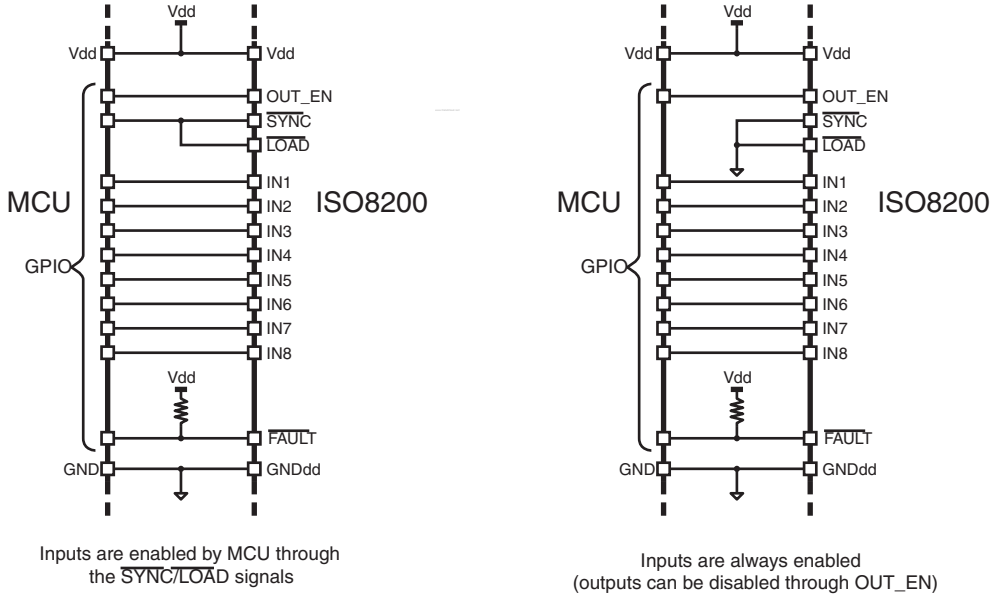
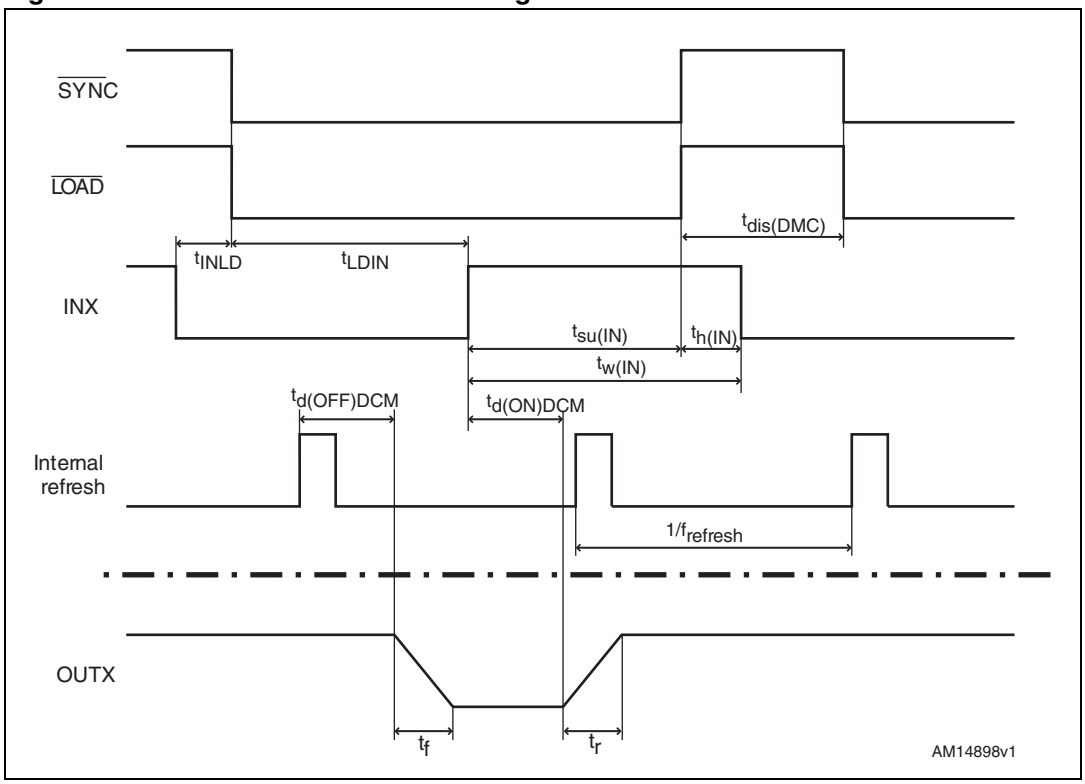


Figure 10. Direct control mode time diagram



6.3 Synchronous control mode (SCM)

When $\overline{\text{SYNC}}$ and $\overline{\text{LOAD}}$ inputs are independently driven, the device can operate in synchronous control mode (SCM). The SCM is used to reduce the jittering of the outputs and to drive all the outputs of different devices at the same time.

In SCM the $\overline{\text{LOAD}}$ signal is forced low in order to update the input buffer while the $\overline{\text{SYNC}}$ signal is high. After that, the $\overline{\text{LOAD}}$ signal is raised and the $\overline{\text{SYNC}}$ one is forced low for at least $t_{SYNC(SCM)}$. During this period, the internal refresh is disabled and any pending transmission between the low voltage and the isolated side is completed. When the $\overline{\text{SYNC}}$ signal is raised the channel output configuration is changed according to the one stored in the input.

If the $t_{SYNC(SCM)}$ limit is met, the maximum jitter of the channel outputs is t_{jitter}(SCM).

If more devices share the same SYNC signal, all device outputs change simultaneously with a maximum jitter related to maximum delay and maximum jitter for single devices.

Table 15. Interface signal operation in synchronous control mode

$\overline{\text{LOAD}}$	$\overline{\text{SYNC}}$	OUT_EN	Device behavior
Don't care	Don't care	Low (1)	The outputs are disabled (turned off).
High	High	High	The outputs are left unchanged.
Low	High	High	The input buffer is enabled. The outputs are left unchanged.
High	Low	High	The internal refresh signal is disabled. The transmission buffer is updated. The outputs are left unchanged.
High	Rising edge	High	The outputs are updated according to the current transmission buffer value.
Low	Low	High	Should be avoided. (DCM operation only)

1. The outputs are turned off on OUT_EN falling edge and they are kept disabled as long as it is low.

Figure 11. Synchronous control mode IC configuration

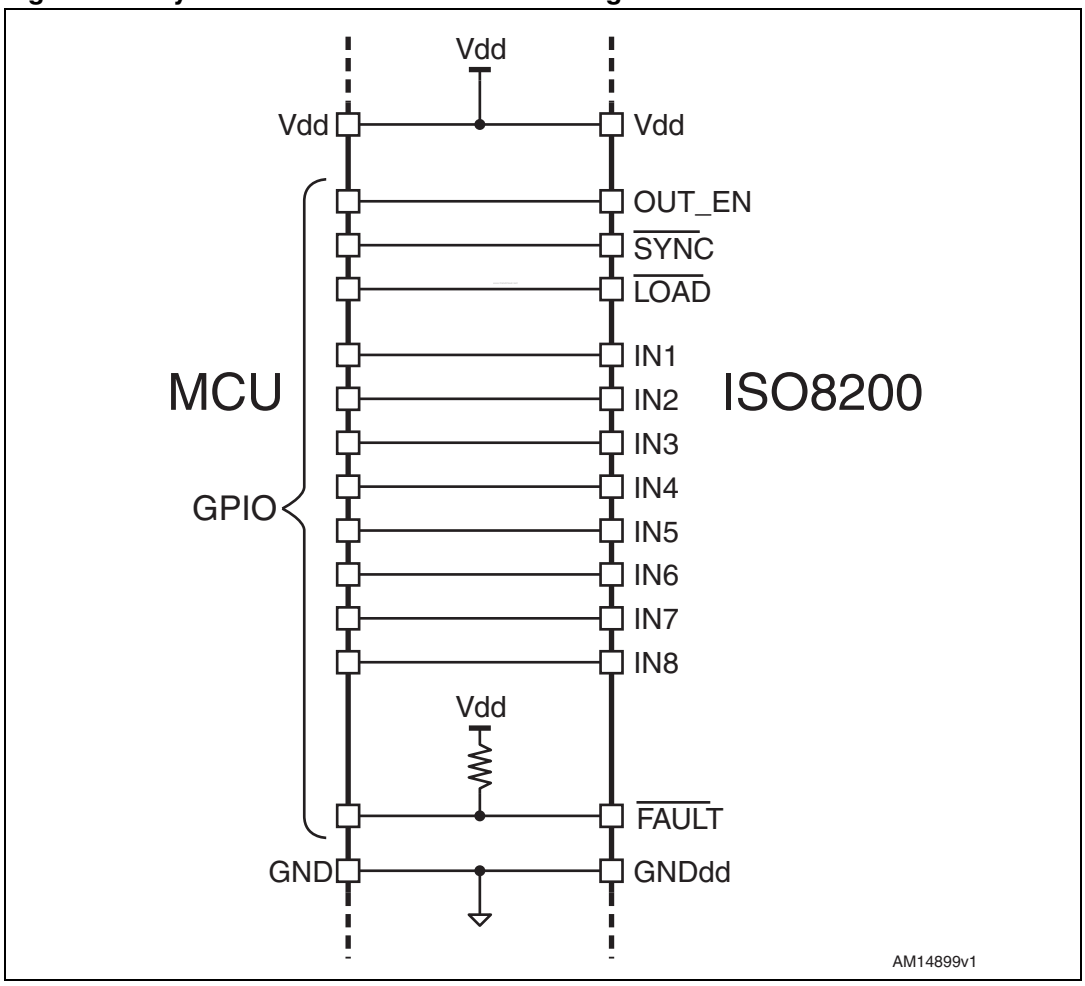


Figure 12. Synchronous control mode timing diagram

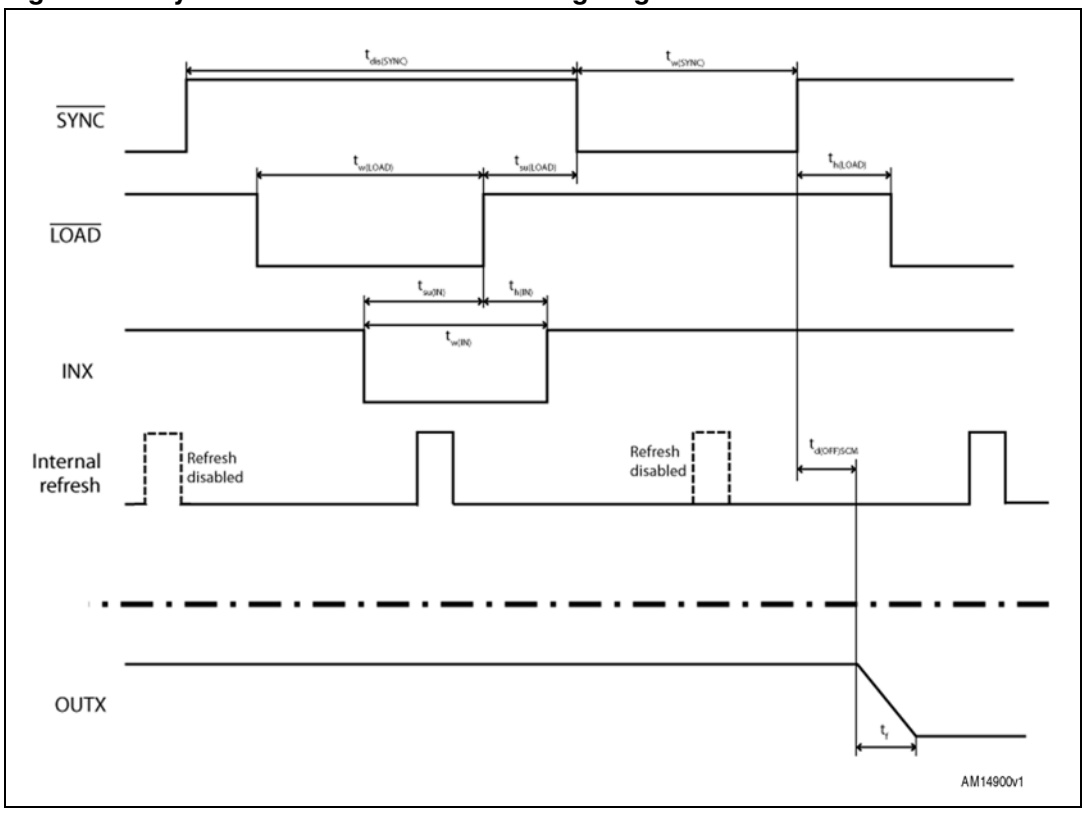
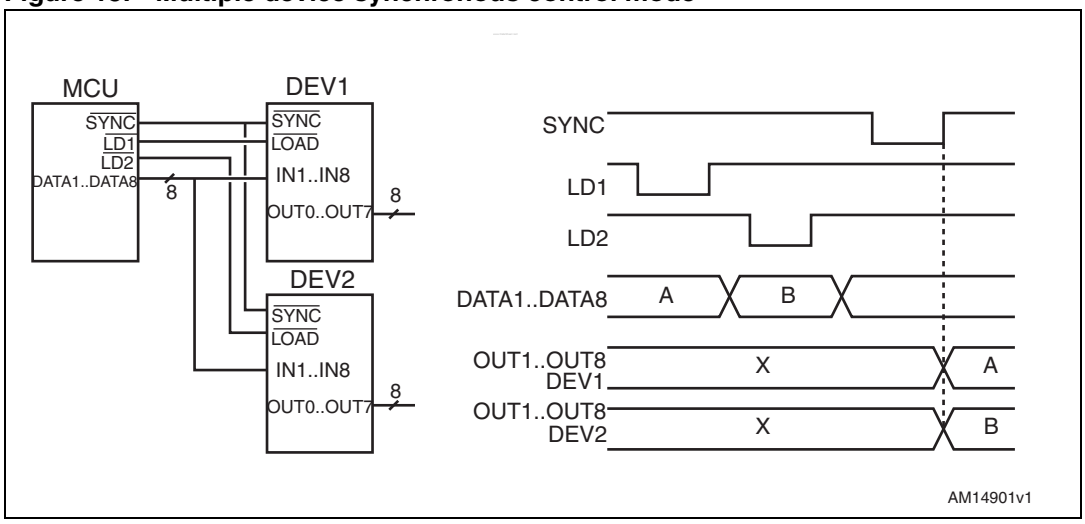


Figure 13. Multiple device synchronous control mode



6.4 Fault indication

The $\overline{\text{FAULT}}$ pin is an active low open drain output indicating fault conditions. This pin is activated when at least one of the following conditions occurs:

- Junction overtemperature of one or more channels ($T_J > T_{TJSD}$);
- Communication error.

6.4.1 Junction overtemperature and case overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated sides.

In SCM operation, when the $\overline{\text{LOAD}}$ signal is high and the $\overline{\text{SYNC}}$ one is low, the communication is disabled. In this case the thermal status of the device cannot be updated and the $\overline{\text{FAULT}}$ indication maybe be different from the current status.

In any case, the thermal protection of the channel outputs are always operative.

Figure 14. Thermal status update (DCM)

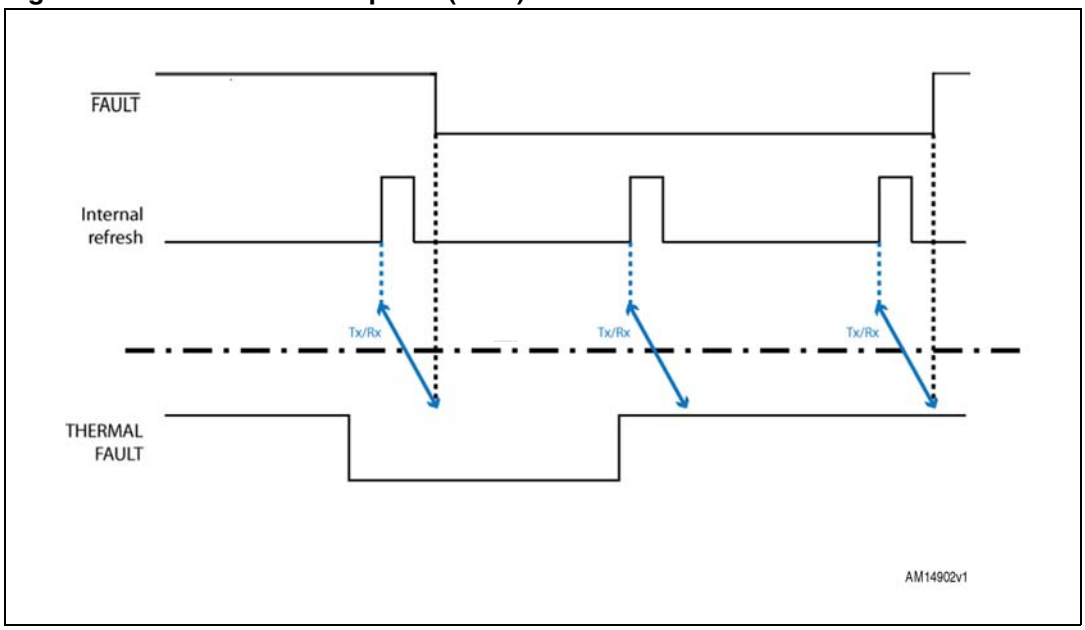
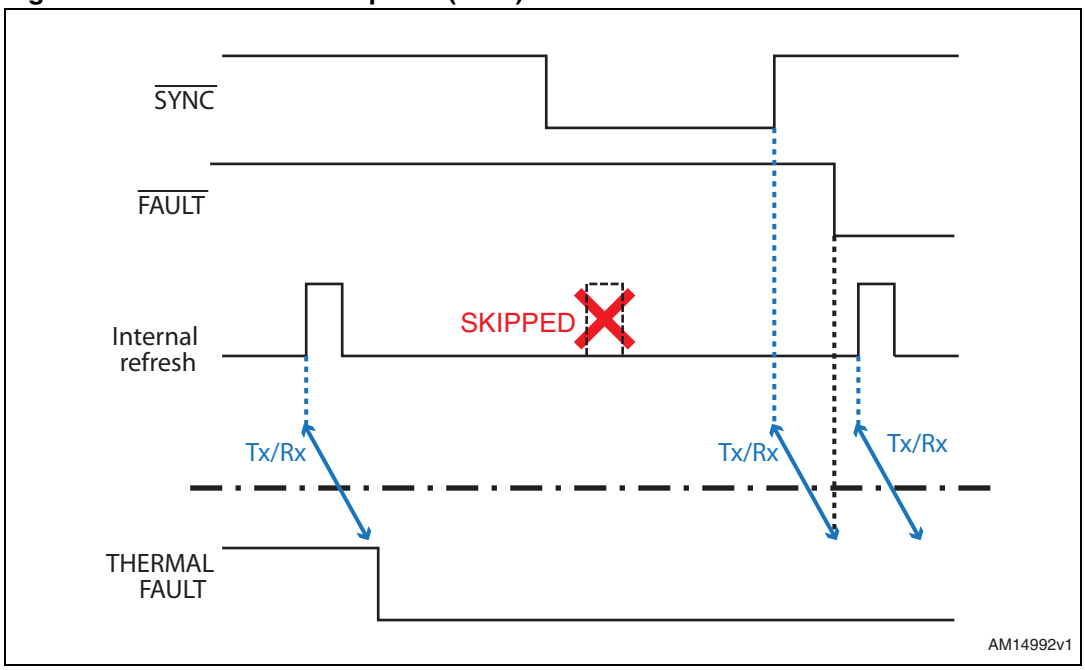


Figure 15. Thermal status update (SCM)



7 Power section

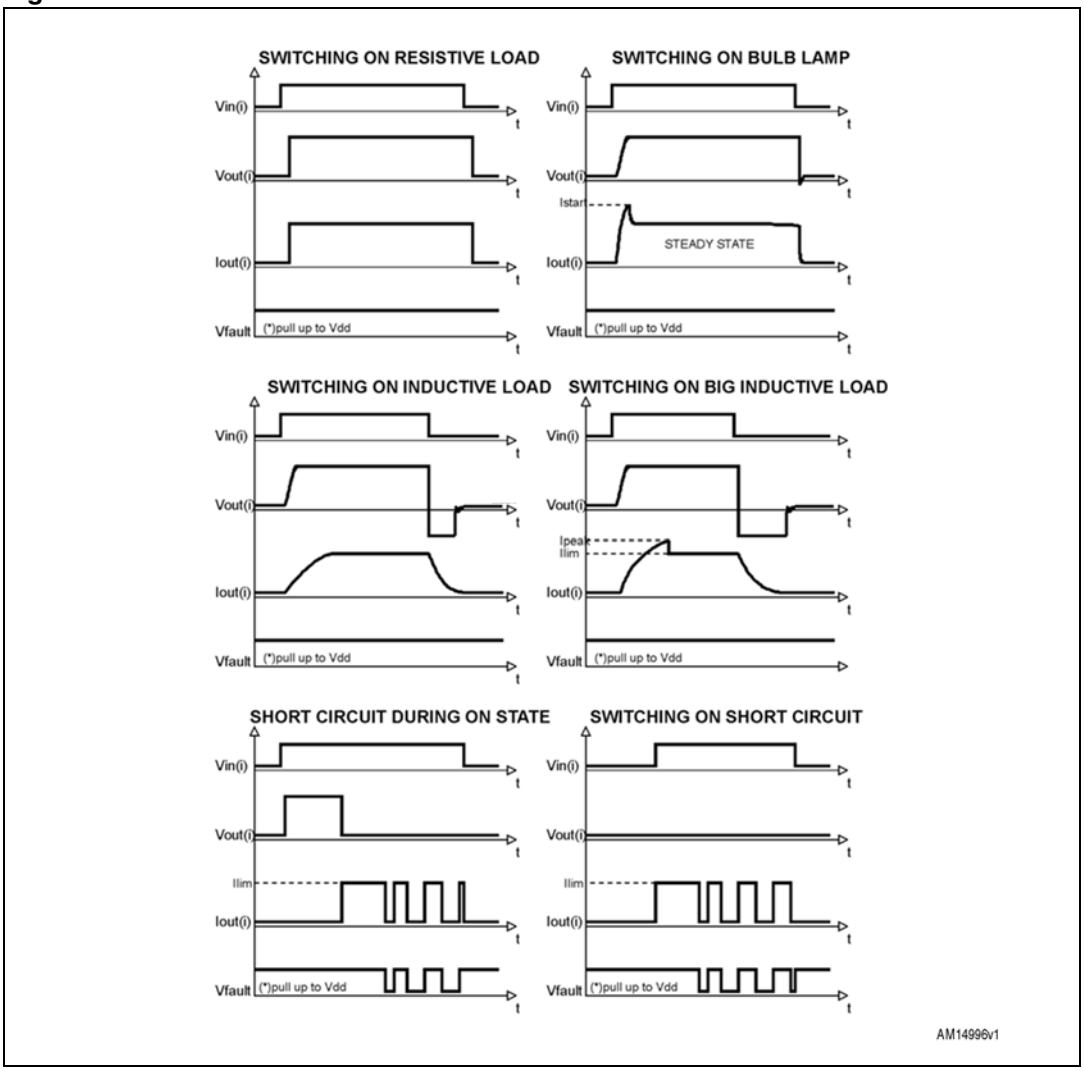
7.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value, which is higher than a fixed threshold.

When this condition is verified the gate voltage is modulated to avoid output current increasing over the limitation value.

Figure 16 shows typical output current waveforms with different load conditions.

Figure 16. Current limitation with different load conditions



7.2 Thermal protection

The device is protected against overheating due to overload conditions. During the driving period, if the output is overloaded, the device suffers two different thermal stresses, the former related to the junction, and the latter related to the case.

The two faults have different trigger thresholds: the junction protection threshold is higher than the case protection one; generally the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold. This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated and the output is switched off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

Figure 17 shows the thermal protection behavior, while *Figure 18* reports typical temperature trends and output vs. input state.

Figure 17. Thermal protection flowchart

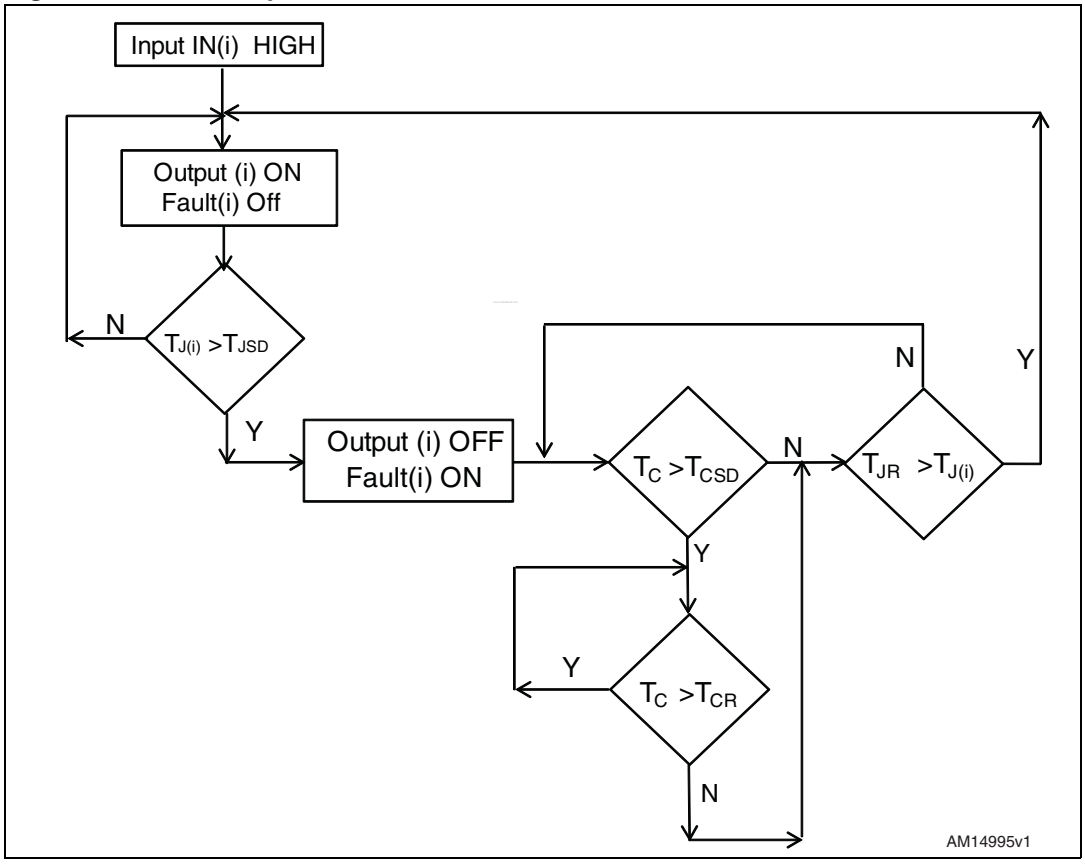
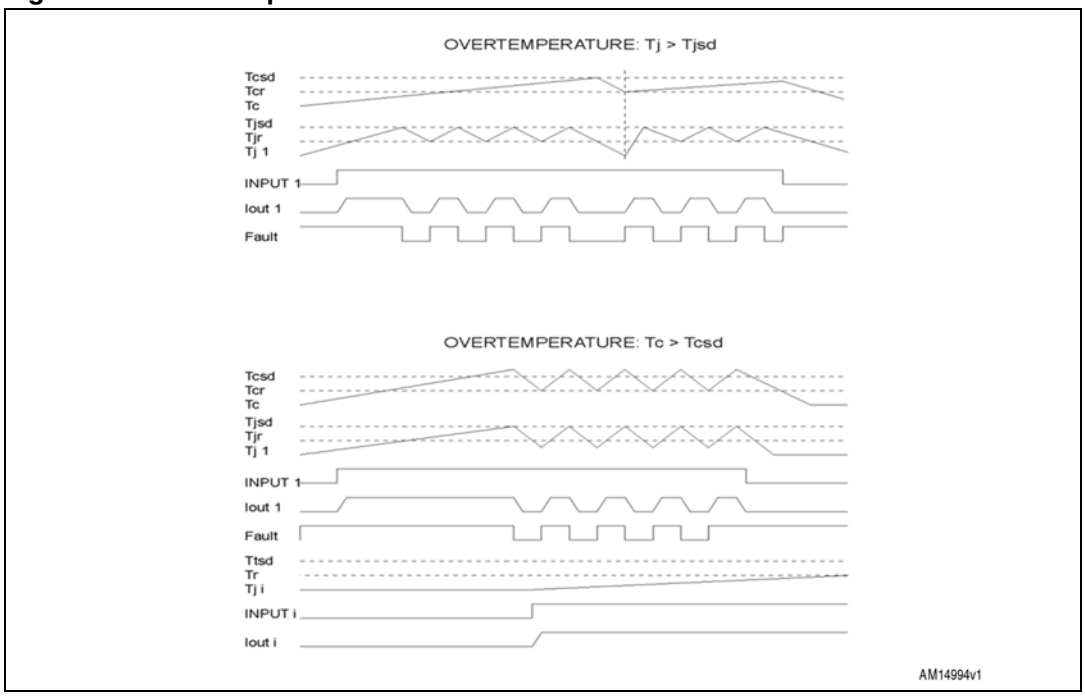


Figure 18. Thermal protection

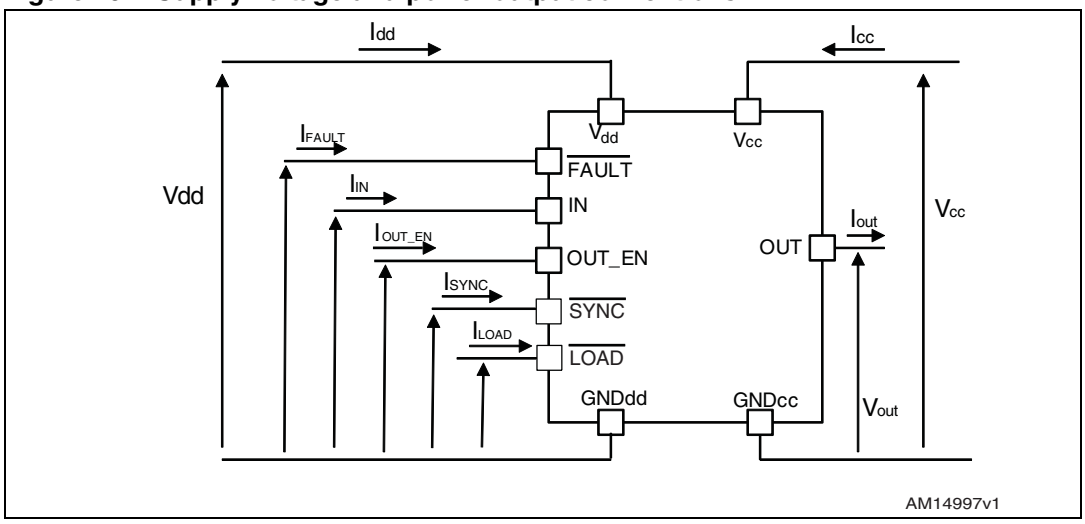


8 Conventions

8.1 Supply voltage and power output conventions

Figure 19, shows the convention used in this paper for voltage and current usage.

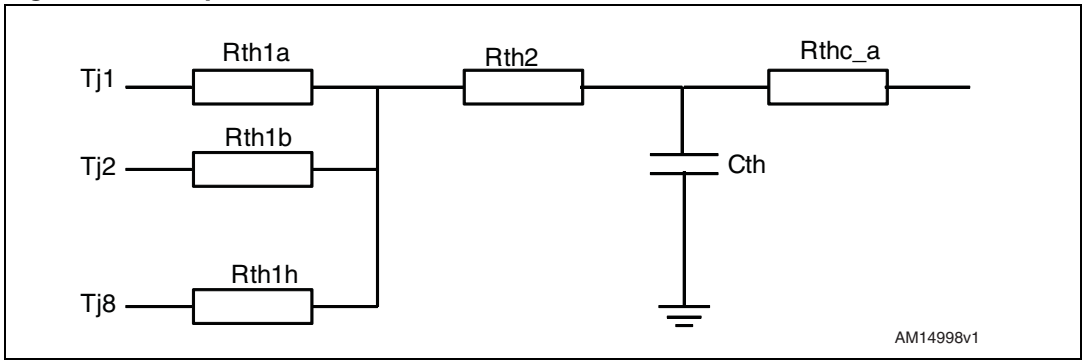
Figure 19. Supply voltage and power output conventions



9 Thermal information

9.1 Thermal impedance

Figure 20. Simplified thermal model



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 16. PowerSO-36 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.60
a1	0.10		0.30
a2			3.30
a3	0		0.10
b	0.22		0.38
c	0.23		0.32
D(1)	9.40		9.80
E	13.90		14.50
E1(1)	10.90		11.10
E2			2.90
E3	5.8		6.2
e		0.65	
e3		11.05	
G	0		0.10
H	15.50		15.90
h			1.10
L	0.80		1.10
N			10°
S	0°		8°

Figure 21. PowerSO-36 mechanical drawing

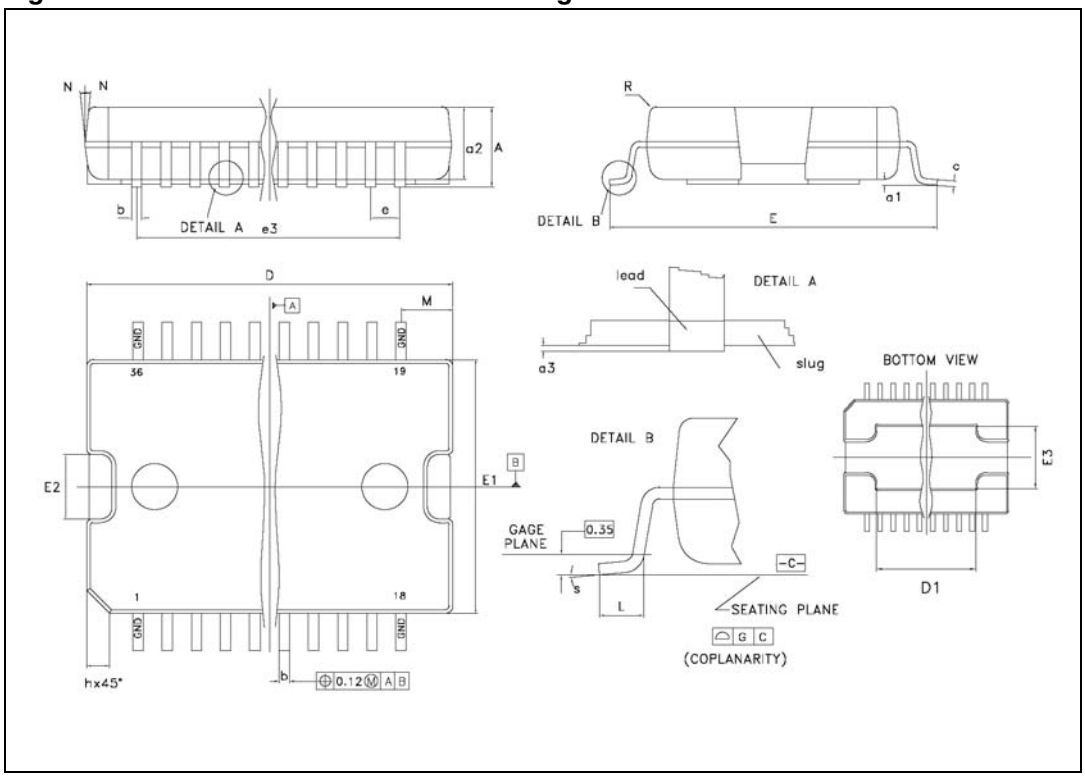


Figure 22. Footprint recommended data

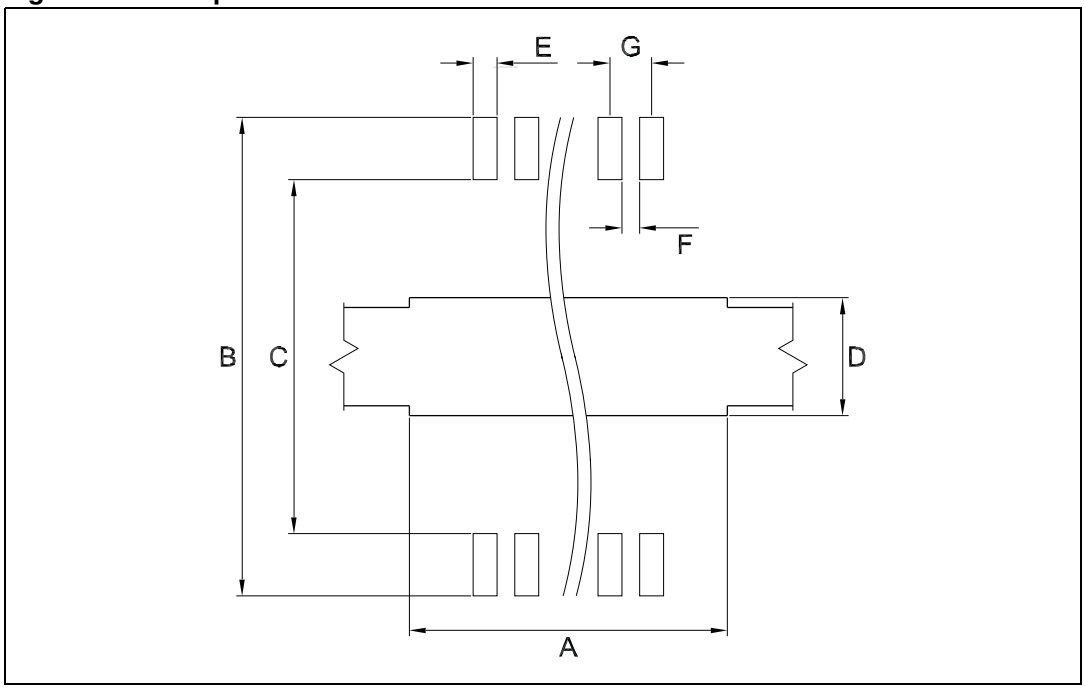


Table 17. Footprint data

Dim.	mm
A	9.5
B	14.7-15.0
C	12.5-12.7
D	6.3
E	0.46
F	0.27
G	0.65

11 Ordering information

Table 18. Ordering information

Order code	Package	Packaging
ISO8200B	PowerSO-36	Tube
ISO8200BTR	PowerSO-36	Tape and reel

12 Revision history

Table 19. Document revision history

Date	Revision	Changes
19-Oct-2012	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com