ISP1103

Universal Serial Bus transceiver

Rev. 01 — 4 October 1999 **Preliminary specification**

1. General description

The ISP1103 is a single-chip generic Universal Serial Bus (USB) transceiver that is fully compliant with the *Universal Serial Bus Specification Rev. 1.1*. It allows 3.3 V USB Application Specific ICs (ASICs) and Programmable Logic Devices (PLDs) to interface with the physical layer of the Universal Serial Bus. It supports transmitting and receiving serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates. It also supports the low-power single-ended input receiver interface in 'suspend' mode operation. The ISP1103 operates on a 3.3 V supply voltage.

The pin configuration conforms to the 'Serial Interface Engine' from the Universal Serial Bus Implementers Forum (USB-IF). The ISP1103 allows for both the 'USB-IF Standard Data Interface' and the 'Philips Encoded Data Interface'. The ISP1103 is fully pin compatible with the industry-standard Philips Semiconductors USB transceiver PDIUSBP11A.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 1.1*
- Supports full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) serial data rates
- Slew-rate controlled differential data driver
- Differential input receiver with wide common-mode range and very high data input sensitivity
- Stable RCV output during SE0 condition
- Two single-ended receivers with hysteresis
- Supports 'Philips Encoded Data Interface' and 'USB-IF Standard Data Interface'
- Low-power operation in 'suspend' mode
- Operates on a 3.3 V supply voltage
- Fully backward compatible with PDIUSBP11A
- Compatible with VHDL 'Serial Interface Engine' from USB Implementers Forum
- Higher than 8 kV ESD protection
- Full industrial operating temperature range −40 to +85 °C
- Available in SO14, SSOP14 and TSSOP14 packages.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1103D	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
ISP1103DB	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
ISP1103DH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

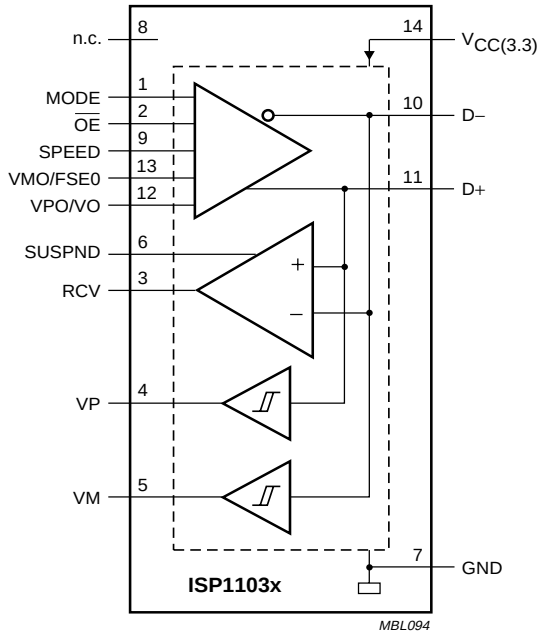


Fig 1. Functional diagram.

5. Pinning information

5.1 Pinning

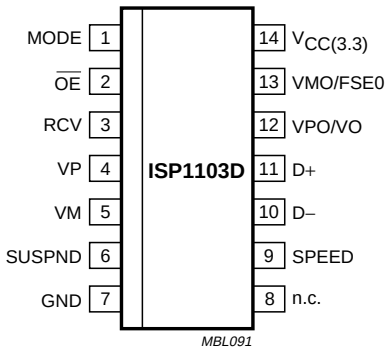


Fig 2. Pinning diagram SO14.

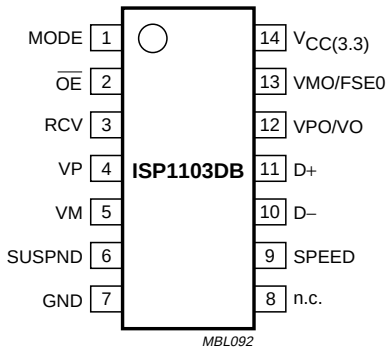


Fig 3. Pinning diagram SSOP14.

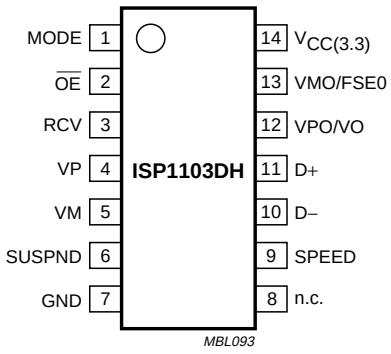


Fig 4. Pinning diagram TSSOP14.

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
MODE	1	I	driver interface selection input (Schmitt trigger): **LOW:** Philips Encoded Data Interface (pins VO, FSE0) **HIGH:** USB-IF Standard Data Interface (pins VPO, VMO); pulled HIGH by an internal pull-up transistor, if left floating
$\overline{OE}$	2	I	output enable input (Schmitt trigger, active LOW); enables the transceiver to transmit data on the bus
RCV	3	O	differential data receiver output (CMOS level); driven HIGH when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition
VP	4	O	single-ended D+ receiver output (CMOS level); used for external detection of single-ended zero (SE0), error conditions, speed of connected device
VM	5	O	single-ended D– receiver output (CMOS level); used for external detection of single-ended zero (SE0), error conditions, speed of connected device
SUSPND	6	I	suspend input (Schmitt trigger); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a HIGH level
GND	7	-	ground supply
n.c.	8	-	not connected
SPEED	9	I	speed selection input (Schmitt trigger); adjusts the slew rate of differential data outputs D+ and D– according to the transmission speed: **LOW:** low-speed (1.5 Mbit/s) **HIGH:** full-speed (12 Mbit/s)

Table 2: Pin description...*continued*

Symbol	Pin	Type	Description
D–	10	AI/O	negative USB data bus connection (analog, differential); for low-speed mode connect to pin $V_{CC(3.3)}$ via a 1.5 kΩ resistor
D+	11	AI/O	positive USB data bus connection (analog, differential); for full-speed mode connect to pin $V_{CC(3.3)}$ via a 1.5 kΩ resistor
VPO/VO	12	I	differential driver data input (Schmitt trigger); see Table 4
VMO/FSE0	13	I	differential driver data input (Schmitt trigger); see Table 4
$V_{CC(3.3)}$	14	-	supply voltage (3.0 to 3.6 V)

6. Functional description

6.1 Function selection

Table 3: Function table

SUSPND	$\overline{OE}$	D+/D–	RCV	VP/VM	Function
L	L	driving	active	active	normal driving (differential receiver active)
L	H	receiving [1]	active	active	receiving
H	L	driving	inactive [2]	active	driving during 'suspend' (differential receiver inactive)
H	H	high-Z [1]	inactive [2]	active	low-power state

[1] Signal levels on D+/D– are determined by other USB devices and external pull-up/down resistors.

[2] In 'suspend' mode (SUSPND = H) the differential receiver is inactive and output RCV is always HIGH. Out-of-suspend ('K') signalling is detected via the single-ended receivers VP and VM.

6.2 Operating functions

Table 4: Driving function ($\overline{OE}$ = L)

MODE	Interface type	VPO/VO	VMO/FSE0	Data
L	Philips Encoded Data Interface	L	L	differential logic 0
		L	H	SE0
		H	L	differential logic 1
		H	H	SE0
H	USB-IF Standard Data Interface	L	L	SE0
		L	H	differential logic 0
		H	L	differential logic 1
		H	H	illegal data

Table 5: Receiving function ($\overline{OE}$ = H)

D+/D–	RCV	VP	VM
differential logic 0	L	L	H
differential logic 1	H	H	L
SE0	RCV*	L	L

[1] RCV* denotes the signal level on output RCV just before SE0 state occurs. This level is kept stable during the SE0 period.

7. Limiting values

Table 6: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(3.3)}$	supply voltage			–0.5	+6.0	V
V_I	input voltage			–0.5	V_{CC} + 0.5	V
$I_{latchup}$	latchup current	$V_I < 0$ or $V_I > V_{CC}$		-	200	mA
V_{esd}	electrostatic discharge voltage	$I_{LI} < 1$ µA	[1]	-	±8000	V
T_{stg}	storage temperature			–60	+150	°C
P_{tot}	total power dissipation			-	<tbf>	W

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model).

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(3.3)}$	supply voltage		3.0	3.6	V
V_I	input voltage		0	5.5	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (D+/D–)		0	3.6	V
T_{amb}	operating ambient temperature		–40	+85	°C

8. Static characteristics

Table 8: Static characteristics: supply pins

$V_{CC} = V_{CC(3.3)}$; $V_{GND} = 0$ V; $T_{amb} = -40$ to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	operating supply current		-	<tbf>	-	mA
$I_{CC(susp)}$	suspend supply current		-	-	10	µA

Table 9: Static characteristics: digital pins

V_{CC} = $V_{CC(3.3)}$; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Schmitt trigger input levels						
$V_{th(LH)}$	positive-going threshold voltage		1.4	-	1.9	V
$V_{th(HL)}$	negative-going threshold voltage		0.9	-	1.5	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	-	-	0.4	V
		I_{OL} = 20 µA	-	-	0.1	V
V_{OH}	HIGH-level output voltage	I_{OL} = 3 mA	2.4	-	-	V
		I_{OL} = 20 µA	$V_{CC(3.3)}$ − 0.1	-	-	V
Leakage current						
I_{LI}	input leakage current		-	-	±1	µA

Table 10: Static characteristics: analog I/O pins (D+, D–) [1]

V_{CC} = $V_{CC(3.3)}$; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{DI}	differential input sensitivity	$\|V_{I(D+)} - V_{I(D-)}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{hys}	hysteresis voltage		0.4	-	0.7	V
Output levels						
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to $V_{CC(3.3)}$	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	2.8	-	$V_{CC(3.3)}$	V
Leakage current						
I_{LZ}	OFF-state leakage current		-	-	±10	µA
Capacitance						
C_{IN}	transceiver capacitance	pin to GND	-	-	20	pF
Resistance						
Z_{DRV}	driver output impedance [2]	steady-state drive	28	-	44	Ω
Z_{INP}	input impedance		10	-	-	MΩ
Termination						
V_{TERM}	termination voltage [3] for upstream port pull-up (R_{PU})		3.0 [4]	-	3.6	V

[1] D+ is the USB positive data pin; D– is the USB negative data pin.

[2] Includes external resistors of 22 Ω ±1% or 24 Ω ±1% on both D+ and D–.

[3] This voltage is available at pin $V_{CC(3.3)}$.

[4] In ‘suspend’ mode the minimum voltage is 2.9 V.

9. Dynamic characteristics

Table 11: Dynamic characteristics: analog I/O pins (D+, D–); full-speed mode [1]

V_{CC} = $V_{CC(3.3)}$; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on D+ to V_{TERM}.; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{FR}	rise time	C_L = 50 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 5	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 5	4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	[2]	90	-	111.1	%
V_{CRS}	output signal crossover voltage	[2] [3]	1.3	-	2.0	V
Driver timing						
t_{PLH}	propagation delay (VPO,VMO/FSE0 to D+,D–)	LOW-to-HIGH; see Figure 8	-	-	14	ns
t_{PHL}		HIGH-to-LOW; see Figure 8	-	-	14	ns
t_{PHZ}	3-state output disable time ($\overline{OE}$ to D+,D–)	HIGH-to-OFF; see Figure 6	-	-	6	ns
t_{PLZ}		LOW-to-OFF; see Figure 6	-	-	5	ns
t_{PZH}	3-state output enable time ($\overline{OE}$ to D+,D–)	OFF-to-HIGH; see Figure 6	-	-	14	ns
t_{PZL}		OFF-to-LOW; see Figure 6	-	-	15	ns
Receiver timing						
Differential receiver						
t_{PLH}	propagation delay (D+,D– to RCV)	LOW-to-HIGH; see Figure 7	-	-	8	ns
t_{PHL}		HIGH-to-LOW; see Figure 7	-	-	8	ns
Single-ended receiver						
t_{PLH}	propagation delay (D+,D– to VP,VM)	LOW-to-HIGH; see Figure 7	-	-	5	ns
t_{PHL}		HIGH-to-LOW; see Figure 7	-	-	8	ns

[1] Test circuit: see Figure 11.

[2] Excluding the first transition from Idle state.

[3] Characterized only, not tested. Limits guaranteed by design.

Table 12: Dynamic characteristics: analog I/O pins (D+, D–); low-speed mode [1]

V_{CC} = $V_{CC(3.3)}$; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on D– to V_{TERM}.; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{LR}	rise time	C_L = 200 to 600 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 5	75	-	300	ns
t_{LF}	fall time	C_L = 200 to 600 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 5	75	-	300	ns
LRFM	differential rise/fall time matching (t_{LR}/t_{LF})	[2]	85	-	118	%
V_{CRS}	output signal crossover voltage	[2] [3]	1.3	-	2.0	V

Table 12: Dynamic characteristics: analog I/O pins (D+, D–); low-speed mode [1] *...continued*

V_{CC} = $V_{CC(3.3)}$; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; C_L = 50 pF; R_{PU} = 1.5 kΩ on D– to V_{TERM}.; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver timing						
t_{PLH}	propagation delay (VPO/VO, VMO/FSE0 to D+,D–)	LOW-to-HIGH; see Figure 8	-	-	165	ns
t_{PHL}		HIGH-to-LOW; see Figure 8	-	-	145	ns
t_{PHZ}	3-state output disable time ($\overline{OE}$ to D+,D–)	HIGH-to-OFF; see Figure 6	-	-	6	ns
t_{PLZ}		LOW-to-OFF; see Figure 6	-	-	5	ns
t_{PZH}	3-state output enable time ($\overline{OE}$ to D+,D–)	OFF-to-HIGH; see Figure 6	-	-	100	ns
t_{PZL}		OFF-to-LOW; see Figure 6	-	-	100	ns
Receiver timing						
Differential receiver						
t_{PLH}	propagation delay (D+,D– to RCV)	LOW-to-HIGH; see Figure 7	-	-	9	ns
t_{PHL}		HIGH-to-LOW; see Figure 7	-	-	10	ns
Single-ended receiver						
t_{PLH}	propagation delay (D+,D– to VP,VM)	LOW-to-HIGH; see Figure 7	-	-	5	ns
t_{PHL}		HIGH-to-LOW; see Figure 7	-	-	8	ns

[1] Test circuit: see Figure 11.

[2] Excluding the first transition from Idle state.

[3] Characterized only, not tested. Limits guaranteed by design.

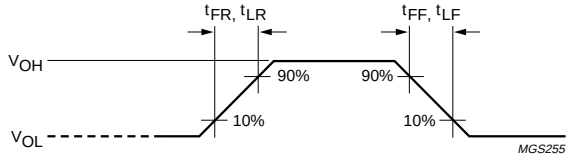


Fig 5. Rise and fall times.

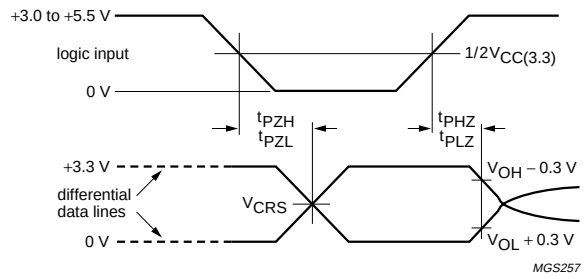


Fig 6. Timing of $\overline{OE}$ to D+, D-.

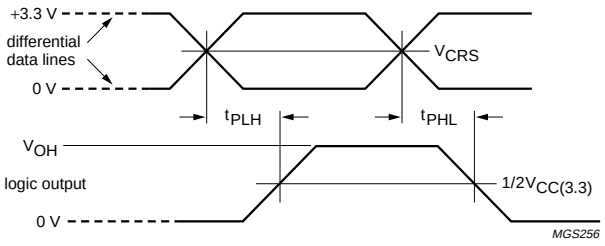


Fig 7. Timing of D+, D- to RCV, VP, VM.

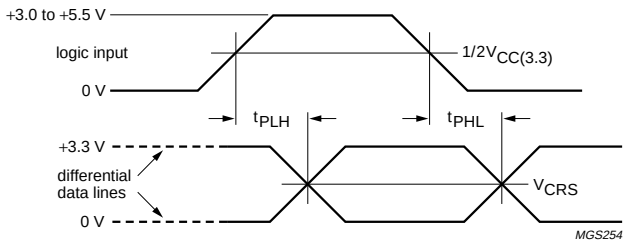
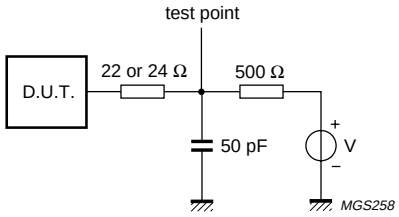


Fig 8. Timing of VPO/VO, VMO/FSE0 to D+, D-.

10. Test information



$V = 0$ V for t_{PZH}, t_{PHZ}

$V = V_{CC(3.3)}$ for t_{PZL}, t_{PLZ}

Fig 9. Load for enable and disable times.

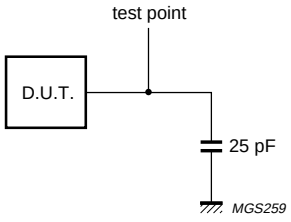
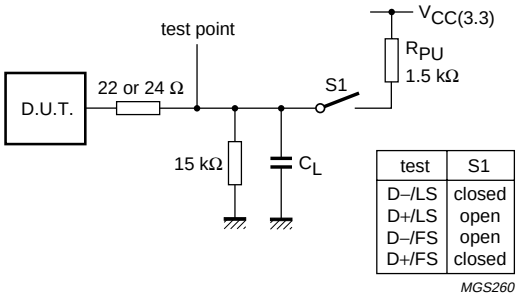


Fig 10. Load for VM, VP and RCV.



test	S1
D–/LS	closed
D+/LS	open
D–/FS	open
D+/FS	closed

Load capacitance:

C_L = 50 pF or 125 pF (full-speed mode, minimum or maximum timing)

C_L = 200 pF or 600 pF (low-speed mode, minimum or maximum timing).

Speed selection:

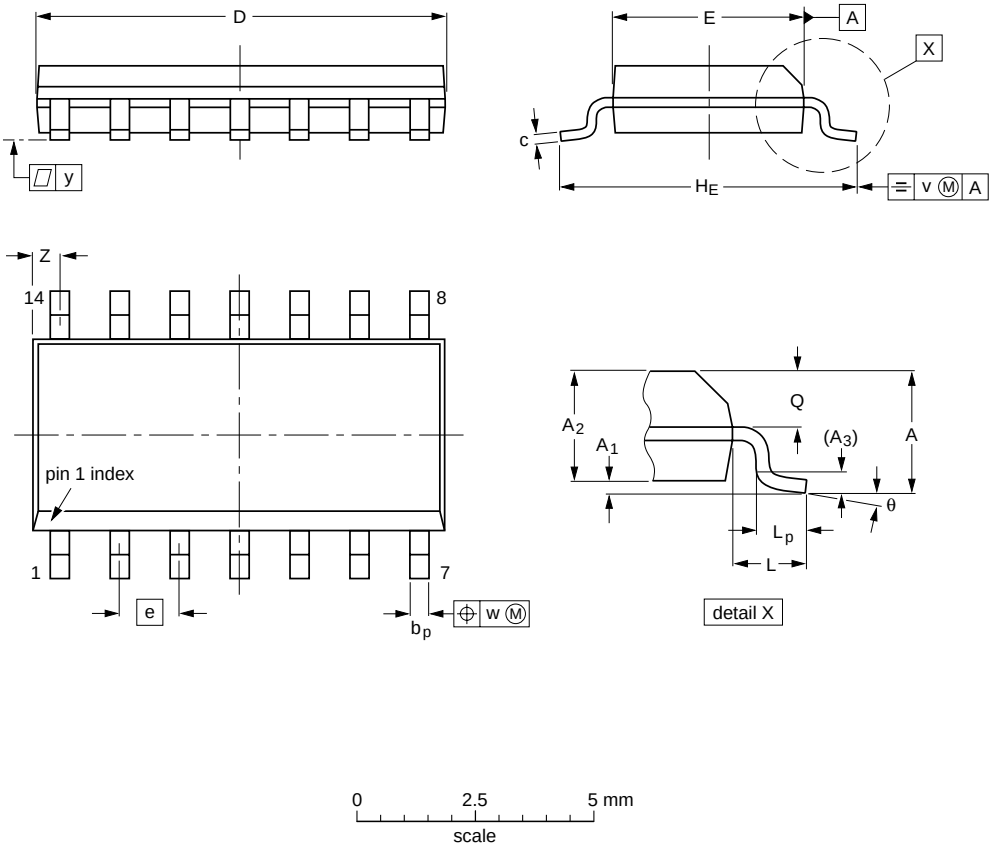
full-speed mode (FS): 1.5 kΩ pull-up resistor on D+

low-speed mode (LS): 1.5 kΩ pull-up resistor on D–.

Fig 11. Load for D+, D-.

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

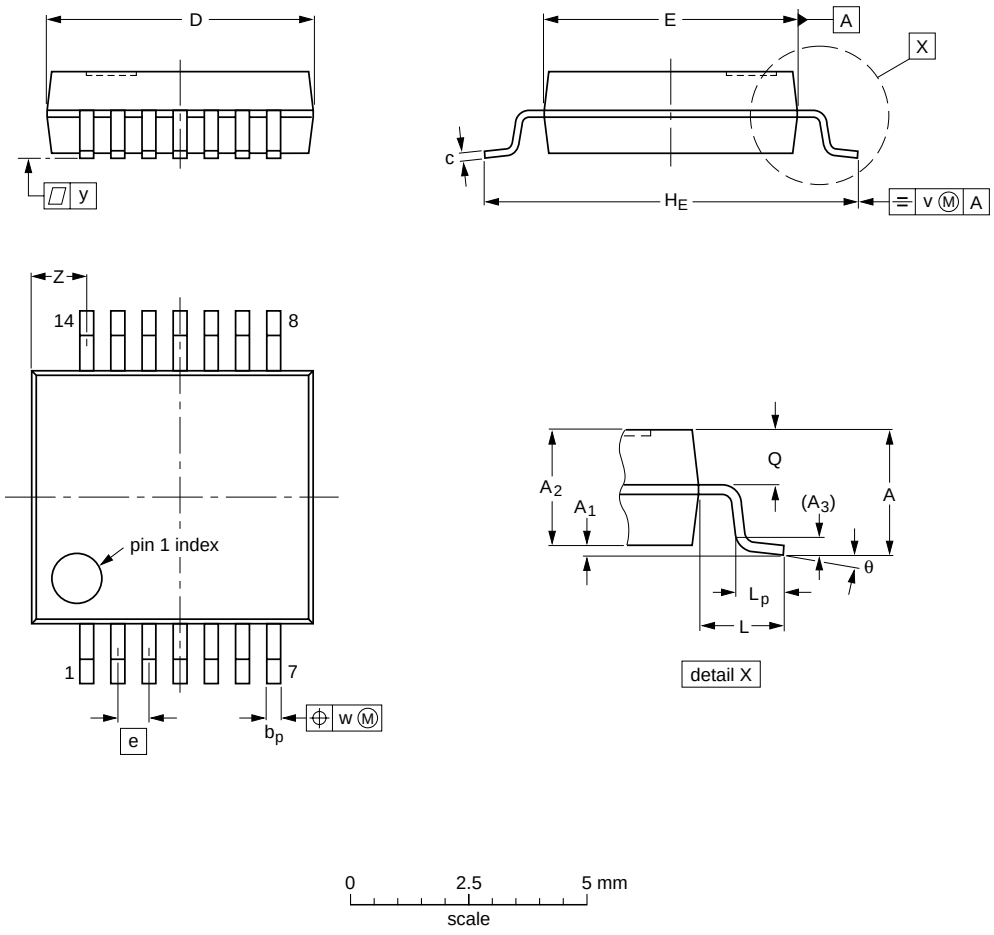
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Fig 12. SO14 package outline.

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

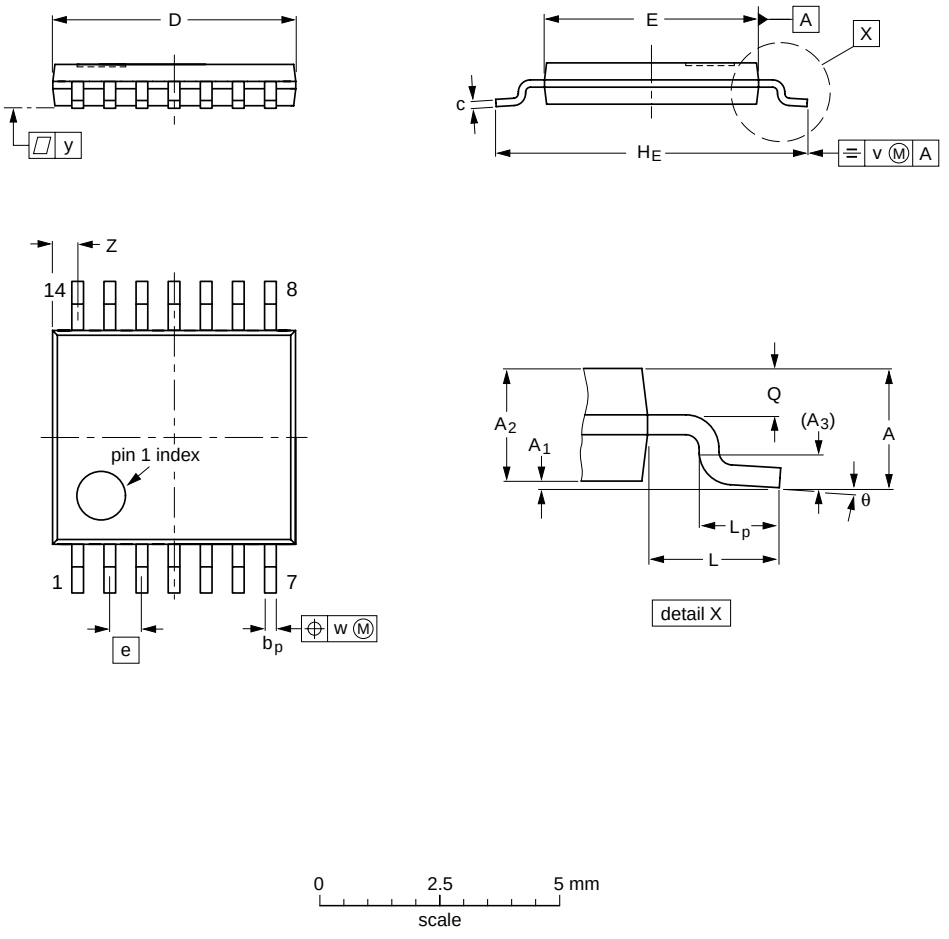
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				~~95-02-04~~ 96-01-18

Fig 13. SSOP14 package outline.

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~94-07-12~~ 95-04-04

Fig 14. TSSOP14 package outline.

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

12.5 Package related soldering information

Table 13: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow [1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable [2]	suitable
PLCC [3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [3] [4]	suitable
SSOP, TSSOP, VSO	not recommended [5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

13. Revision history

Table 14: Revision history

Rev	Date	CPCN	Description
01	**19991004**		**Preliminary specification; initial version.**

14. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

15. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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