

N-Channel MOSFET

Pb **Lead Free Package and Finish**

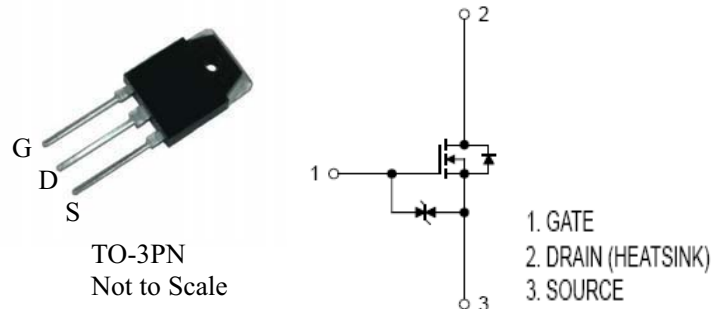
Applications:

- ATX Power
- LCD Panel Power

V _{DSS}	R _{DS(on)} (Typ)	I _D (Max)
950V	0.85Ω	11A

Features:

- RoHS Compliant & Halogen Free
- Low ON Resistance
- Low Gate Charge
- ESD Capability Improved



Ordering Information

Part Number	Package Type	Brand
ISW11N90A	TO-3PN	IPS

Absolute Maximum Ratings T_c= 25 °C unless otherwise specified

Symbol	Parameter	Maximum	Units
V _{DSS}	Drain-to-Source Voltage (NOTE *1)	950	V
I _D	Continuous Drain Current	11	A
I _{D@ 100 °C}	Continuous Drain Current	Figure3	
I _{DM}	Pulsed Drain Current, V _{GS@ 10V} (NOTE *2)	Figure6	
P _D	Power Dissipation	170	W
	Derating Factor above 25°C	1.36	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy;	300	mJ
VESD(GS)	Gate Source ESD Voltage(HBM,c=100pF,R=1.5K Ω)	6000	V
dv/dt	Peak Diode Recovery dv/dt (NOTE *3)	5.0	V/ns
T _L T _{PKG}	Maximum Temperature for Soldering Leads at 0.063in(1.6mm) from Case for 10 seconds Package Body for 10 seconds	300 260	°C
T _J and T _{STG}	Operation Junction and Storage Temperature Range	150, -55 to 150	°C

Caution: Stresses greater than those listed in "Absolute Maximum Ratings" Table may cause permanent damage to the device.

Thermal Resistance

Symbol	Parameter	Maximum	Units	Test Condition
R _{θJC}	Junction-to-Case	0.73	°C/W	Drain lead soldered to water cooled heatsink, PD ad-justed for a peak junction temperature of +150oC. 1 cubic foot chamber, free air.
R _{θJA}	Junction-to-Ambient	40		

Electrical Characteristics TJ= 25 °C unless otherwise specified:

OFF Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
V _{DSS}	Drain-to-Source Breakdown Voltage	950	--	--	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	--	0.5	--	V/°C	Reference to 25 °C , ID=250uA
I _{DS(off)}	Off-State Drain-to-Source Current	--	--	1.0	uA	V _{DS} = 950V, V _{GS} =0V, T _a = 25 °C
		--	--	250		V _{DS} =760V, V _{GS} = 0 V, T _a = 125 °C
I _{GSS(F)}	Gate-to-Source Forward Leakage	--	--	1.0	uA	V _{GS} =+20V
I _{GSS(R)}	Gate-to-Source Reverse Leakage	--	--	-1.0		V _{GS} =-20V

ON Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
R _{DS(ON)}	Drain-to-Source On-Resistance	--	0.85	1.3	Ω	V _{GS} =10V,I _D =4.5A (NOTE*4)
g _{fs}	Forward Transconductance	--	11	--	S	V _{DS} >2I _D *R _{DS(on)} _{max} I _D =11A (NOTE*4)
V _{GS(TH)}	Gate Threshold Voltage	2.0	--	4.0	V	V _{DS} = V _{GS} , I _D = 250μA

Dynamic Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
C _{iss}	Input Capacitance	--	2956	--	pF	V _{GS} =0V V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	--	206	--		
C _{rss}	Reverse Transfer Capacitance	--	18	--		
Q _g	Total Gate Charge	--	66	--	nC	V _{DD} =450V I _D =11A V _{gs} =10V
Q _{gs}	Gate-to-Source Charge	--	13	--		
Q _{gd}	Gate-to-Drain (“Miller”)Charge	--	25	--		

Resistive Switching Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
t _{d(ON)}	Turn-on Delay Time	--	18	--	ns	V _{DD} = 450V I _D =11A V _{GS} = 10V R _G =4.7Ω
trise	Rise Time	--	28	--		
t _{d(OFF)}	Turn-Off Delay Time	--	49	--		
t _{fall}	Fall Time	--	34	--		

Source-Drain Diode Characteristics						
Symbol	Parameter	Rating			Units	Test Conditions
		Min.	Typ.	Max.		
I_S	Continuous Source Current (Body Diode)	--	--	11	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	44	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	$I_S=11A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	265	--	nS	$I_F=11A,$ $T_j = 25^{\circ}C$ $di/dt=100A/us$
Q_{rr}	Reverse Recovery Charge	--	1.7	--	uC	

Notes:

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- *1. $T_j=+25^{\circ}C$ to $+150^{\circ}C$.
 - *2. Repetitive rating; pulse width limited by maximum junction temperature.
 - *3. $I_{SD}=11A$ $di/dt \leq 100A/us$, $V_{DD} \leq BV_{DSS}$, $T_{jmax}=+150^{\circ}C$.
 - *4. Pulse width $\leq 380us$; duty cycle $\leq 2\%$.

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

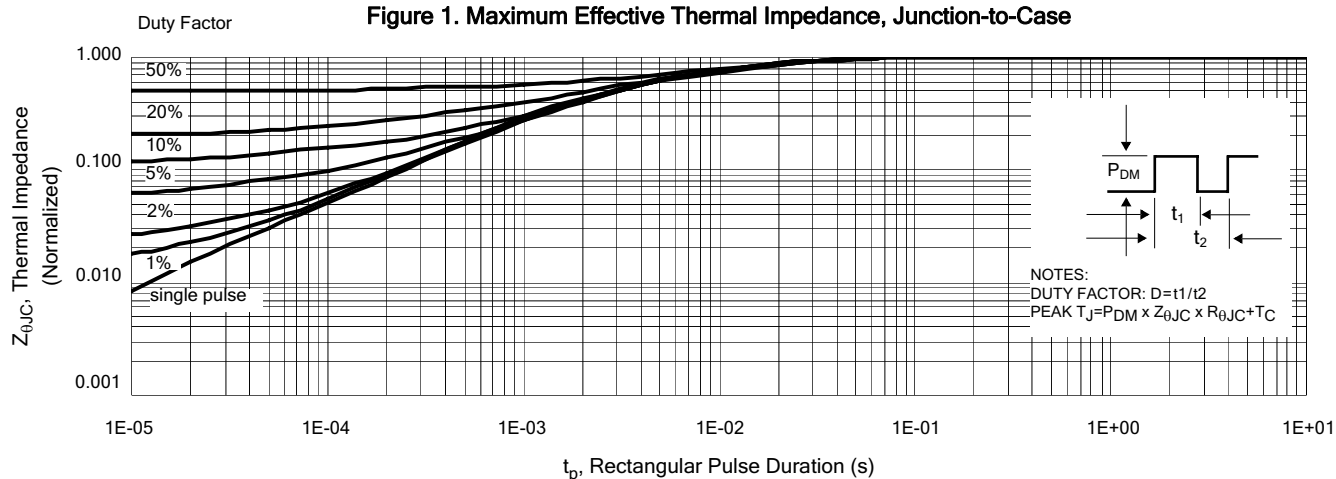


Figure 2. Maximum Power Dissipation vs Case Temperature

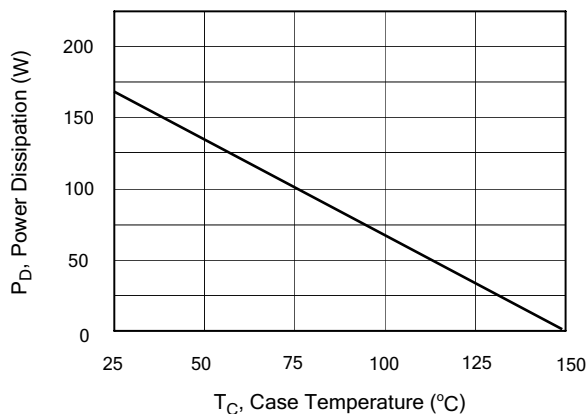


Figure3. Maximum Continuous Drain Current vs Case Temperature

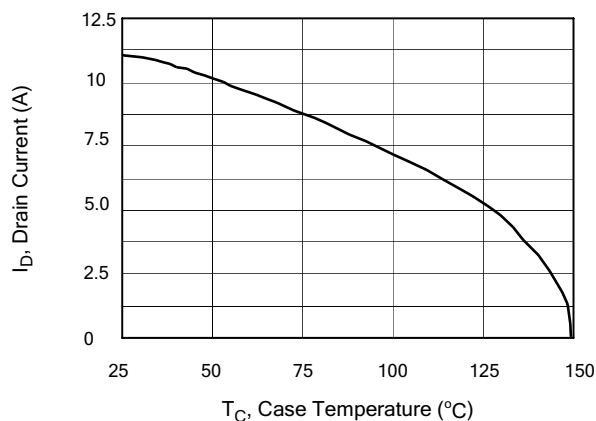


Figure 4. Typical Output Characteristics

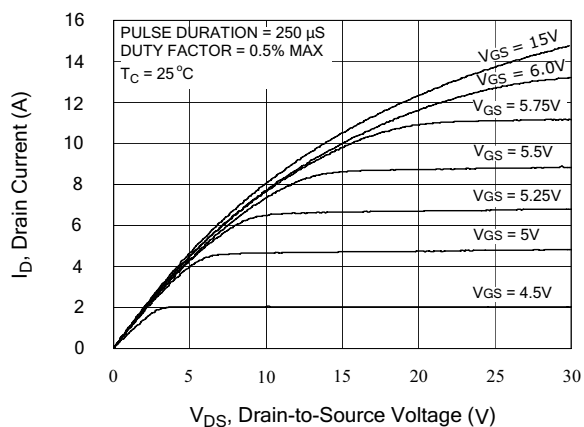


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

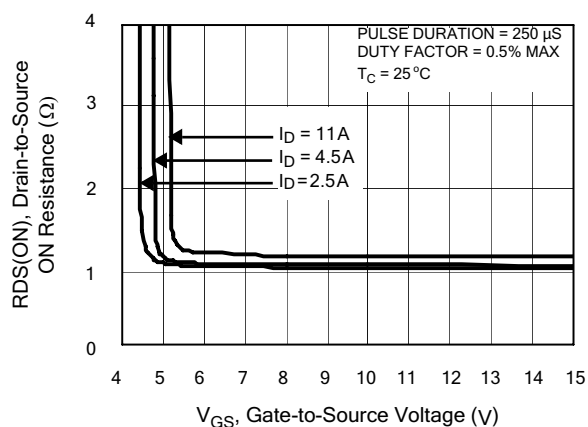


Figure 6. Maximum Peak Current Capability

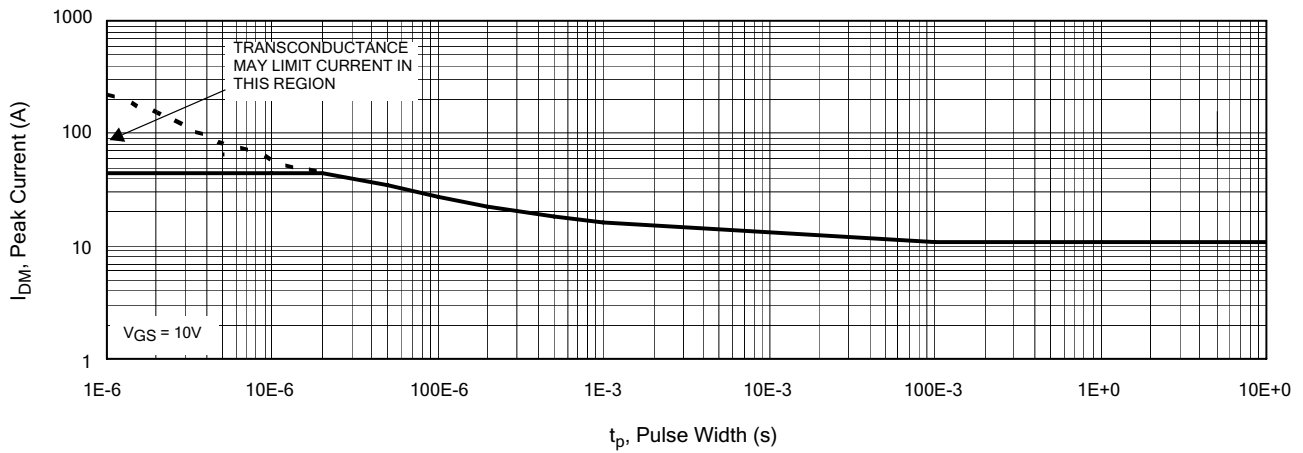


Figure 7. Typical Transfer Characteristics

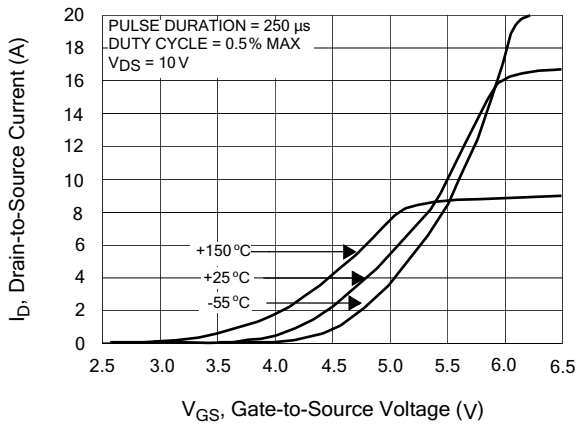


Figure8. Unclamped Inductive Switching Capability

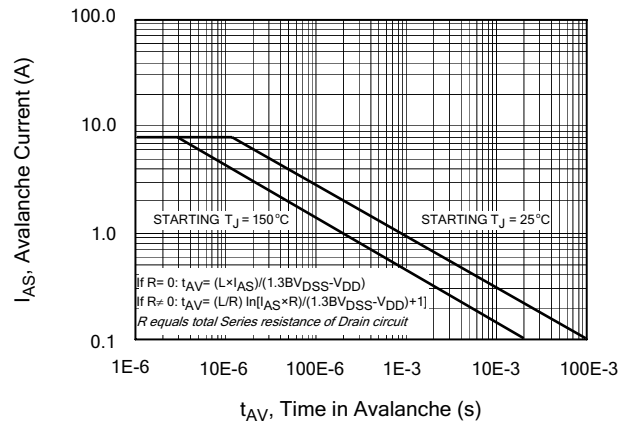


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

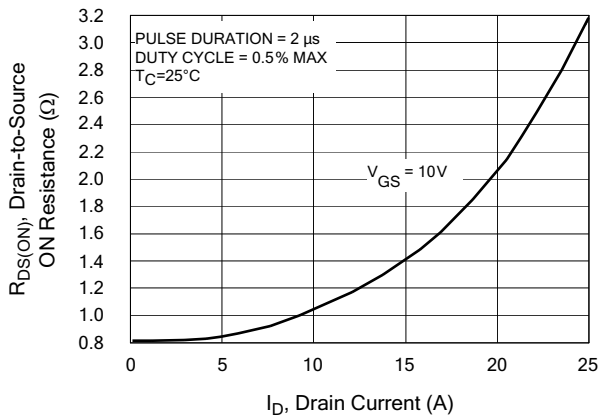


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

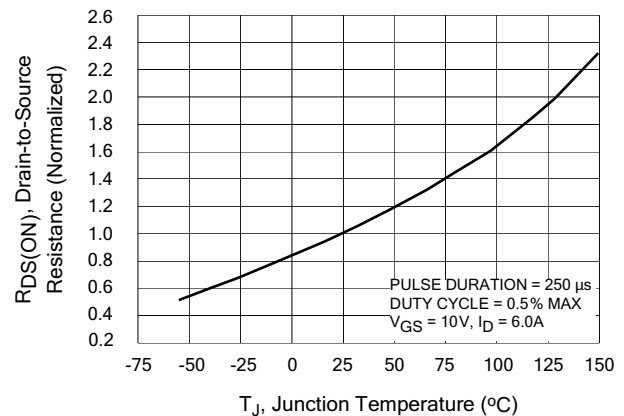


Figure 11. Typical Breakdown Voltage vs Junction Temperature

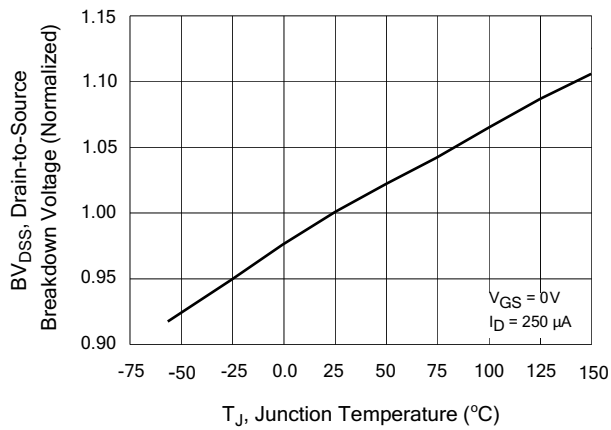


Figure 12. Typical Threshold Voltage vs Junction Temperature

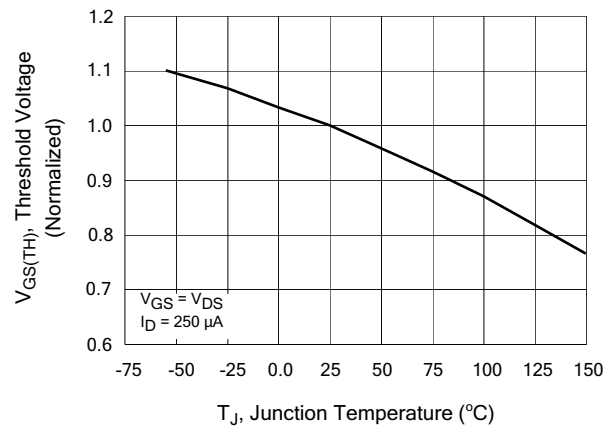


Figure 13. Maximum Forward Bias Safe Operating Area

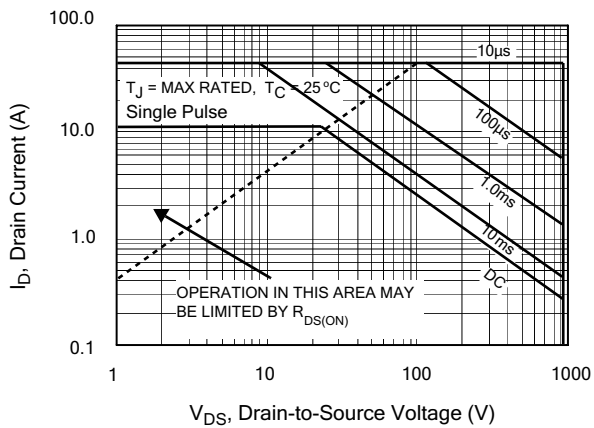


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

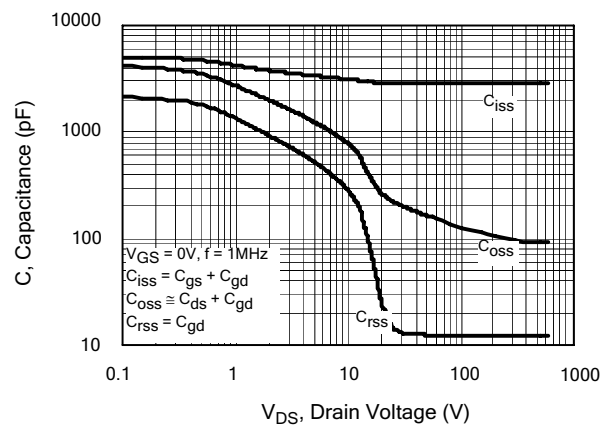


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

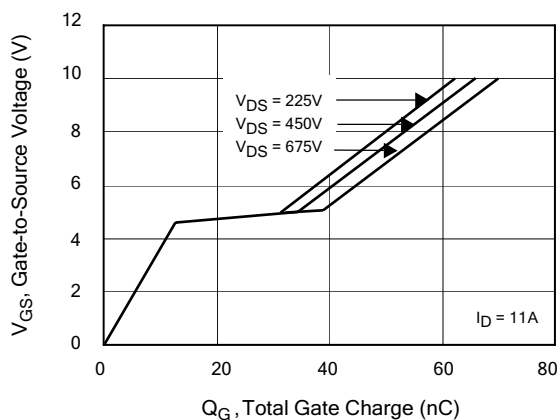
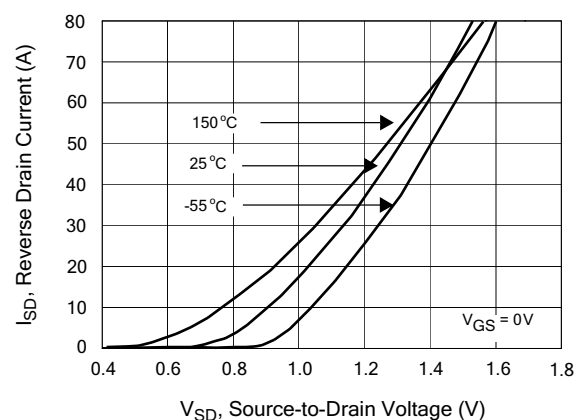


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

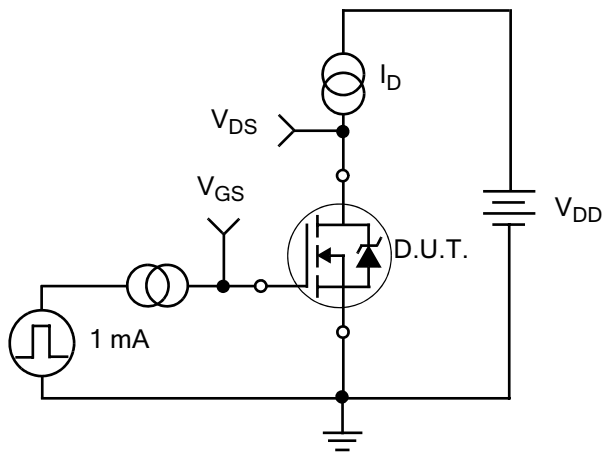


Figure 17. Gate Charge Test Circuit

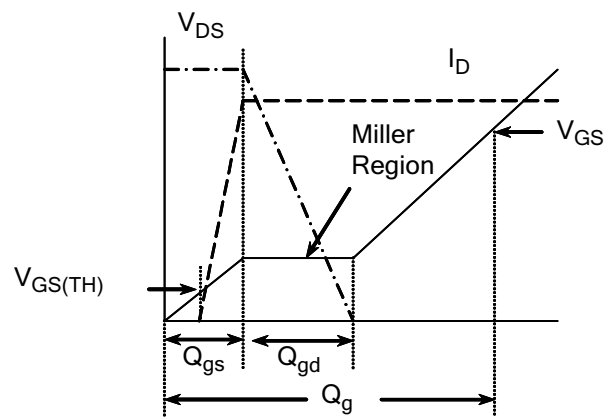


Figure 18. Gate Charge Waveform

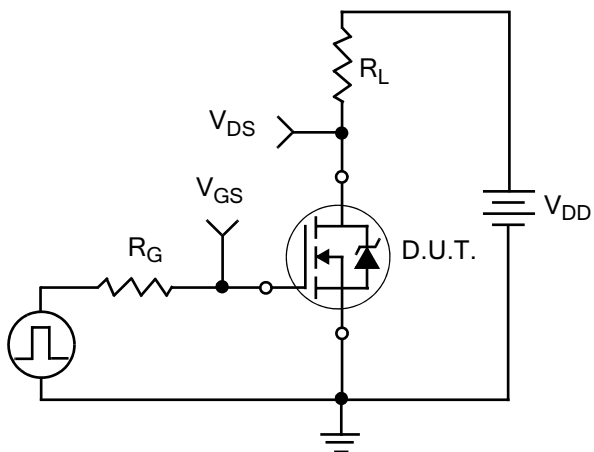


Figure 19. Resistive Switching Test Circuit

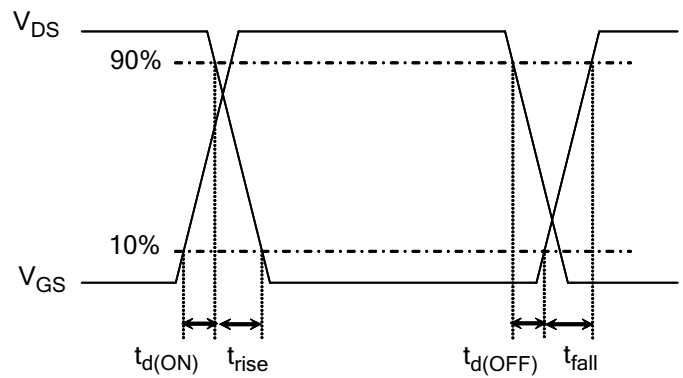


Figure 20. Resistive Switching Waveforms

Test Circuits and Waveforms

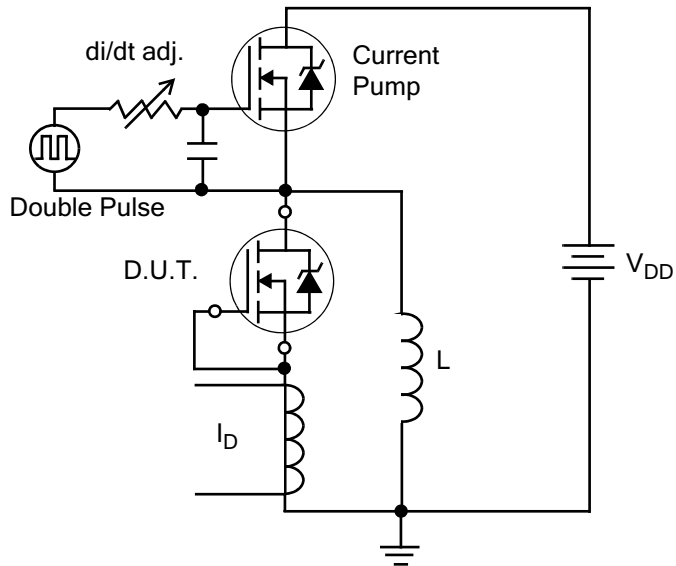


Figure 21. Diode Reverse Recovery Test Circuit

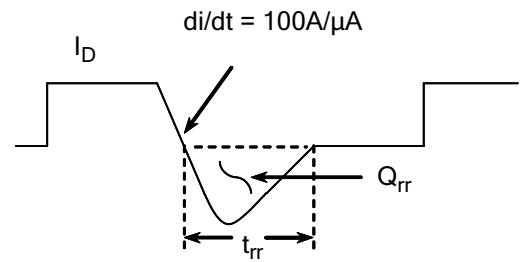


Figure 22. Diode Reverse Recovery Waveform

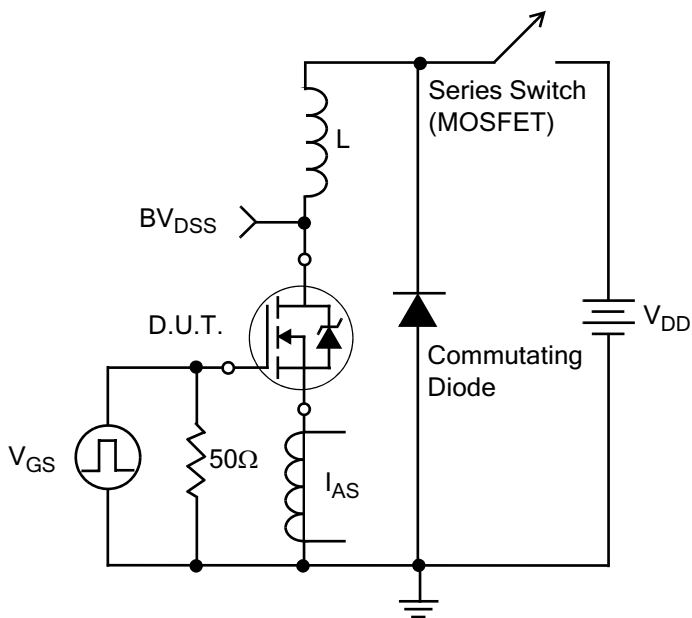


Figure 23. Unclamped Inductive Switching Test Circuit

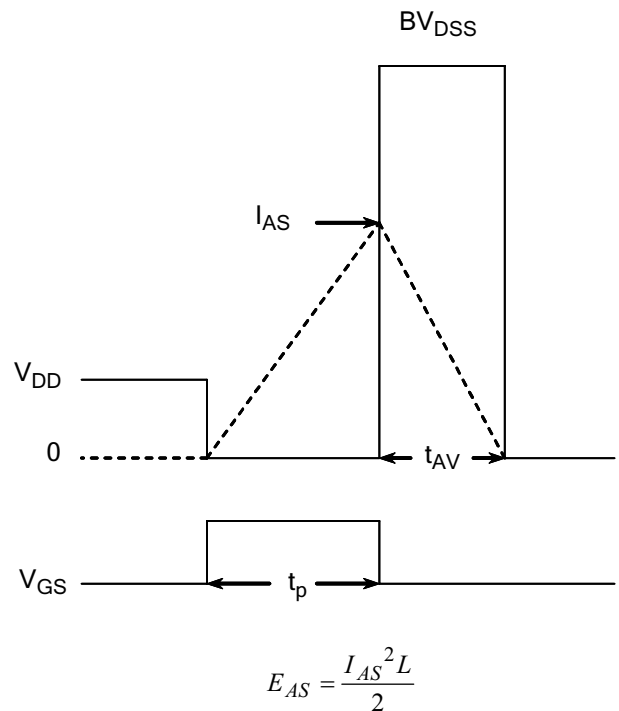


Figure 24. Unclamped Inductive Switching Waveforms

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