IT6633E-P

3-to-1 HDMI 1.3 Active Switch with EDID RAM

Preliminary Datasheet

ITE TECH. INC.

General Description

The IT6633 is a three-to-one HDMI v.1.3 active switch that supports a signalling rate of up to 2.25Gbps and the new Deep Color modes. A one-port SINK systems such as flat-panel TVs or LCD projectors could also easily upgrade to three-port by adding an IT6633 at the front. The IT6633 operates in software mode that allows the system to control it via a two-line serial interface, PCSCL/PCSDA. The IT6633 offers two selectable serial programming addresses by PCADR0.

As a active switch, the IT6633 equalizes incoming TMDS data with optimal quality regardless of the incoming signal quality. The highly acclaimed equalization technology of ITE TECH. INC. provides for support of long or low-quality HDMI cables at even the highest speeds. Input terminations of the TMDS inputs and output current levels are both programmable. In addition, the input terminations are disconnectable and hence significantly lower the system power consumption in inactive modes.

The IT6633 embeds an EDID RAM to save the cost of the Three external EDID ROMs. The process of downloading the EDID data into the RAM is simplified by the automatic read-back capability of the IT6633, minimizing the need of MCU intervention. The IT6633 also embeds three 1K-ohm resisters for HPD signal paths to save external resisters and easy to implement the plug authentication.

The IT6633 also incorporates I^2C repeater in its DDC switches, which isolates the DDC capacitances of the two sides of the switch. This allows for longer cable cascading as well as significantly eases the system design to pass **Test ID 8-9: DDC/CEC Line Capacitance and Voltage** of the HDMI Compliance Test.

The IT6633 also distinguish itself from its peers in that it offers ±8kV of Human Body Mode ESD protection to all TMDS high-speed input pins. This saves significant costs in external high-speed ESD diodes, which could be very expensive .

Features

- HDMI active switch, providing superior performance over traditional passive switches
- Compliant with HDMI 1.3 and DVI 1.0 standards
- Serial data rate at up to 2.25Gbps, capable of supporting the following digital video formats in Deep Color Mode at up to 36 bits (12 bits/color):
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i to 1080p
  - PC resolutions: VGA, SVGA, XGA, SXGA to UXGA
- Single 3.3V operation
- Internal AC-coupling at TMDS inputs to cope with uneven intra-pair DC levels of incoming TMDS signals.
- Embedded EDID RAM saves external EDID ROM costs
- Embedded HDP resistors
- Integrated HPD switches
- Active port detection by monitoring PWR5V inputs and TMDS input clock.
- DDC I^2C repeater isolates backend DDC capacitive loading from frontend, enhancing the DDC operation compatibility
- Human Body Mode ESD protection up to ±8kV for all TMDS differential input pins
- Disconnectable input terminations with auto-calibrated impedances
- Adaptive input equalization supporting long and short cables at the same time
- Software-mode operation providing flexibility
- Two possible serial programming device address..
- Programmable TMDS output current level
- Programmable source terminations compliant with HDMI 1.3 standard, providing optimal source data eyes at high speeds
- High-impedance TMDS output when disabled
- Optional backend receiver termination detection for auto powerdown
- 64-Pin LQFP package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6633E-P	0~70	64-pin LQFP	Green

Pin Diagram

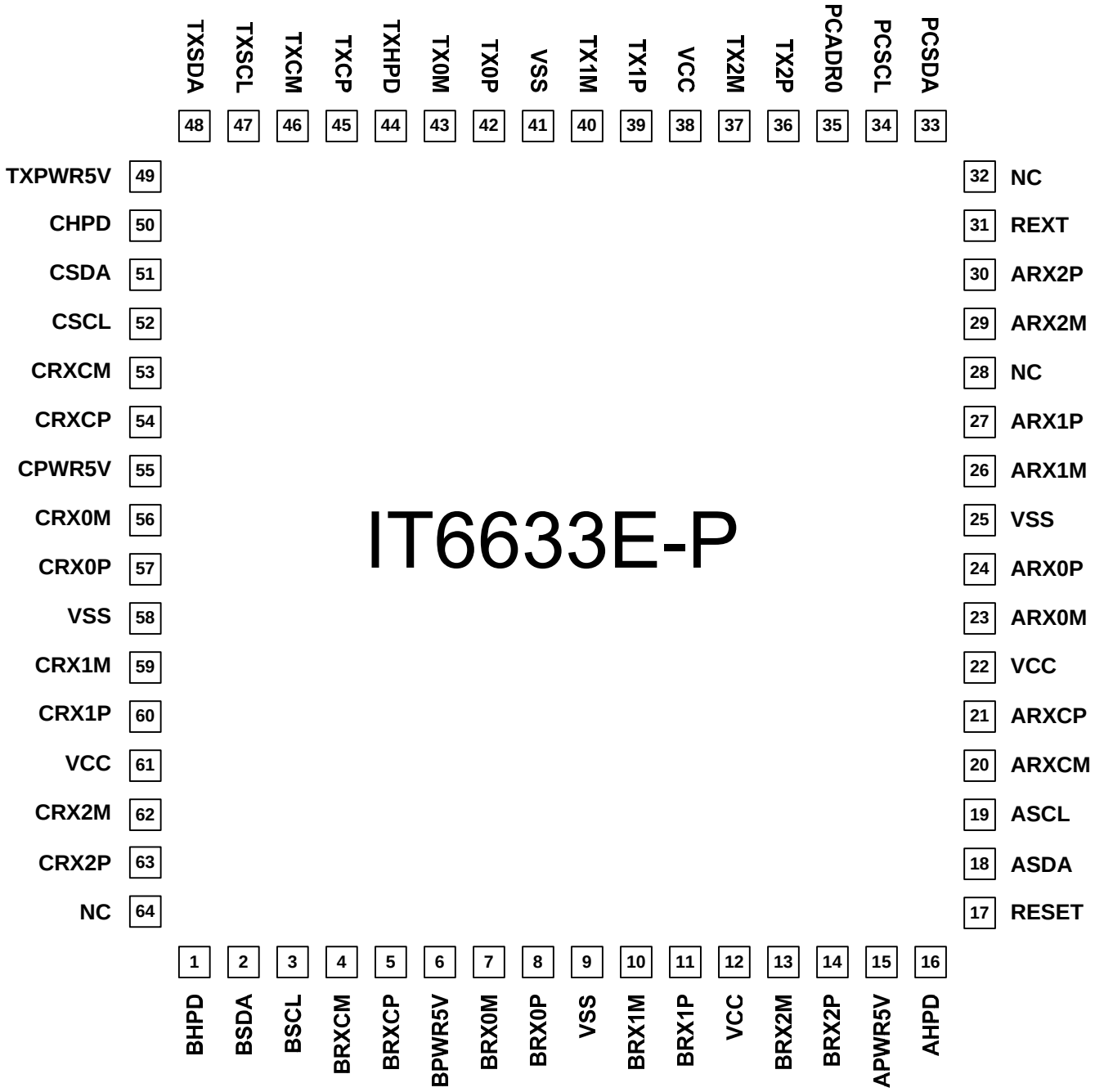


Figure 1. IT6633 pin diagram

Pin Description

TMDS High Speed Differential Input Pins (All these pins provide ±8kV HBM ESD Protection)

Pin Name	Direction	Description	Type	Pin No.
ARX2P	Input	Channel 2 positive input of Port A	TMDS	30
ARX2M	Input	Channel 2 negative input of Port A	TMDS	29
ARX1P	Input	Channel 1 positive input of Port A	TMDS	27
ARX1M	Input	Channel 1 negative input of Port A	TMDS	26
ARX0P	Input	Channel 0 positive input of Port A	TMDS	24
ARX0M	Input	Channel 0 negative input of Port A	TMDS	23
ARXCP	Input	Clock channel positive input of Port A	TMDS	21
ARXCM	Input	Clock channel negative input of Port A	TMDS	20
BRX2P	Input	Channel 2 positive input of Port B	TMDS	14
BRX2M	Input	Channel 2 negative input of Port B	TMDS	13
BRX1P	Input	Channel 1 positive input of Port B	TMDS	11
BRX1M	Input	Channel 1 negative input of Port B	TMDS	10
BRX0P	Input	Channel 0 positive input of Port B	TMDS	8
BRX0M	Input	Channel 0 negative input of Port B	TMDS	7
BRXCP	Input	Clock channel positive input of Port B	TMDS	5
BRXCM	Input	Clock channel negative input of Port B	TMDS	4
CRX2P	Input	Channel 2 positive input of Port C	TMDS	63
CRX2M	Input	Channel 2 negative input of Port C	TMDS	62
CRX1P	Input	Channel 1 positive input of Port C	TMDS	60
CRX1M	Input	Channel 1 negative input of Port C	TMDS	59
CRX0P	Input	Channel 0 positive input of Port C	TMDS	57
CRX0M	Input	Channel 0 negative input of Port C	TMDS	56
CRXCP	Input	Clock channel positive input of Port C	TMDS	54
CRXCM	Input	Clock channel negative input of Port C	TMDS	53

TMDS High Speed Differential Output Pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Output	Channel 2 positive output of output port	TMDS	36
TX2M	Output	Channel 2 negative output of output port	TMDS	37
TX1P	Output	Channel 1 positive output of output port	TMDS	39
TX1M	Output	Channel 1 negative output of output port	TMDS	40
TX0P	Output	Channel 0 positive output of output port	TMDS	42
TX0M	Output	Channel 0 negative output of output port	TMDS	43

TXCP	Output	Clock channel positive output of output port	TMDS	45
TXCM	Output	Clock channel negative output of output port	TMDS	46

DDC, HPD and PWR5V Control Pins

Pin Name	Direction	Description	Type	Pin No.
ASCL	I/O	Port A DDC bus clock line	5V-Tol.	19
ASDA	I/O	Port A DDC bus data line	5V-Tol.	18
BSCL	I/O	Port B DDC bus clock line	5V-Tol.	3
BSDA	I/O	Port B DDC bus data line	5V-Tol.	2
CSCL	I/O	Port C DDC bus clock line	5V-Tol.	52
CSDA	I/O	Port C DDC bus data line	5V-Tol.	51
TXSCL	I/O	Output Port DDC bus clock line	5V-Tol.	47
TXSDA	I/O	Output Port DDC bus data line	5V-Tol.	48
TXHPD	Input	HPD signal of the HDMI Sink	5V-Tol.	44
AHPD	Output	HPD signal to be sent back to Source connected to Port A	LVTTL	16
BHPD	Output	HPD signal to be sent back to Source connected to Port B	LVTTL	1
CHPD	Output	HPD signal to be sent back to Source connected to Port C	LVTTL	50
TXPWR5V	Output	When ‘1’, indicates that the selected input port has a valid PWR5V input and TMDS clock	LVTTL	49
APWR5V	Input	PWR5v of input port A for detection	5V-Tol	15
BPWR5V	Input	PWR5v of input port B for detection	5V-Tol	6
CPWR5V	Input	PWR5v of input port C for detection	5V-Tol	55

Other Control and Configuration Pins

Pin Name	Direction	Description	Type	Pin No.
RESET	Input	Reset signals for logic blocks (active-high)	LVTTL	17
PCSCL	Input	Serial programming Clock for chip programming (5V-tolerant)	Schmitt	34
PCSDA	I/O	Serial programming Data for chip programming (5V-tolerant)	Schmitt	33
PCADR0	Input	Control of serial programming device address: ‘0’: 0x94 ‘1’: 0x96 (default to ‘0’: 0x94 by internal weak pulled-down resistor of 100kΩ)	LVTTL	35
REXT	Analog	External resistor for auto-calibration. Must be tied to VSS via a 500Ω precision resistor.	Analog	31
NC		Must be left unconnected		28, 32, 64

Power and Ground Pins

Pin Name	Description	Type	Pin No.
VCC	Chip power supply (3.3V)	Power	12, 22, 38, 61
VSS	Chip ground	Ground	9, 25, 41, 58

Functional Description

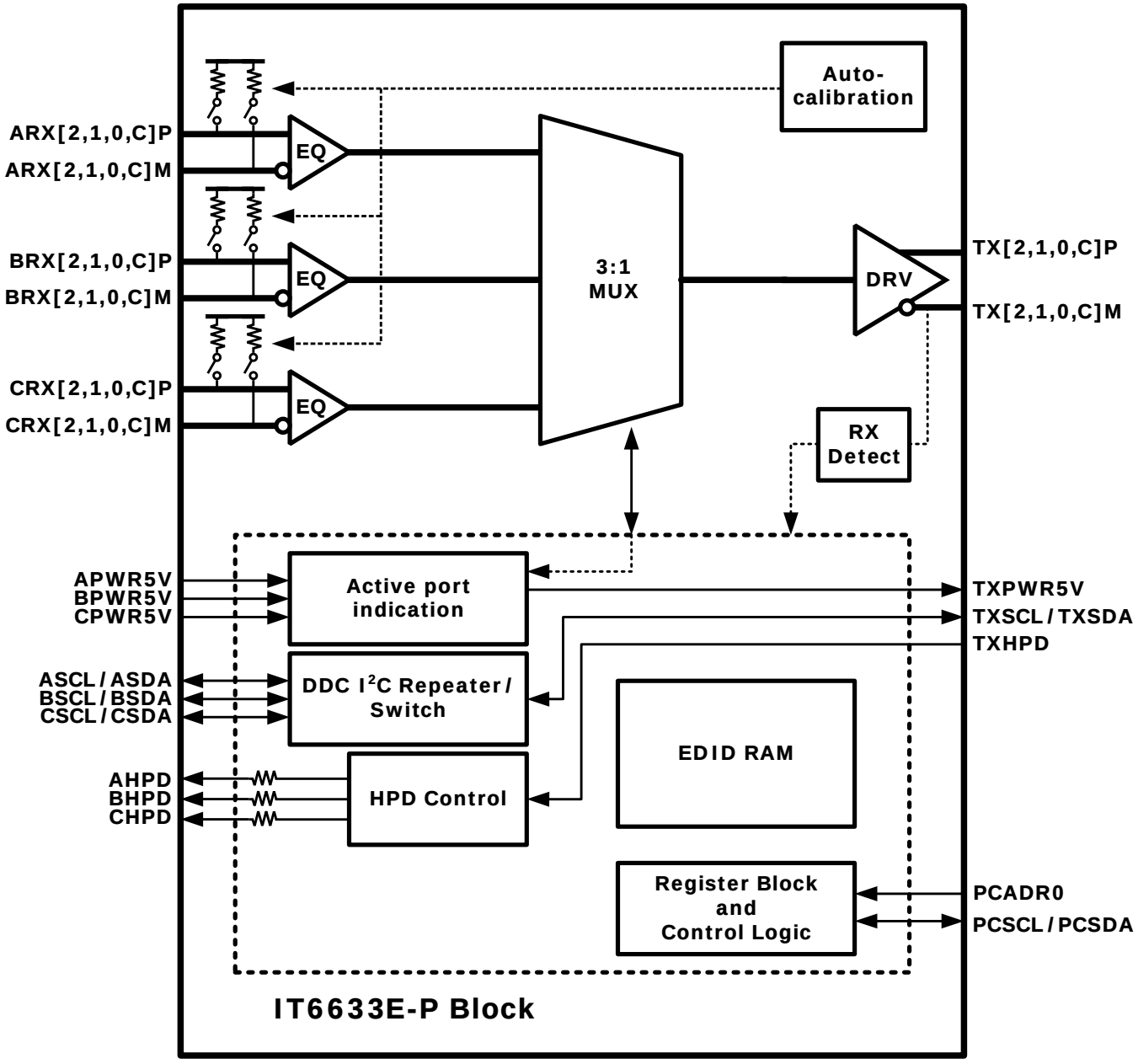
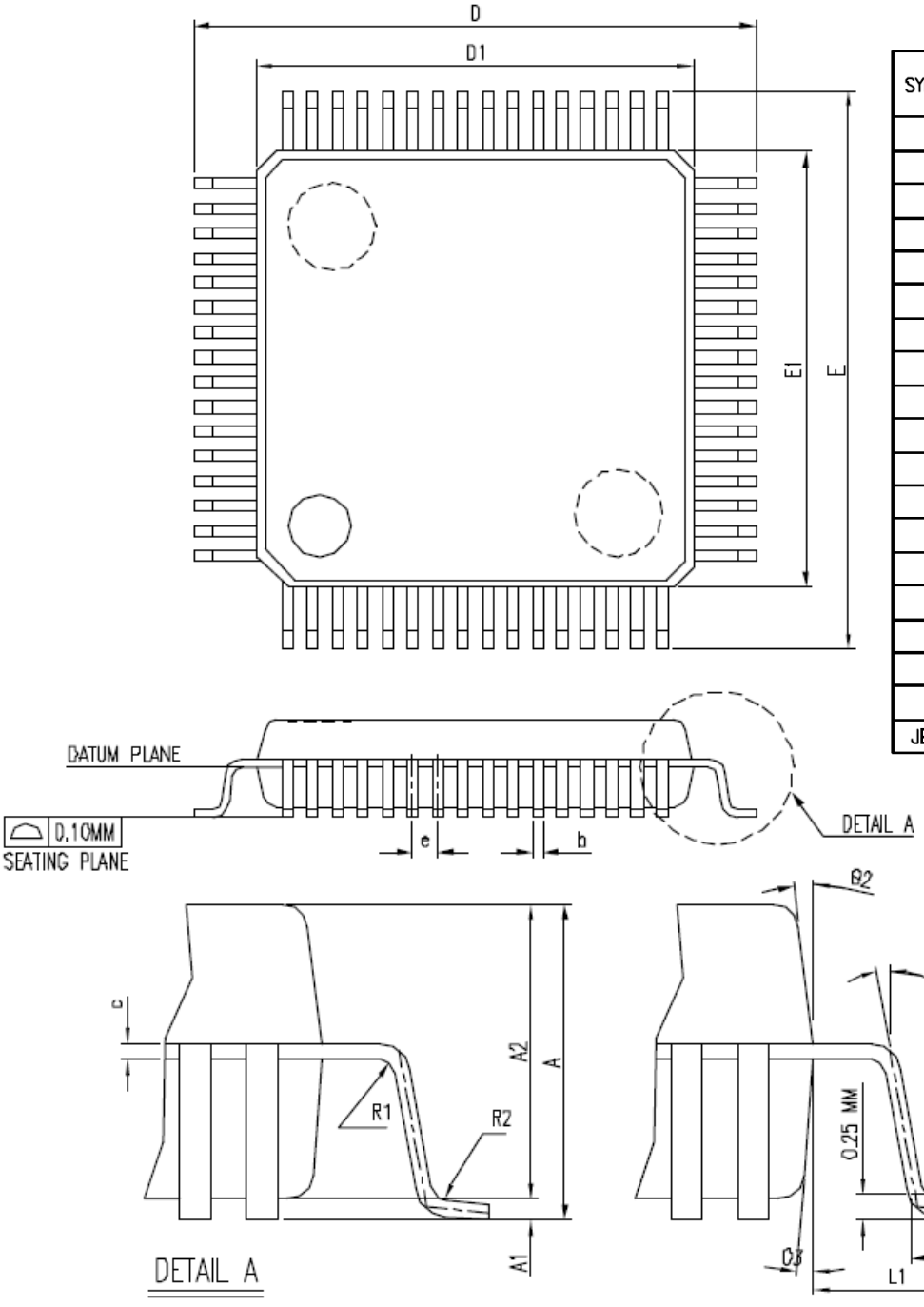


Figure 2. Functional block diagram of IT6633

Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.0019		0.0059
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09		0.20	0.0035		0.0078
e	0.40 BASIC			0.016 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.0031		
R2	0.08		0.20	0.0031		0.0078
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBD)					

Figure 3. 64-pin LQFP Package Dimensions