IT6692FN

Single Chip HDMI to VGA Converter with Embedded MCU

Preliminary Datasheet

ITE TECH. INC.

General Description

The IT6692FN is a high-performance single-chip HDMI to VGA converter. Combined with HDMI 1.3 receiver and triple DACs, the IT6692FN supports HDMI input and VGA output by conversion function. The build-in HDMI receiver is fully compliant with HDMI 1.3a specification. With HDMI 1.3a receiver, the IT6692FN can support resolutions up to Full HD (1080P), WUXGA and UXGA. Also the build-in triple DACs can support up to 10 bit deep colors.

The single chip IT6692FN provides high performance, cost effective, HDMI2VGA conversion function, and it can help modern NBs like ultrabooks and tablets to be compatible with traditional VGA only projectors, monitors, and TVs.

With Embedded MCU and Flash, IT6692FN is easy to program thru the ISP interface. Customers need no external Flash and MCU to save the BOM cost and board size.

Features (HDMI 1.3 RX)

- Single-link HDMI 1.3 receiver
- Compliant with HDMI 1.3a and DVI 1.0 specifications
- Supporting link speeds of up to 2.25Gbps (link clock rate of 225MHz).
- Auto-calibrated input termination impedance provides process-, voltage- and temperature-invariant matching to the input transmission lines.

Features (VGA DACs)

- Tripe **10-Bit** DAC Converters
- **200 MSPS** Throughput Rate
- Complementary Outputs
- DAC Output Current Range 2mA to 18.5mA

Features (Combined)

- Support up to **Full HD (1080P)** CEA display format
- Support up to **WUXGA(1920X1200 RB mode) and UXGA(1600x1200)** VESA display format
- Support HDMI Input deep color depth up to **12bit**, and support VGA output deep color depth up to **10bit**
- Embedded MCU and Flash
- 64-pin QFN (9mm x 9mm) package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6692FN	0~70	64-pin QFN	Green

Pin Diagram

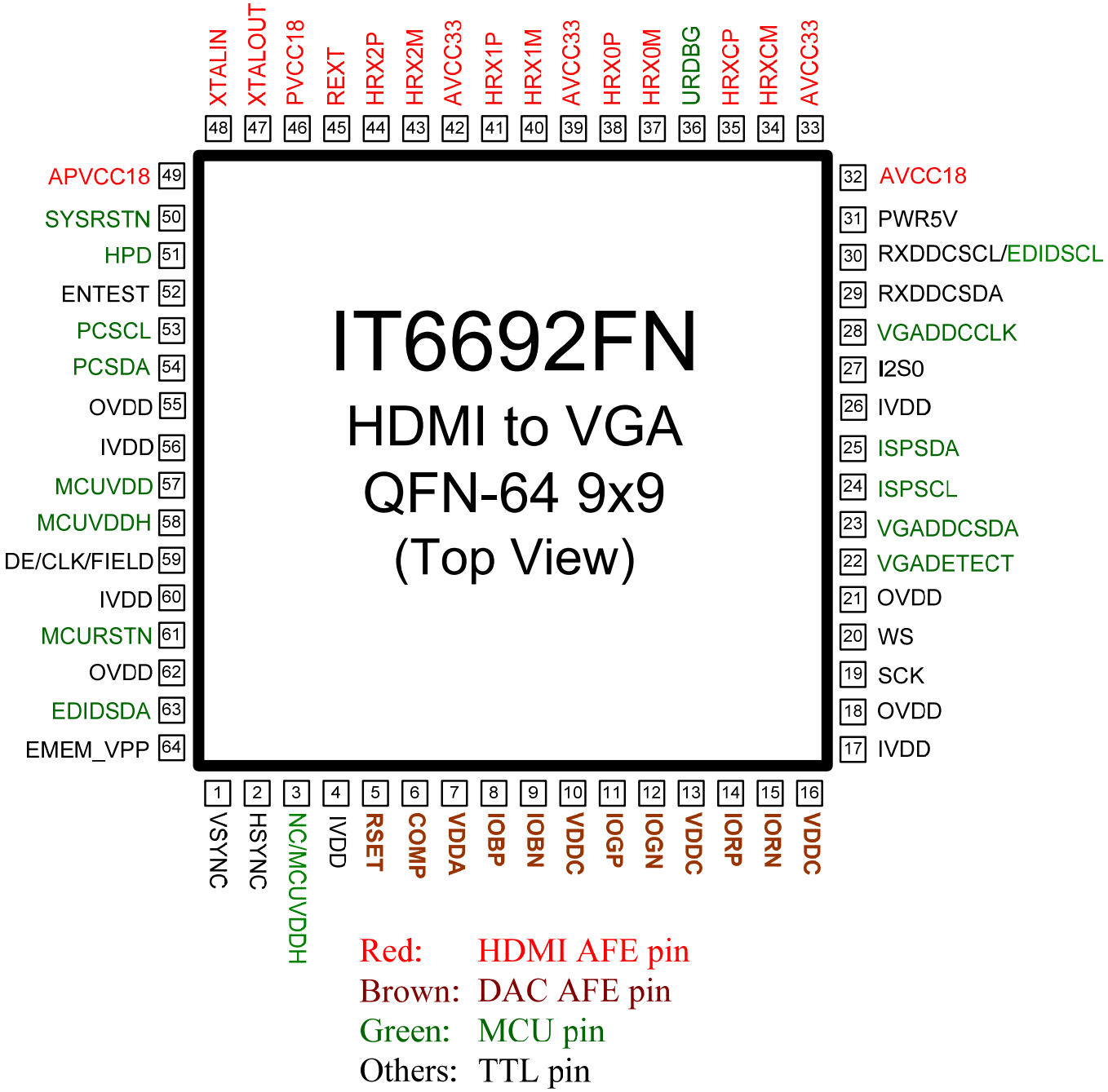


Figure 1. IT6692FN pin diagram

Pin Description

Digital Pins

Pin Name	Direction	Description	Type	Pin No.
DE/CLK/FIELD	Output	Digital Video timing debug Pin. Default is off.	LVTTL	59
HPD	Output	HDMI Hot-Plug control pin	LVTTL	51
HSYNC	Output	Horizontal sync. signal	LVTTL	2
VSYNC	Output	Vertical sync. signal	LVTTL	1
SCK	Output	I2S serial clock output	LVTTL	19
WS	Output	I2S word select output	LVTTL	20
I2S0	Output	I2S serial data output	LVTTL	27
RXDDCSCL	I/O	DDC I2C Clock for HDMI Port (5V-tolerant)	Schmitt	30
RXDDCSDA	I/O	DDC I2C Data for HDMI Port (5V-tolerant)	Schmitt	29
PWR5V	Input	TMDS transmitter detection for Port (5V-tolerant)	Schmitt	31
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	50
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	53
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	54
ENTEST	Input	Test mode, must be tied to Ground.	Schmitt	52
EMEM_VPP	Input	Must be tied to Ground.		64

HDMI Analog Front-End interface pins

Pin Name	Direction	Description	Type	Pin No.
R0X2P	Analog	HDMI Channel 2 positive input for HDMI Port	TMDS	44
R0X2M	Analog	HDMI Channel 2 negative input for HDMI Port	TMDS	43
R0X1P	Analog	HDMI Channel 1 positive input for HDMI Port	TMDS	41
R0X1M	Analog	HDMI Channel 1 negative input for HDMI Port	TMDS	40
R0X0P	Analog	HDMI Channel 0 positive input for HDMI Port	TMDS	38
R0X0M	Analog	HDMI Channel 0 negative input for HDMI Port	TMDS	37
R0XCP	Analog	HDMI Clock Channel positive input for HDMI Port	TMDS	35
R0XCM	Analog	HDMI Clock Channel negative input for HDMI Port	TMDS	34
REXT	Analog	External resistor for setting termination impedance value. Should be tied to GND via a 500Ω SMD resistor.	Analog	45
XTALIN	Input	Crystal clock input	Analog	48
XTALOUT	Output	Crystal clock output	Analog	47

DAC Analog Front-End interface pins

Pin Name	Direction	Description	Type	Pin No.
IORP, IOGP, IOBP	Output	Red, Green, and Blue Current Outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.	Analog	14 11 8
IORN, IOGN, IOBN	Output	Differential Red, Green, and Blue Current Output. These RGB video outputs are specified to directly drive a doubly terminated 75Ω load. If the complementary outputs are not required, these outputs should be tied to ground.	Analog	15 12 9
R_{SET}	Analog	Voltage Reference Input for DACs or Voltage Reference Output.	Analog	5
COMP	Analog	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1uF ceramic capacitor must be connected between COMP and VDDA.	Analog	6

MCU Control Pins

Pin Name	Direction	Description	Type	Pin No.
MCURSTN	Input	MCU Hardware reset pin. Active LOW	LVTTL	61
EDIDSDA	I/O	I2C Master Data for EDID programming(5V-tolerant)	LVTTL	63
VGADETECT	Input	Detect VGA plug-on or not	LVTTL	22
VGADDCSDA	I/O	DDC clock interface to VGA (5V tolerant)	LVTTL	23
VGADDCCLK	I/O	DDC data interface to VGA (5V tolerant)	LVTTL	28
ISPSCL	I/O	ISP programming data pin	LVTTL	24
ISPSDA	I/O	ISP programming data pin	LVTTL	25
URDBG	I/O	UR interface for S/W debugging	LVTTL	36

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	4, 17, 26, 56, 60
OVDD	I/O Pin power (3.3V)	Power	18, 21, 55, 62
AVCC33	HDMI analog frontend power (3.3V)	Power	33, 39, 42
AVCC18	HDMI analog frontend power (1.8V)	Power	32
PVCC18	HDMI receiver PLL power (1.8V)	Power	46
APVCC18	HDMI crystal and audio PLL power (1.8V)	Power	49
VDDA	ADC Analog power supply (1.8V) for Voltage reference circuit.	Power	7
VDDC	Analog power supply (1.8V) for three DACs.	Power	10, 13, 16

MCUVDD	Internal Generated Power for Embedded MCU (2.5V)	Power	57
MCUVDDH	Supply Power for Embedded MCU (5V)	Power	58
NC/MCUVDDH	Supply Power for Embedded MCU (5V)	Power	3
GND	Exposed GND pad	Ground	65

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
AVCC33	HDMI analog frontend power	-0.3		4.0	V
AVCC18	HDMI analog frontend power	-0.3		2.5	V
PVCC18	HDMI receiver PLL power	-0.3		2.5	V
APVCC18	HDMI audio PLL power	-0.3		2.5	V
VDDA	ADC Analog power(1.8V) for Voltage reference circuit.	-0.3		2.5	V
VDDC	Analog power supply (1.8V) for three DACs.	-0.3		2.5	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	**4000**			V
ESD_MM	Machine mode ESD sensitivity	**300**			V

Notes:

1. **Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.**

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.62	1.8	1.98	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
AVCC33	HDMI analog frontend power[2]	3.135	3.3	3.465	V
AVCC18	HDMI analog frontend power	1.62	1.8	1.98	V
PVCC18	HDMI receiver PLL power	1.62	1.8	1.98	V
APVCC18	HDMI audio PLL power	1.62	1.8	1.98	V
VDDA	ADC Analog power(1.8V) for Voltage reference circuit.	1.71	1.8	1.9	V
VDDC	Analog power supply (1.8V) for three DACs.	1.71	1.8	1.9	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C

Θ_{ja}	Junction to ambient thermal resistance				°C/W

Notes:
1. AVCC33, AVCC18, PVCC18 and APVCC18 should be regulated.
2. AVCC33 supplies the termination voltage. Therefore the range is specified by the HDMI Standard.

Operation Supply Current Specification

Symbol	Parameter	PCLK	Typ	Max	Unit
I_{IVDD_OP}	IVDD current under normal operation	27MHz	20	27	mA
		74.25MHz	48	62	mA
		148.5MHz	90	108	mA
		222.75MHz	128	146	mA
I_{OVDD_OP}	OVDD current under normal operation (with 20pF capacitive output loading)	27MHz	0.1	0.1	mA
		74.25MHz	0.1	0.2	mA
		148.5MHz	0.2	0.3	mA
		222.75MHz	0.3	0.3	mA
I_{AVCC18_OP}	AVCC18 current under normal operation (with input Vdiff= 750 mV)	27MHz	14	14	mA
		74.25MHz	18	18	mA
		148.5MHz	22	22	mA
		222.75MHz	27	27	mA
I_{AVCC33_OP}	AVCC33 current under normal operation (with input Vdiff= 750 mV)	27MHz	45	45	mA
		74.25MHz	45	45	mA
		148.5MHz	45	45	mA
		222.75MHz	45	45	mA
I_{PVCC18_OP}	PVCC18 current under normal operation	27MHz	48	48	mA
		74.25MHz	63	63	mA
		148.5MHz	78	78	mA
		222.75MHz	98	98	mA
$I_{APVDD18\_OP}$	APVDD18 current under normal operation	27MHz	0.4	0.4	mA
		74.25MHz	0.4	0.4	mA
		148.5MHz	0.4	0.4	mA
		222.75MHz	0.4	0.4	mA
I_{VDDA}	DAC VDDA current under normal operation	(all speeds)	0.5	0.5	mA
I_{VDDC}	DAC VDDC current under normal operation	(all speeds)	68	68	mA
PW_{TOTAL_OP}	Total power consumption under normal operation[3]	27MHz	**420**	**433**	mW
		74.25MHz	**505**	**530**	mW
		148.5MHz	**615**	**648**	mW
		222.75MHz	**728**	**760**	mW

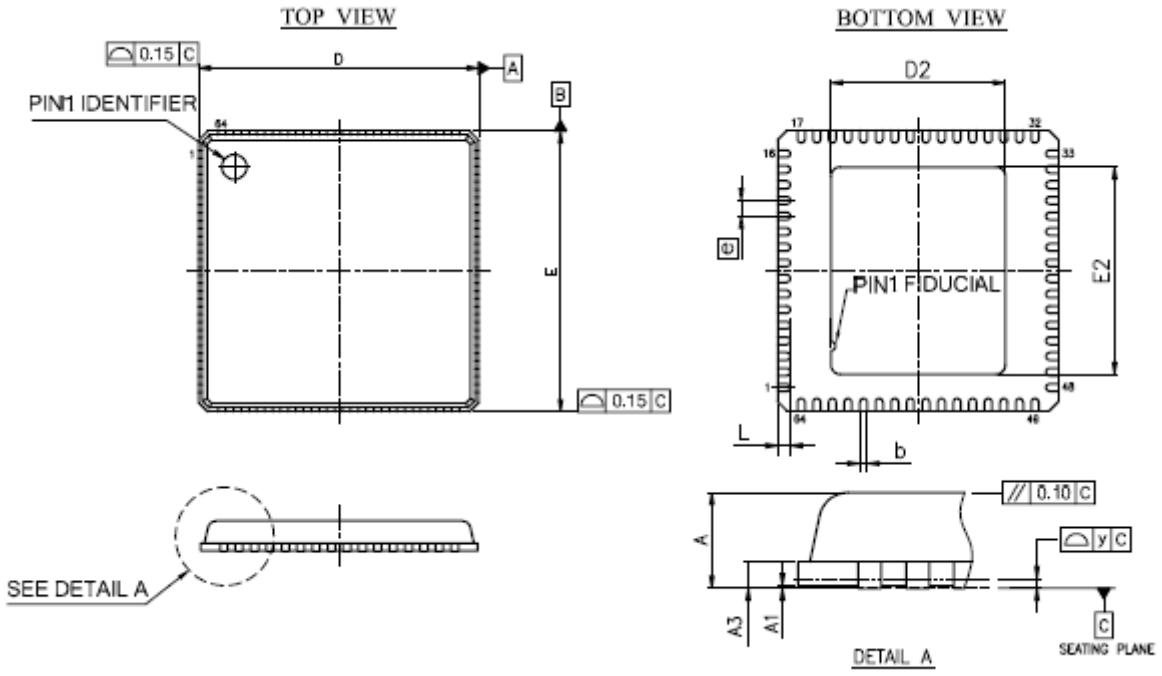
Notes:
1. Typ: OVDD=AVCC33 =3.3V, IVDD=AVCC18=PVCC18=APVCC18=VDDA=VDDC=1.8V, Typical pattern
   Max: OVDD=AVCC33 =3.3V, IVDD=AVCC18=PVCC18=APVCC18=VDDA=VDDC=1.8V, Worst case pattern
2. PCLK=27MHz: 480p without Audio
   PCLK=74.25MHz: 1080i without audio,
   PCLK=148.5MHz: 1080p without audio,
   PCLK=222.75MHz: 1080p**@36-bit Deep Color** without audio
3. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.

DAC Specification

(VDDA=VDDC=1.8V±5%, R_{SET}=100Ω, R_L=37.5Ω. All specification are T_A=25℃, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE					
MAX Luminance Voltage	0.665	0.7	0.77	Volts	Input Data=(3FFh)
MIN Luminance Voltage		0		Volts	Input Data=(000h)
Resolution (Each DAC)			10	Bits	
Offset Error		0	0	LSB	
Gain Error		0		LSB	
Integral Linearity Error	-1		+1	LSB	
Differential Linearity Error	-1		+1	LSB	
Monotonic		Yes			
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			Volts	
Input Low Voltage, V_{IL}		0.8		Volts	
ANALOG OUTPUTS					
Output Current	2		18.5	mA	R_{SET}=1kΩ ~ 100Ω
Video Channel to Video Channel Mismatch		2	6	%	% of Max Luminance Voltage
Video Channel to Video Channel Output Skew		1		ns	
Video Noise Injection Ratio	-2.5	1	2.5	%	% of Max Luminance Voltage
Overshoot/Undershoot	-12	1	12	%	
Video Channel Rise/Fall Time		1	3	ns	
Maximum Settling Time After Overshoot/Undershoot		1	3	ns	
POWER DISSIPATION					
RGB Channels Supply Current	0.5	64.5		mA	Min. current is measured in power-down mode.
Voltage Reference Supply Current	50	280		uA	
Digital Supply Current	0.3	3.8		mA	

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.035	0.039	0.80	0.90	1.00
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.350	0.354	0.358	8.90	9.00	9.10
D2	0.141	0.149	0.157	3.58	3.78	3.98
E	0.350	0.354	0.358	8.90	9.00	9.10
E2	0.141	0.149	0.157	3.58	3.78	3.98
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
y	--	--	0.003	--	--	0.08

Figure 2. 64-pin QFN Package Dimensions