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IT7236AFN/ IT7236BFN/ IT7236CFN

Touch ASIC Cap Button Controller

Preliminary Specification V0.3.1.1

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
-	Initial release for IT7236 product in QFN package	-

CONTENTS

FIGURES

TABLES

1. Features

- **Programmable Capacitance-to-Digital Converter (CDC)**
  - Maximum 14 capacitance sensor inputs
  - 10 ms update rate, all 14 sensor stages (under decimation rate 64)
  - No external RC components required
  - Automatic conversion sequencer

- **On-chip Automatic Calibration Logic**
  - Automatic calibration & compensation for environmental changes
  - Automatic adaptive threshold and sensitivity levels

- **8051 Embedded Controller**
  - Two clocks per machine cycle architecture
  - Instruction set compatible with standard 8051
  - Maximum 16 MHz for CPU speed
  - Supports CPU power-saving mode

- **On-chip 8KByte e-Flash ROM**
  - 8Kx8 e-Flash ROM for internal CPU firmware program
  - e-Flash 100K times program / erase
  - Extra 8Kx8 SRAM for saving e-Flash power consumption by launching firmware in e-Flash

- **On-chip 2KB Shared SRAM**
  - Used for external host to share information or handshaking with internal firmware
  - Used as internal data buffer for internal CPU

- **Supports High Current General Purpose Input/Output (GPIO) and PWM Function for LED Dimming Control**
  - up to 7 pins for these functions

- **Supports Low Current GPIO function for General Purpose Function Control**
  - up to 14 pins for these functions at 32-pin QFN (7 pins at 24-/16-pin QFN)

- **Watchdog**
  - At least 0.1 second dog barking

- **Supports Dynamic Power Saving Mode**
  - Provides host special commands to switch between two operational modes: active and idle modes

- **I2C Compatible Interface**
  - Compliant with I^{2}C specification v2.1
  - Supports slave device only
  - Supports standard and fast modes
  - 7-bit device addressing modes
  - Supports 1 address select pins to configure the device address selection

- **Operation Power**
  - Two power sources: VCCIO: 1.62V~5.5V, AVCC: 2.25V~5.5V
  - Provides one internal power regulator for core power generation

- **Power Consumption (@System Clock 8MHz,ADC Clock 250KHz)**
  - Active mode: 1.25 mA
  - Idle mode: 730 uA
  - Deep idle mode: 120uA

- **Package**
  - 32-pin QFN
  - 24-pin QFN
  - 16-pin QFN

- **Supports up to Two True 7 bits of DAC (Output 0V~5V or 0V~3.3V voltage range by Power)**
  - Supports LED driving as well

- **RoHS Compliant (100% Green Available)**

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2. General Description

The IT7236, one MCU-base programmable controller with capacitance sensors, is used to implement functions such as buttons, scroll bars, and wheels. One single electrode capacitance-to-digital converter (CDC) is integrated into this controller. This chip also includes one powerful twin-turbo 8051 CPU along with one 8K bytes of e-Flash ROM to support customer-specified features.

The IT7236 also provides a post-processing with CDC, and it can automatically calibrate and compensate the front-end CDC values for environmental changes. It also modifies the threshold and sensitivity levels automatically. The chip supports one interrupt output indicated that the CDC value over the user programming sensitivity level.

The IT7236 supports one I^2C compatible interface to communicate with the host. Through this interface, the host can program the internal controlled registers to configure this chip to meet users' requirements. Furthermore, GPIO and PWM-Based current-control functions are supported to indicate the specific status or LED dimming by the user's definition.

The IT7236 is available in 32-pin, 24-pin, or 16-pin QFN package type.

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3. Block Diagram
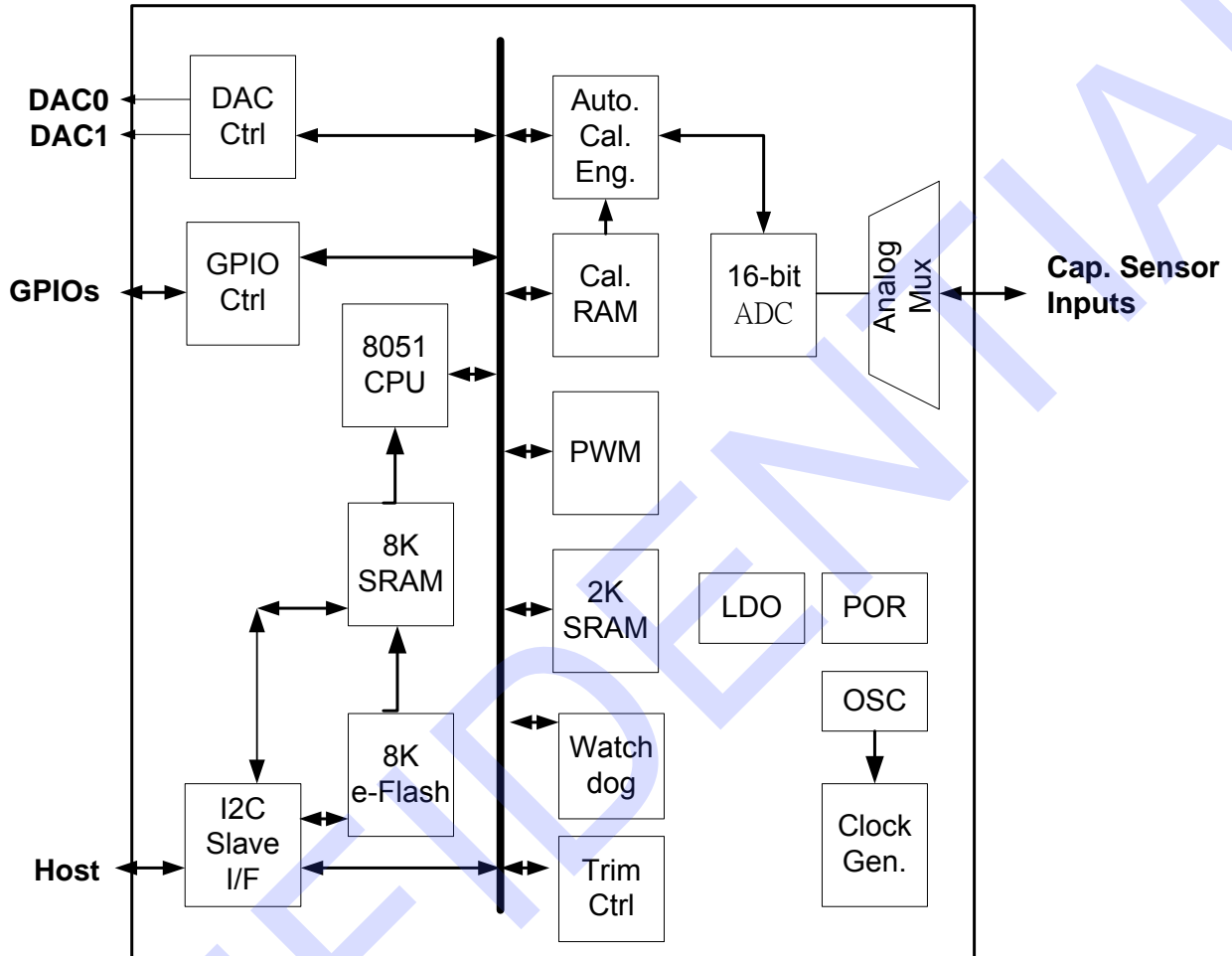
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4. Pin Configuration
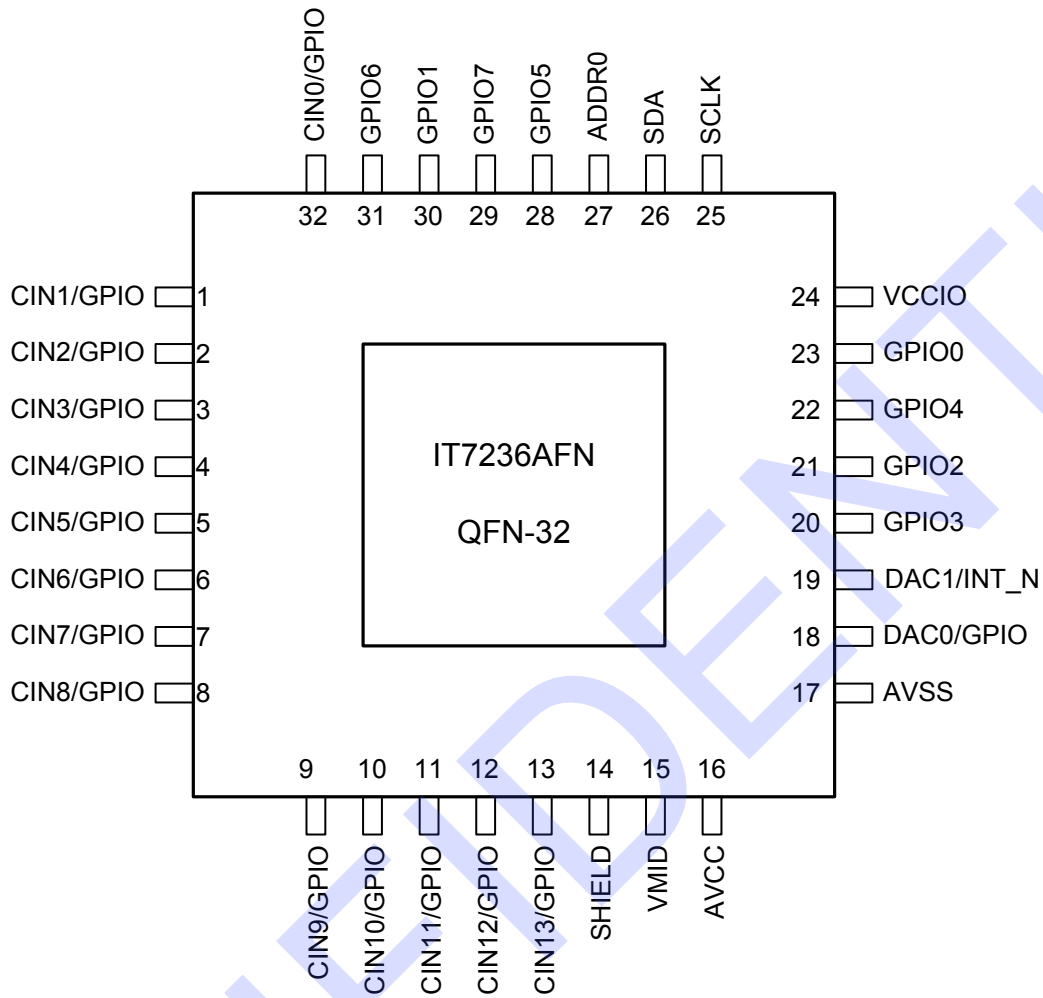
Table 4-1. IT7236AFN Pins Listed in Numeric Order (32-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN1/GPIO	9	CIN9/GPIO	17	AVSS	25	SCLK
2	CIN2/GPIO	10	CIN10/GPIO	18	DAC0/GPIO	26	SDA
3	CIN3/GPIO	11	CIN11/GPIO	19	DAC1/INT_N	27	ADDR0
4	CIN4/GPIO	12	CIN12/GPIO	20	GPIO3	28	GPIO5
5	CIN5/GPIO	13	CIN13/GPIO	21	GPIO2	29	GPIO7
6	CIN6/GPIO	14	SHIELD	22	GPIO4	30	GPIO1
7	CIN7/GPIO	15	VMID	23	GPIO0	31	GPIO6
8	CIN8/GPIO	16	AVCC	24	VCCIO	32	CIN0/GPIO

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```
                    GPIO5  ADDR0  SDA  SCLK  VCCIO  GPIO0

                     24     23    22    21    20     19

          GPIO1 ⊏ 1                                  18 ⊐ GPIO4

          GPIO6 ⊏ 2                                  17 ⊐ GPIO2

       CIN2/GPIO ⊏ 3           IT7236BFN            16 ⊐ GPIO3

       CIN4/GPIO ⊏ 4             QFN-24             15 ⊐ DAC1/INT_N

       CIN5/GPIO ⊏ 5                                  14 ⊐ DAC0/GPIO

       CIN6/GPIO ⊏ 6                                  13 ⊐ AVSS

                      7     8     9    10    11     12

                  CIN7/GPIO CIN8/GPIO CIN9/GPIO SHIELD VMID AVCC
```
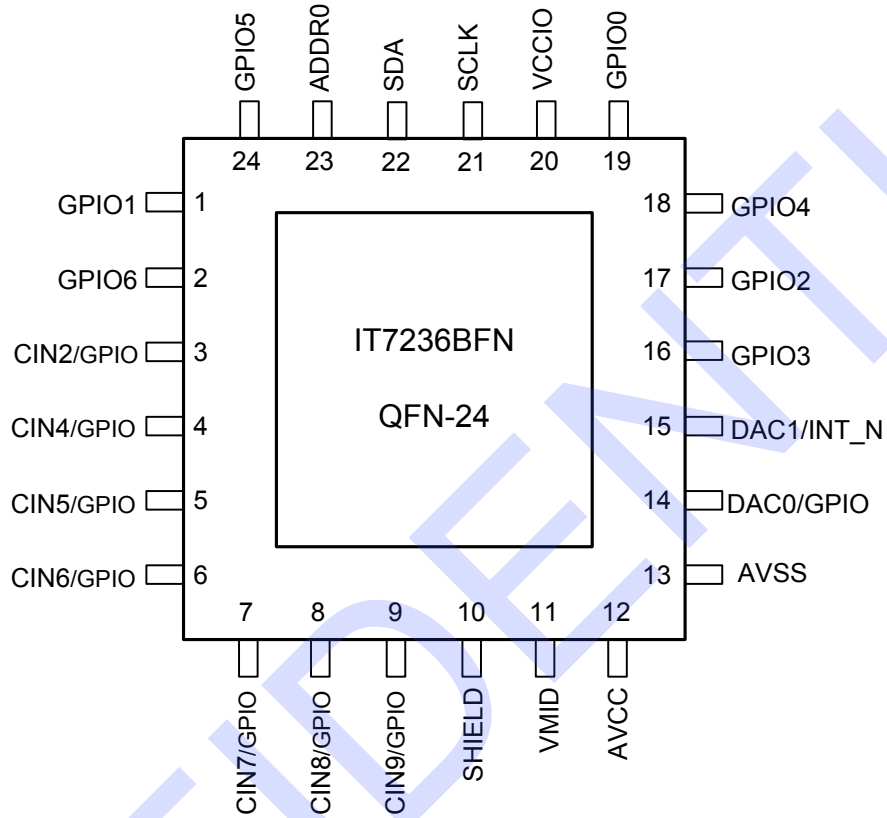
Table 4-2. IT7236BFN Pins Listed in Numeric Order (24-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GPIO1	7	CIN7/GPIO	13	AVSS	19	GPIO0
2	GPIO6	8	CIN8/GPIO	14	DAC0/GPIO	20	VCCIO
3	CIN2/GPIO	9	CIN9/GPIO	15	DAC1/INT_N	21	SCLK
4	CIN4/GPIO	10	SHIELD	16	GPIO3	22	SDA
5	CIN5/GPIO	11	VMID	17	GPIO2	23	ADDR0
6	CIN6/GPIO	12	AVCC	18	GPIO4	24	GPIO5

CIN1/GPIO — 16
CIN0/GPIO — 15
SDA — 14
SCLK — 13

CIN2/GPIO — 1
CIN4/GPIO — 2
CIN6/GPIO — 3
CIN7/GPIO — 4

IT7236CFN

QFN-16

12 — VCCIO
11 — DAC1/INT_N
10 — DAC0/GPIO
9 — AVSS

5 — CIN8/GPIO
6 — SHIELD
7 — VMID
8 — AVCC
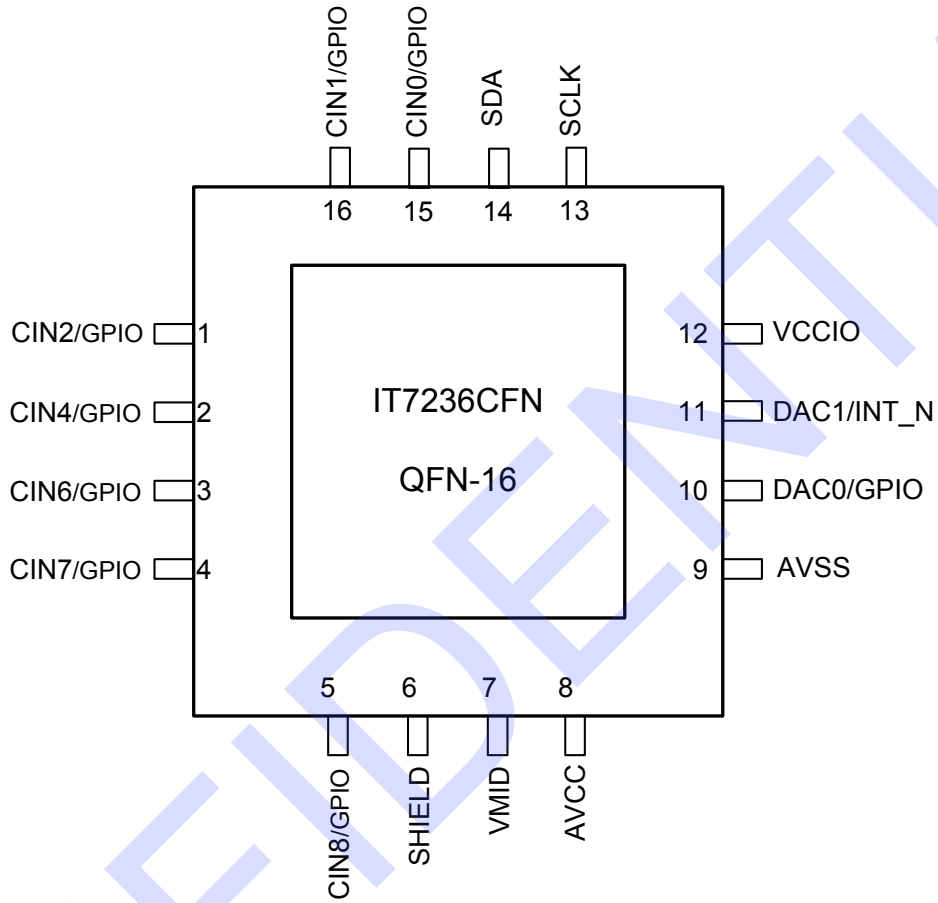
Table 4-3. IT7236CFN Pins Listed in Numeric Order (16-pin QFN)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CIN2/GPIO	5	CIN8/GPIO	9	AVSS	13	SCLK
2	CIN4/GPIO	6	SHIELD	10	DAC0/GPIO	14	SDA
3	CIN6/GPIO	7	VMID	11	DAC1/INT_N	15	CIN0/GPIO
4	CIN7/GPIO	8	AVCC	12	VCCIO	16	CIN1/GPIO

5. Pin Description

Table 5-1. Pin Description of Capactiance Sensor Related Pins

Signal	Attribute	Description
Capacitance Sensor Related Pins (Analog I/F)		
CIN*/GPIO	AI	*Capacitance Sensor Input Channels/ General-Purpose IO* These inputs are used to sense the capacitance values. They can be companioned with capacitance sensors to implement functions such as buttons, scroll bars, and wheels. Besides, their function can be switched to general-purpose input/output (GPIO) by setting the internal control registers. The voltage levels of these GPIOs are decided by the AVCC power.
VMID	AI	*Bias Voltage* This pin must be connected to ground with one 0.1uF capacitor to supply one bias voltage.
SHIELD	AO	*CDC Active Shield Output* This pin must be connected to the external plane.

Table 5-2. Pin Description of Digital-to-Analog Output

Signal	Attribute	Description
Digital-to-Analog Output Pins (Digital I/F)		
DAC0/GPIO	IOK16	*DAC Output 0/General-Purpose IO* This pin will output the analog voltage level corresponding to the programming digital value. Besides, its function can be switched to general-purpose input/output (GPIO) by setting the internal control registers. The voltage levels of these GPIOs are decided by the VCCIO power.
DAC1/INT_N	IOK16	*DAC Output 1/Interrupt* This pin will output the analog voltage level corresponding to the programming digital value. Besides, its function can be switched to interrupt output function by setting the internal control registers.

Table 5-3. Pin Description of General Purpose Input/Output

Signal	Attribute	Description
General Purpose Input/Output Pins (Digital I/F)		
GPIO*	IOK16	*General Purpose Input/Output* These pins are dedicated to the general-purpose input/output function. The voltage levels of these GPIOs are decided by the VCCIO power.

Table 5-4. Pin Description of I²C Interface

Signal	Attribute	Description
I2C Interface Pins (Digital I/F)		
ADDR0	IK	*I²C Address Select Bit 0* This pin is used to specify the decoded address of this chip.
SCLK	IOK16	*I²C Clock*
SDA/GPIO7	IOK16	*I²C Data/ General Purpose IO* The pin is used to be the I2C SDA function. Besides, its function can be switched to general-purpose input/output (GPIO) and the voltage level is decided by the VCCIO power.

Table 5-5. Pin Description of Power/Ground Signals

Signal	Attribute	Description
Power/Ground Pins (Analog I/F)		
VCCIO	I	*Power for Digital Component and IO Pad (1.62~5.5V)*
AVSS	I	*Analog Ground for Analog Component*
AVCC	I	*Analog Power for Analog Component (2.25~5.5V)*

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
AO: Analog Output PAD.
IOK16: 16 mA Bidirectional PAD with Schmitt Trigger Input PAD.

6. Serial Interface

6.1 Overview

The chip is available with an I^2C –compatible interface and supports 4 transfer types - single write, burst write, single read, and burst read.

6.2 I2C- Compatible Interface

The chip supports 2-wire I^2C serial interface protocol of the industry standard. It is also compatible with System Management Bus(SMBus) protocol.

6.2.1 Device Address

The chip supports 2 different 7-bit device addresses which are controlled by the ADD0 pin. The related device addresses are listed below.

Table 6-1. I^2C Device Address

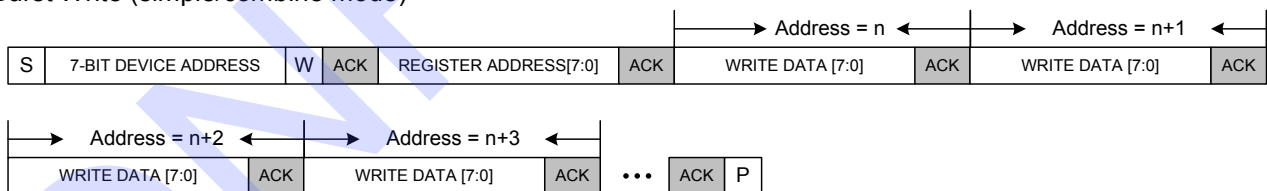| ADD0	I^2C Address
0	1000 110
1	0110 101

6.2.2 Data Transfer

Data is transferred over the I^2C bus in 8-bit address and 8-bit data. The chip supports the following 4 transfer types. The related protocol and timing diagrams are shown below.

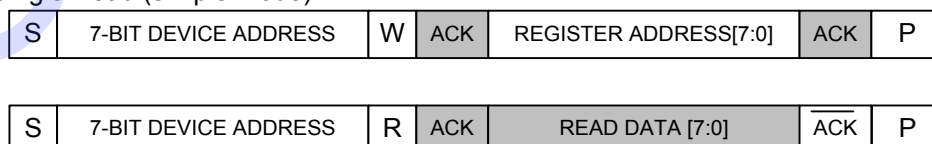Single Write (simple/combine mode)

S	7-BIT DEVICE ADDRESS	W	ACK	REGISTER ADDRESS[7:0]	ACK	WRITE DATA [7:0]	ACK	P

Burst Write (simple/combine mode)

						→ Address = n ←		→ Address = n+1 ←	
S	7-BIT DEVICE ADDRESS	W	ACK	REGISTER ADDRESS[7:0]	ACK	WRITE DATA [7:0]	ACK	WRITE DATA [7:0]	ACK

→ Address = n+2 ←		→ Address = n+3 ←				
WRITE DATA [7:0]	ACK	WRITE DATA [7:0]	ACK	•••	ACK	P

Single Read (combine mode)

S	7-BIT DEVICE ADDRESS	W	ACK	REGISTER ADDRESS[7:0]	ACK	SR	7-BIT DEVICE ADDRESS	R	ACK

READ DATA [7:0]	$\overline{ACK}$	P

Single Read (simple mode)

S	7-BIT DEVICE ADDRESS	W	ACK	REGISTER ADDRESS[7:0]	ACK	P

S	7-BIT DEVICE ADDRESS	R	ACK	READ DATA [7:0]	$\overline{ACK}$	P

Burst Read (combine mode)

| S | 7-BIT DEVICE ADDRESS | W | ACK | REGISTER ADDRESS[7:0] | ACK | SR | 7-BIT DEVICE ADDRESS | R | ACK |

Address = n | Address = n+1 | Address = n+2 | Address = n+3

| READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | ••• | $\overline{ACK}$ | P |

Burst Read (simple mode)

| S | 7-BIT DEVICE ADDRESS | W | ACK | REGISTER ADDRESS[7:0] | ACK | P |

Address = n | Address = n+1 | Address = n+2

| S | 7-BIT DEVICE ADDRESS | R | ACK | READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | ••• | $\overline{ACK}$ | P |

S	START BIT		ACK	ACKNOWLEDGE BIT			OUTPUT FROM HOST
P	STOP BIT		$\overline{ACK}$	NO ACKNOWLEDGE BIT			OUTPUT FROM OUR IC
SR	REPEATED START BIT

Note 1:

Special Single Read (simple mode)

| S | 7-BIT DEVICE ADDRESS | W | ACK | REGISTER ADDRESS[7:0] | ACK | P |

| S | 7-BIT DEVICE ADDRESS | R | ACK | READ DATA [7:0] | $\overline{ACK}$ | P |

Same READ DATA

| S | 7-BIT DEVICE ADDRESS | R | ACK | READ DATA [7:0] | $\overline{ACK}$ | P |
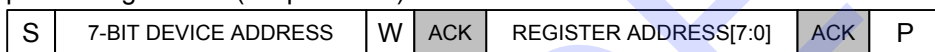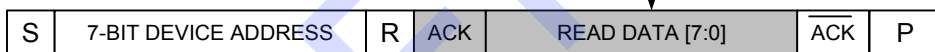
Special case: If a normal single read of simple mode is followed by the repeated read part of the normal single read of simple mode, the first read data is the same as that of the second owing to their identical register address.

Note 2:

Special Write/Read

Address = n

| S | 7-BIT DEVICE ADDRESS | W | ACK | REGISTER ADDRESS[7:0] | ACK | WRITE DATA [7:0] | ACK |

Address = n+1 | Address = n+2

| WRITE DATA [7:0] | ACK | WRITE DATA [7:0] | ACK | ••• | ACK | SR |

Address = n | Address = n+1

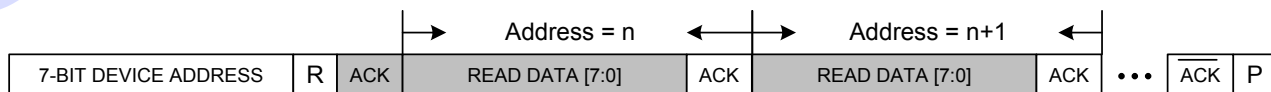| 7-BIT DEVICE ADDRESS | R | ACK | READ DATA [7:0] | ACK | READ DATA [7:0] | ACK | ••• | $\overline{ACK}$ | P |
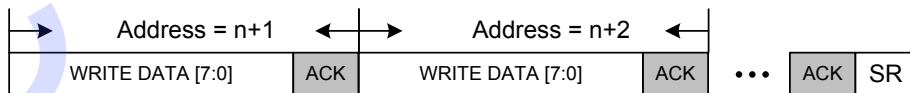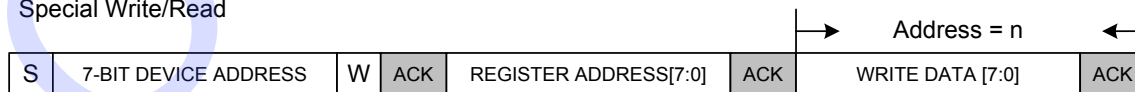
Figure 6-1. Example of I²C Timing for Single Register Write/Read Operation

I2C Write

I2C Read
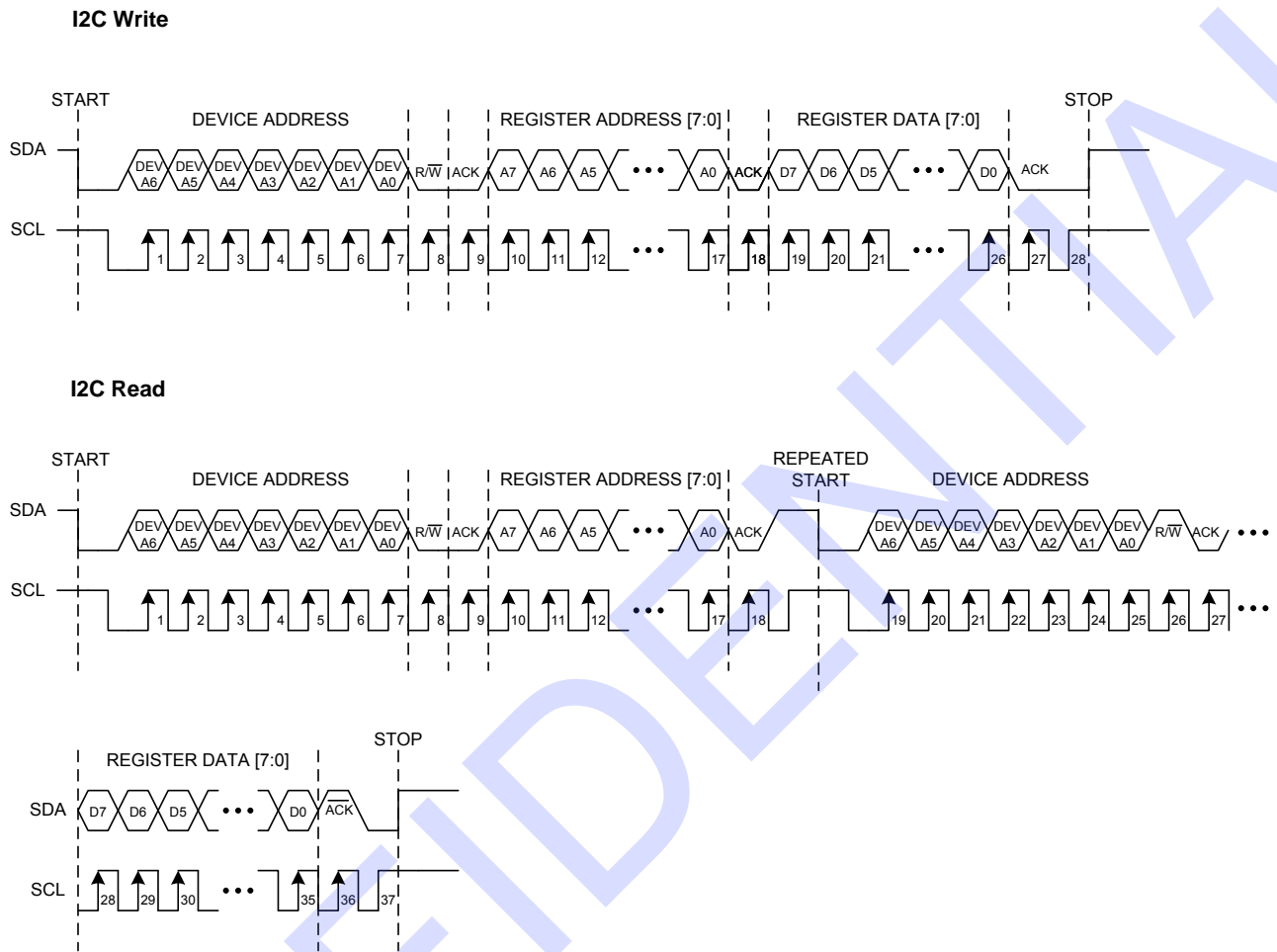
6.2.3 Timeouts

The I²C interface supports a timeout reset mechanism to prevent I²C bus halt due to any abnormal transaction. If SCL is low over 4ms, the I²C interface will reset itself and be ready to receive a new command.
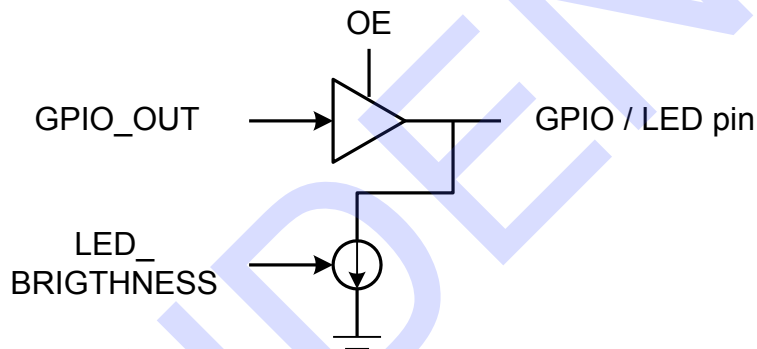
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7. General Purpose I/O Port

7.1 Overview

Some pins of this chip provide the multi-function to meet the diversity of system requirements. They can be programmed to switch up to 23 additional General purpose Input/Output (GPIO) pins (14 CIN + 8 GPIO + DAC0), or up to 10 LED driving output pins (8 GPIO +DAC0 +DAC1) in this chip. The GPIO1~4 and GPIO6 can be programmed as the digital I/O mode or LED driving mode. The CIN0 ~ 13 can be programmed as the digital I/O mode or CIN mode. In the digital I/O mode, each pin can be programmed with different directions independently. Besides, GPIO function provides interrupt related registers when the GPIO pin is used as an interrupt pin. In CIN mode, each pin is used to sense capacitance values. They can be companioned with capacitance sensors to implement functions such as buttons, scroll bars, and wheels. In the LED driving mode, each pin can be programmed to drive different currents by the corresponding internal control registers.
The voltage levels of these CIN0 ~ 13 input or the GPIO function at these CIN pads are limited to the AVCC while the input and output voltage levels at these GPIO pads are limited to the VCCIO.

Figure 7-1. A PWM-Based Current Control LED Driving Pad

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8. DC Characteristics

Absolute Maximum Ratings

Power Supply (VCCIO) .... -0.3V to 5.5V

Power Supply (AVCC) .... -0.3V to 3.6V

Digital Input Voltage .... -0.3V to VCCIO + 0.3V

Digital Output Voltage .... -0.3V to VCCIO + 0.3V

Analog Input Voltage .... -0.3V to AVCC + 0.3V

Operation Temperature .... -40°C to 85°C

Storage Temperature .... -40°C to 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition VCCIO=3.0V~3.6V, Ta=-25°C ~85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS	-	-	0.3*VCCIO	V
V_{IH}	Input High Voltage	CMOS	0.7*VCCIO	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	-	1.80	-	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	-	2.10	-	V
V_{OL}	Output Low Voltage	I_{OL}=2mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=2mA	2.4	-	-	V
R_I	Input Pull-up Resistance	V_{IL}=0V or V_{IH}=VCCIO	-	75	-	KΩ
I_{IL}	Input Leakage Current	no pull-up	-1	-	1	uA
I_{OZ}	Tri-state Leakage Current		-1	-	1	mA
C_{IN}	Input Capacity		-	10	-	pF
C_{OUT}	Output Capacity		-	10	-	pF
C_{BID}	Bi-directional Buffer Capacity		-	10	-	pF

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9. AC Characteristics
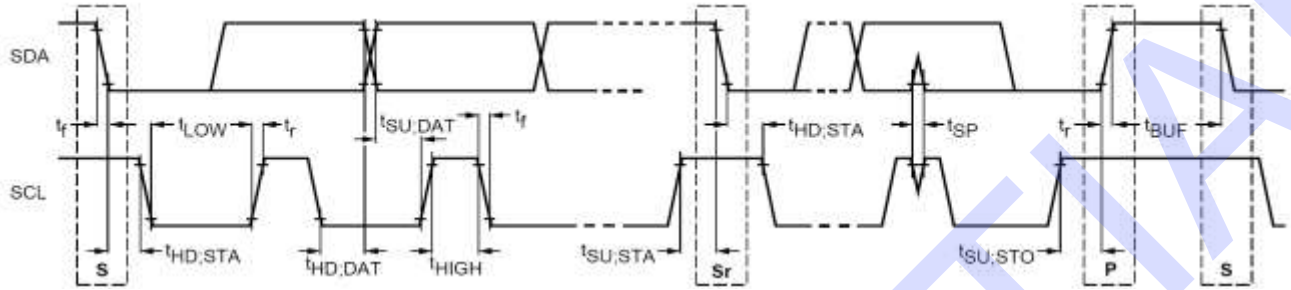
Figure 9-1. Definition of Timing for I²C Interface

Table 9-1. I²C AC Characteristic

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	1	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	-	us
t_{LOW}	LOW period of the SCL clock	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	0.6	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6	-	us
$t_{HD;DAT}$	Data hold time	0	0.9	us
$t_{SU;DAT}$	Data set-up time	100	-	ns
t_r	Rise time of both SDA and SCL signals	$20+0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V
$t_{timeout}$	Cumulative SCL low timeout limit	3	5	ms

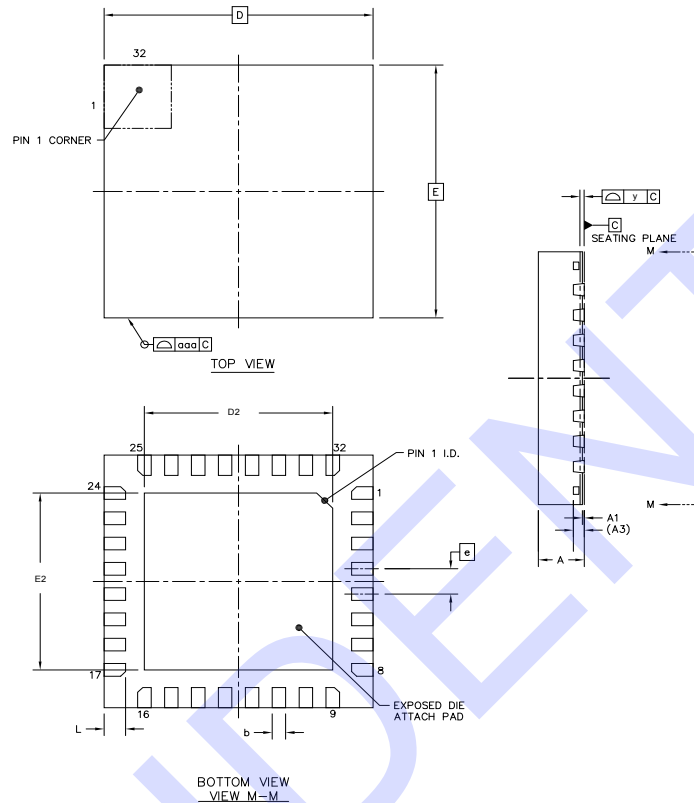This page is intentionally left blank.

10. Package Information

QFN 32L Outline Dimensions   unit: inches/mm

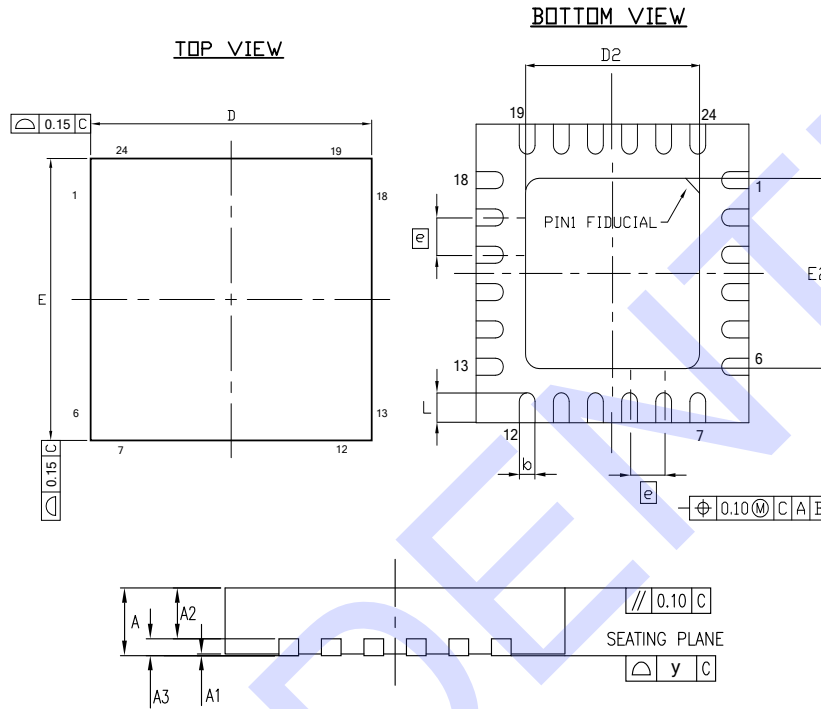| Symbol	Dimensions in inches			Dimensions in mm		
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**
A	0.030	0.033	0.035	0.75	0.85	0.90
A1	0.000	---	0.002	0.00	---	0.05
A3	0.008 REF			0.203 REF		
b	0.007	0.01	0.012	0.18	0.25	0.30
D	0.197BSC			5.00 BSC		
D2	0.124	---	0.142	3.15	---	3.60
E	0.197BSC			5.00BSC		
E2	0.124	---	0.142	3.15	---	3.60
e	0.020 BSC			0.50 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45
y	--	--	0.003	--	--	0.08

Notes:
1. Controlling dimension：Millimeter
2. Reference document：JEDEC MO-220.3. Take SMT into consideration, please use the minimum number of D2's And E2's dimensions.

DI-SAW-QFN32(5*5)v0

QFN 24L Outline Dimensions   unit: inches/mm

Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.030	--	0.035	0.76	--	0.9
A1	0.000	0.0008	0.0019	0.00	0.02	0.05
A2	0.022	--	0.028	0.57	--	0.70
A3	0.008 REF			0.20 REF		
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.157 BSC			4.00 BSC		
D2	0.094	----	0.106	2.40	---	2.70
E	0.157 BSC			4.00 BSC		
E2	0.094	---	0.106	2.40	---	2.70
e	0.020 BSC			0.50 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45
y	--	--	0.003	--	--	0.08

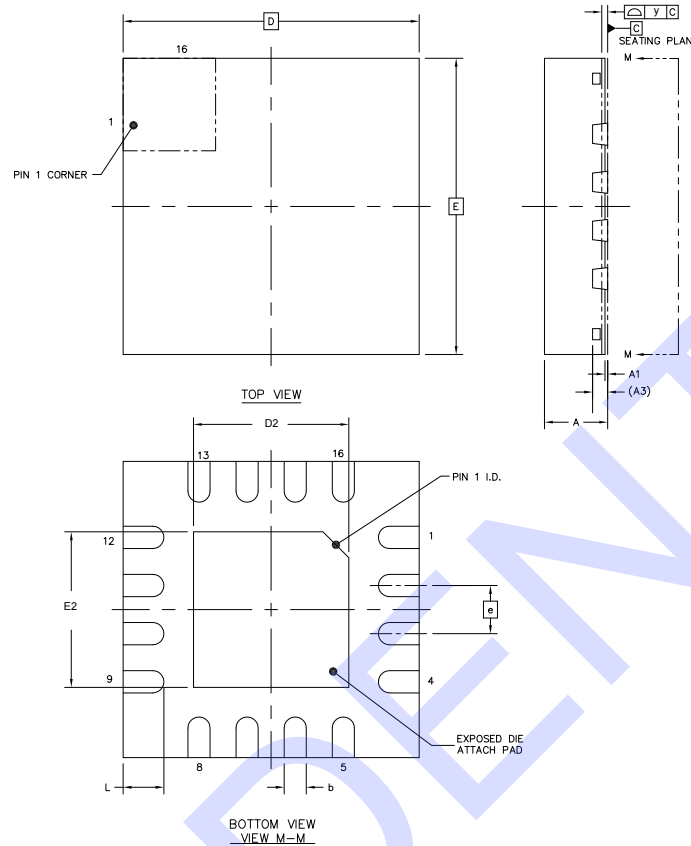**Notes:**
1. Controlling dimension：Millimeter
2. Reference document：JEDEC MO-220.

DI-SAW-QFN24(4*4)v4

QFN 16L Outline Dimensions   unit: inches/mm

TOP VIEW

SEATING PLANE

BOTTOM VIEW
VIEW M—M

Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	---	0.002	0.00	---	0.05
A3	0.008 REF			0.203 REF		
b	0.010	0.012	0.014	0.25	0.30	0.35
D	0.157BSC			4.00 BSC		
D2	0.079	---	0.087	2.00	---	2.20
E	0.157BSC			4.00BSC		
E2	0.079	---	0.087	2.00	---	2.20
e	0.026 BSC			0.65 BSC		
L	0.020	0.022	0.024	0.50	0.55	0.60
y	--	--	0.003	--	--	0.08

Notes:
1. Controlling dimension：Millimeter
2. Reference document：JEDEC MO-220.
3. Take SMT into consideration, please use the minimum number of D2's And E2's dimensions.

DI-SAW-QFN16(4*4)v0

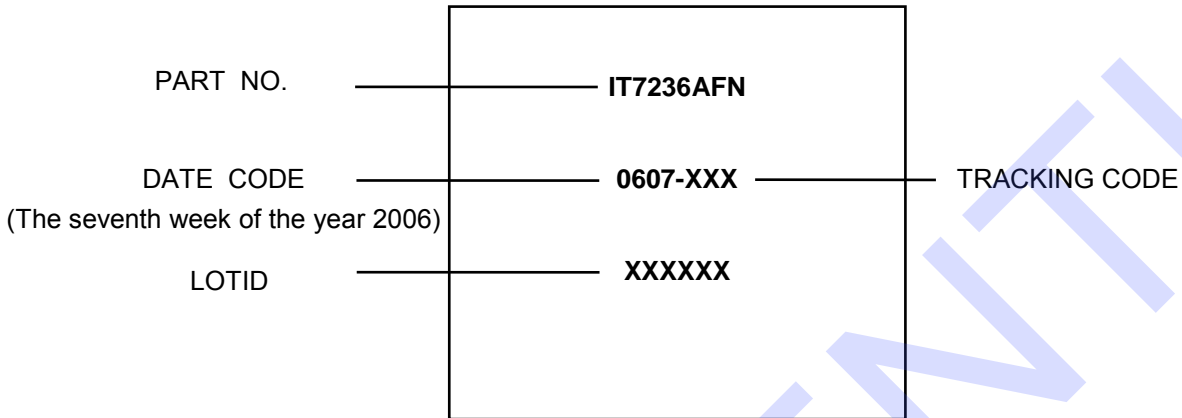This page is intentionally left blank.

11. Ordering Information

Part No.	Package
IT7236AFN/AX	32-pin 5*5 0.9mm QFN
IT7236BFN/AX	24-pin 4*4 0.9mm QFN
IT7236CFN/AX	16-pin 4*4 0.9mm QFN

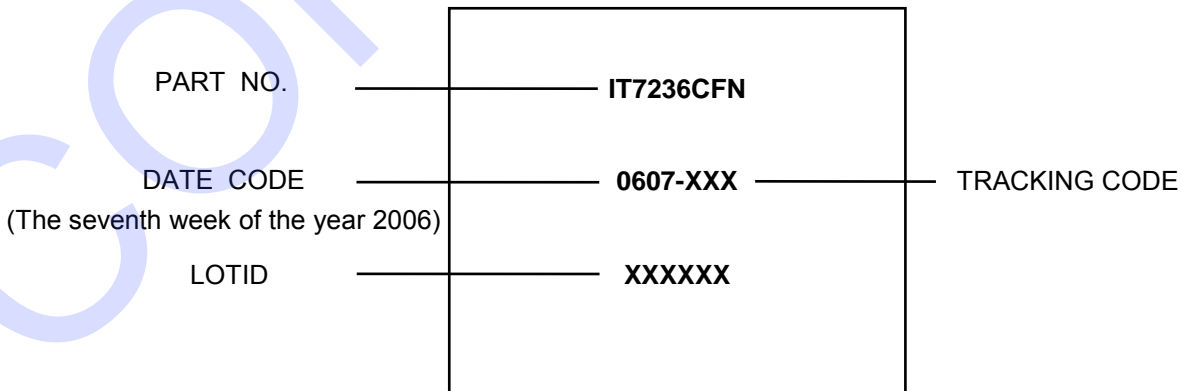This page is intentionally left blank.

12. Top Marking Information

a. IT7236AFN (QFN32)

PART NO. ——————————— **IT7236AFN**

DATE CODE ——————————— **0607-XXX** ——————————— TRACKING CODE
(The seventh week of the year 2006)

LOTID ——————————— **XXXXXX**

b. IT7236BFN (QFN24)

PART NO. ——————————— **IT7236BFN**

DATE CODE ——————————— **0607-XXX** ——————————— TRACKING CODE
(The seventh week of the year 2006)

LOTID ——————————— **XXXXXX**

c. IT7236CFN (QFN16)

PART NO. ——————————— **IT7236CFN**

DATE CODE ——————————— **0607-XXX** ——————————— TRACKING CODE
(The seventh week of the year 2006)

LOTID ——————————— **XXXXXX**

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)
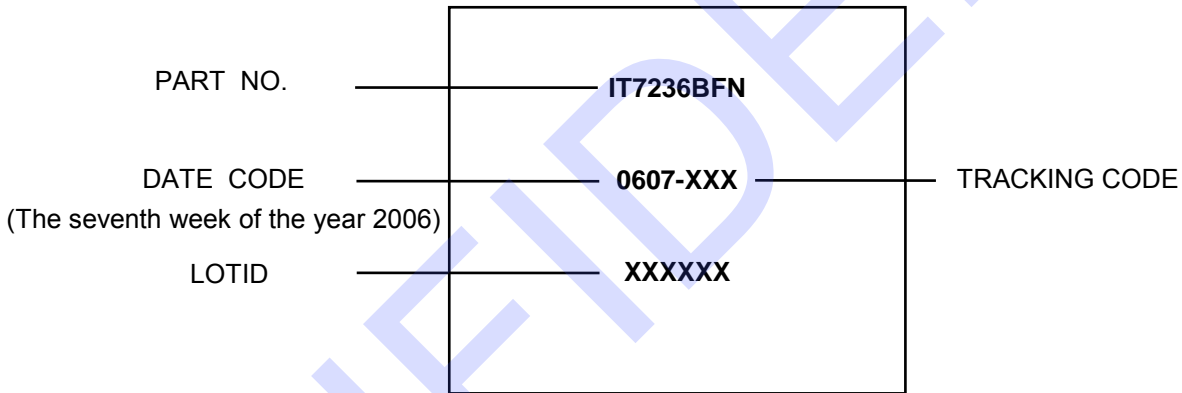
0. **PARTIES**
ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. **ACCEPTANCE OF TERMS**
BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. **DELIVERY**
(a)   Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b)   Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c)   Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. **TERMS OF PAYMENT**
(a)   Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b)   Seller reserves the right to change credit terms at any time in its sole discretion.

4. **LIMITED WARRANTY**
(a)   Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b)   Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c)   No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d)   This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e)   Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f)   EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. **LIMITATION OF LIABILITY**
(a)   Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b)   THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c)   Buyer will not return any goods without first obtaining a customer return order number.
(d)   AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e)   No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f)   BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. **SUBSTITUTIONS AND MODIFICATIONS**
Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. **CANCELLATION**
The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. **INDEMNIFICATION**
Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. **NO CONFIDENTIAL INFORMATION**
Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. **ENTIRE AGREEMENT**
(a)   These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b)   Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. **APPLICABLE LAW**
The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. **JURISDICTION AND VENUE**
The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. **ATTORNEYS' FEES**
Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.