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IT8783E/F

Environment Control – Low Pin Count Input / Output (EC - LPC I/O)

Preliminary Specification V0.5

(For A Version)

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
Table 5-9	Pin Description of Serial Port 6 Signals ■ The power information of the followings was added: – Pin 85 • RTS6# • GP34 • CIRRX1 – Pin 77 • SOUT6 • GP35	17
Table 5-12	Pin Description of Keyboard Controller Signals ■ The power information of the followings was added: • GP10-13	21
Table 5-16	Pin Description of Miscellaneous Signals ■ The second function for pin 77 was corrected to #SOUT6.	23
8.3.11	GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=00h) ■ The default was modified to 00h.	
Table 8-18	Location Mapping Table ■ GP 60-62 were removed.	80

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FIGURES

TABLES

1. Features

- **Low Pin Count Interface**
  - Complies with Intel Low Pin Count Interface Specification Rev. 1.1
  - Supports LDRQ#, SERIRQ protocols
  - Supports PCI PME# Interfaces

- **ACPI & LANDesk Compliant**
  - ACPI V. 2.0 compliant
  - Register sets compatible with “Plug and Play ISA Specification V. 1.0a”
  - LANDesk 3.X compliant
  - Supports 12 logical devices

- **Enhanced Hardware Monitor**
  - Built-in 8-bit Analog to Digital Converter
  - 3 thermal inputs from either remote thermal resistor or thermal diode or diode-connected transistor, the temperature sensor of the current mode
  - 8 voltage monitor inputs (VBAT measured internally)
  - 1 chassis open detection input with low power Flip-Flop dual-powered by battery or VCCH
  - Watch Dog comparison of all monitored values
  - SST/PECI I/F support
  - H/W Smart fan control

- **Fan Speed Controller**
  - Provides fan on-off and PWM control
  - Supports 3 programmable Pulse Width Modulation (PWM) outputs
  - 128 steps of PWM modes
  - Monitors 3 fan tachometer inputs

- **Six 16C550 UARTs**
  - Supports six standard Serial Ports
  - Supports IrDA 1.0/ASKIR protocols
  - Supports CIR

- **IEEE 1284 Parallel Port**
  - Standard mode: Bi-directional SPP compliant
  - Enhanced mode: EPP V. 1.7 and V. 1.9 compliant
  - High-speed mode: ECP, IEEE 1284 compliant
  - Back-drive current reduction
  - Printer power-on damage reduction
  - Supports POST (Power-On Self Test) Data Port

- **Floppy Disk Controller**
  - Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
  - Enhanced digital data separator
  - 3-Mode drives supported
  - Supports automatic write protection via software

- **Keyboard Controller**
  - 8042 compatible for PS/2 keyboard and mouse
  - Hardware KBC
  - GateA20 and Keyboard reset output
  - Supports multiple keyboard power-on events (Any keys, 2-5 sequential keys, 1-3 simultaneous keys)
  - Supports mouse double-click and/or mouse move power on events

- **40 General Purpose I/O Pins**
  - Input mode supports either switch de-bounce or programmable external IRQ input routing
  - Output mode supports 2 sets of programmable LED blinking periods
  - 8 GPIO Pins in the same group

- **Serial Flash I/F for BIOS**
  - Supports 8 M-bit of SPI I/F
  - Supports H/W lock

- **Watch Dog Timer**
  - Time resolution 1 minute or 1 second, maximum 65535 minutes or 65535 seconds
  - Output to KRST# and PWROK when expired

- **ITE’s Innovative Automatic Power-failure Resume and Power Button De-bounce**

- **VCCH and Vbat Supported**

- **Single 24/48 MHz Clock Input**

- **Built-in 32.768 kHz Oscillator**

- **+5V/3.3V Power Supply**

- **Supports RS485 Automatic Direction Control**

- **Supports Wide Operation Temperature Range: -40℃-100℃**

- **128-pin QFP / 128-pin LQFP**

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2. General Description

The IT8783E/F is a highly integrated Super I/O using the Low Pin Count Interface. It provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, including H/W Monitor and Fan Speed Controller. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.1". The IT8783E/F is ACPI & LANDesk compliant.
The IT8783E/F features an enhanced hardware monitor providing three thermal inputs from remote thermal resistors, or thermal diode or diode-connected transistor (2N3904).

The IT8783E/F contains one Fan Speed Controller, which can control up to three fan speeds through three separate 128 steps of Pulse Width Modulation (PWM) output pins and monitor up to three FANs' Tachometer inputs. It also features six 16C550 UARTs, one IEEE 1284 Parallel Port, one Floppy Disk Controller and one Keyboard Controller.

Integrated in the IT8783E/F are 12 logical devices, which can be individually enabled or disabled via software configuration registers, one high-performance 2.88MB floppy disk controller, with digital data separator, supporting two drives in 360K/ 720K/ 1.2M/ 1.44M/ 2.88M format, one multi-mode high-performance parallel port supporting the bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9), and IEEE 1284 compliant Extended Capabilities Port (ECP), six 16C550 standard compatible enhanced UARTs performing asynchronous communication, and supporting an IR interface. The device also features one fan speed controller controlling and monitoring three fans, six GPIO ports controlling up to 40 GPIO pins, and one integrated Keyboard Controller.

The IT8783E/F utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled, the inputs are inhibited with the clock disabled and the outputs are tri-stated. The device requires a single 24/48 MHz clock input and operates with +5V/3.3V power supply. The IT8783E/F is available in 128-pin LQFP / 128-pin QFP.

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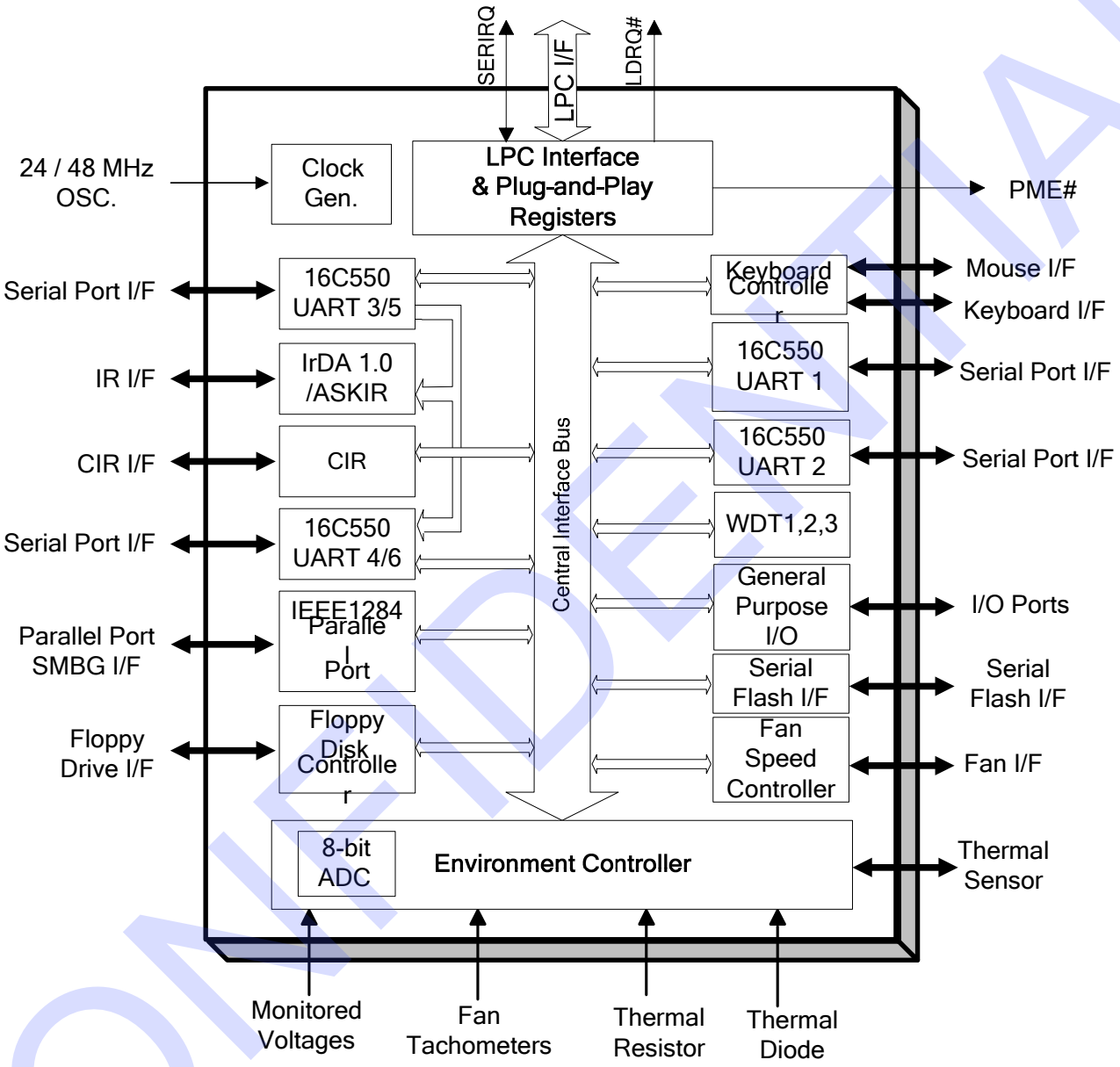
3. Block Diagram



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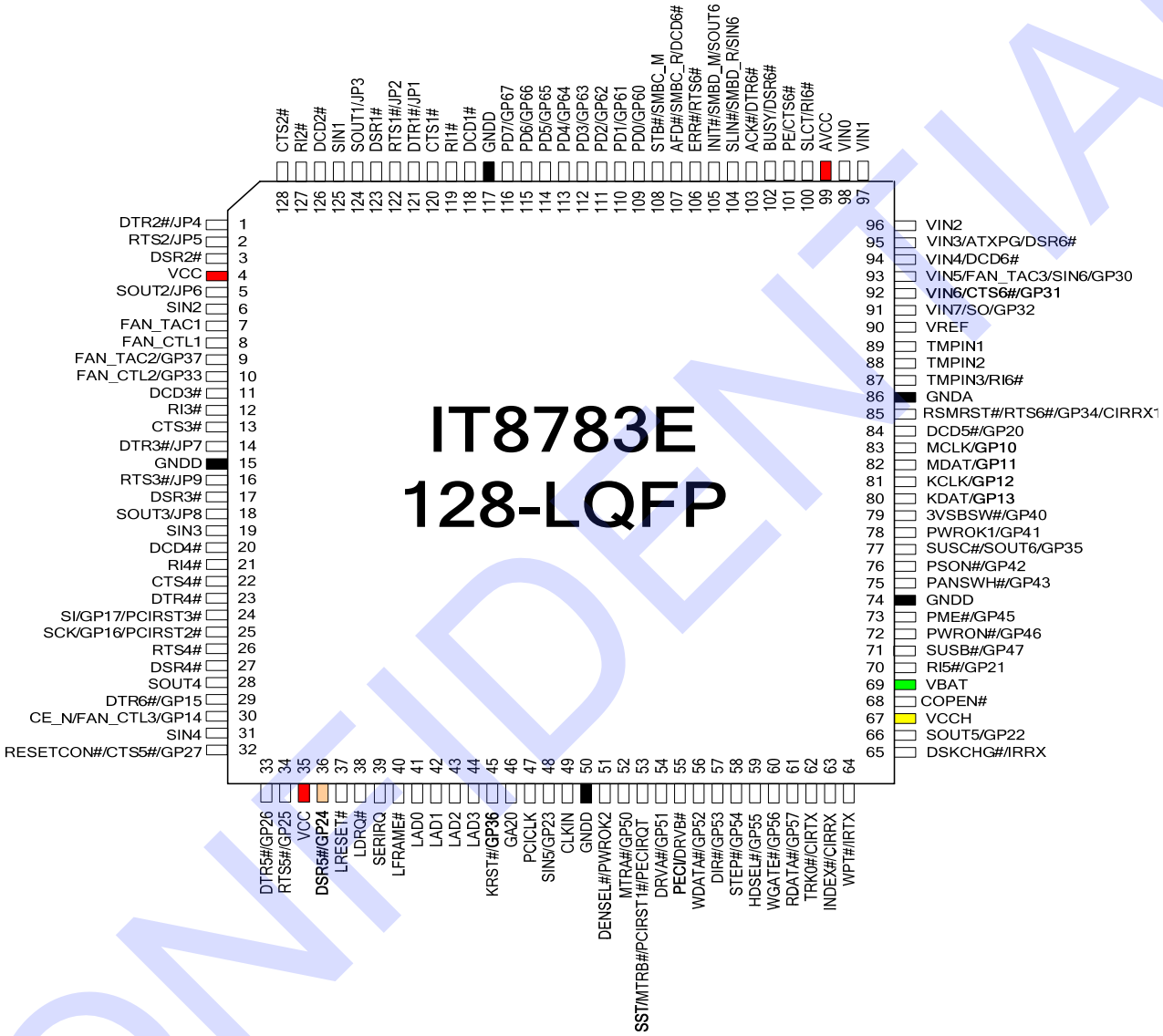
4. Pin Configuration

IT8783E Top View



IT8783F Top View

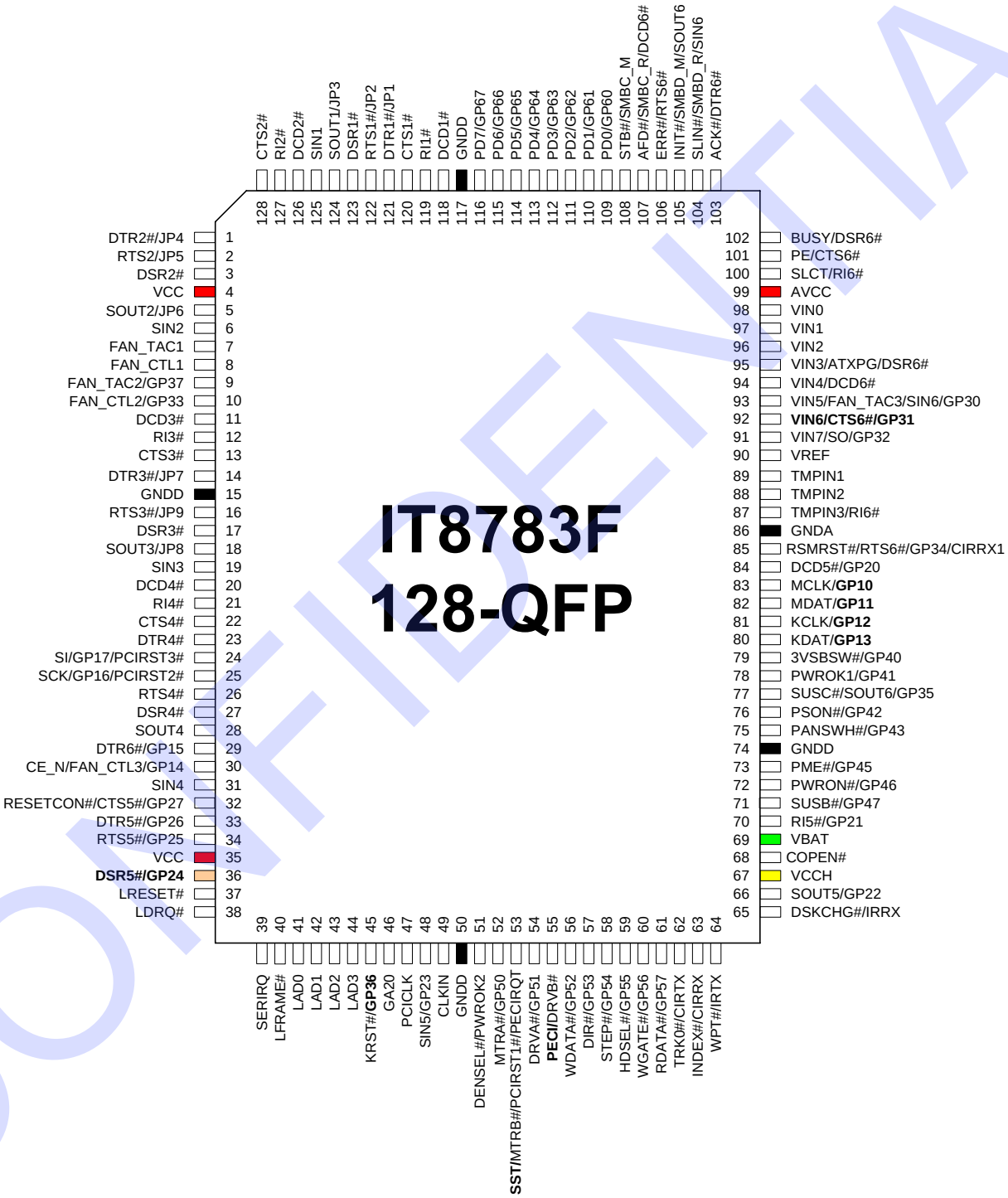


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DTR2#/JP4	33	DTR5#/GP26	65	DSKCHG#/IRRX	97	VIN1
2	RTS2/JP5	34	RTS5#/GP25	66	SOUT5//GP22	98	VIN0
3	DSR2#	35	VCC	67	VCCH	99	AVCC
4	VCC	36	DSR5#/GP24	68	COPEN#	100	SLCT/RI6#
5	SOUT2/JP6	37	LRESET#	69	VBAT	101	PE/CTS6#
6	SIN2	38	LDREQ#	70	RI5#/I/GP21	102	BUSY/DSR6#
7	FAN_TAC1	39	SERIRQ	71	SUSB#/GP47	103	ACK#/DTR6#
8	FAN_CTL1	40	LFRAME#	72	PWRON#/GP46	104	SLIN#/SMBD_R/SIN6
9	FAN_TAC2/GP37	41	LAD0	73	PME#/GP45	105	INIT#/SMBD_M/SOUNT6
10	FAN_CTL2/GP33	42	LAD1	74	GNDD	106	ERR#/RTS6#
11	DCD3#	43	LAD2	75	PANSWH#/GP43	107	AFD#/SMBC_R/DCD6#
12	RI3#	44	LAD3	76	PSON#/GP42	108	STB#/SMBC_M
13	CTS3#/	45	KRST#/GP36	77	SUSC#/SOUT6#/GP35	109	PD0/GP60
14	DTR3#/JP7	46	GA20	78	PWROK1/GP41	110	PD1/GP61
15	GNDD	47	PCICLK	79	3VSBSW#/GP40	111	PD2/GP62
16	RTS3#/JP9	48	SIN5#/GP23	80	KDAT/GP13	112	PD3/GP63
17	DSR3#/	49	CLKIN	81	KCLK/GP12	113	PD4/GP64
18	SOUT3/JP8	50	GNDD	82	MDAT/GP11	114	PD5/GP65
19	SIN3/	51	DENSEL#/PWROK2	83	MCLK/GP10	115	PD6/GP66
20	DCD4#/	52	MTRA#/GP50	84	DCD5#/GP20	116	PD7/GP67
21	RI4#/	53	SST/MTRB#/PCIRST1#/PECIRQT	85	RSMRST#/RTS6#/GP34/CIRRX1	117	GNDD
22	CTS4#/	54	DRVA#/GP51	86	GNDA	118	DCD1#
23	DTR4#/	55	PECI/DRVB#	87	TMPIN3/RI6#	119	RI1#
24	SI/GP17/PCIRST3#	56	WDATA#/GP52	88	TMPIN2	120	CTS1#
25	SCK/GP16/PCIRST2#	57	DIR#/GP53	89	TMPIN1	121	DTR1#/JP1
26	RTS4#	58	STEP#/GP54	90	VREF	122	RTS1#/JP2
27	DSR4#/	59	HDSEL#/GP55	91	VIN7/SO#/GP32	123	DSR1#
28	SOUT4/	60	WGATE#/GP56	92	VIN6/CTS6#/GP31	124	SOUT1/JP3
29	DTR6#/GP15	61	RDATA#/GP57	93	VIN5/FAN_TAC3/SIN6/GP30	125	SIN1
30	CE_N/FAN_CTL3/GP14	62	TRK0#/CIRTX	94	VIN4//DCD6#	126	DCD2#
31	SIN4	63	INDEX#/CIRRX	95	VIN3/ATXPG/DSR6#	127	RI2#
32	RESETCON#/CTS5#/GP27	64	WPT#/IRTX	96	VIN2	128	CTS2#

Table 4-2. Pins Listed in Alphabetical Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
79	3VSBSW#/GP40	106	ERR#/RTS6#	112	PD3/GP63	100	SLCT/RI6#
103	ACK#/DTR6#	8	FAN_CTL1	113	PD4/GP64	104	SLIN#/SMBD_R/SIN6
107	AFD#/SMBC_R/DCD6#	10	FAN_CTL2/GP33	114	PD5/GP65	124	SOUT1/JP3
99	AVCC	7	FAN_TAC1	115	PD6/GP66	5	SOUT2/JP6
102	BUSY/DSR6#	9	FAN_TAC2/GP37	116	PD7/GP67	18	SOUT3/JP8
30	CE_N/FAN_CTL3/GP14	46	GA20	101	PE/CTS6#	28	SOUT4/
49	CLKIN	86	GNDA	55	PECI/DRVB#	66	SOUT5//GP22
68	COPEN#	15	GNDD	73	PME#/GP45	53	SST/MTRB#/PCIRST1#/PECIRQT
120	CTS1#	50	GNDD	76	PSON#/GP42	108	STB#/SMBC_M
128	CTS2#	74	GNDD	78	PWROK1/GP41	58	STEP#/GP54
13	CTS3#/	117	GNDD	72	PWRON#/GP46	71	SUSB#/GP47
22	CTS4#/	59	HDSEL#/GP55	61	RDATA#/GP57	77	SUSC#/SOUT6#/GP35
118	DCD1#	63	INDEX#/CIRRX	32	RESETCON#/CTS5#/GP27	89	TMPIN1
126	DCD2#	105	INIT#/SMBD_M/SOUNT6	119	RI1#	88	TMPIN2
11	DCD3#	81	KCLK/GP12	127	RI2#	87	TMPIN3/RI6#
20	DCD4#/	80	KDAT/GP13	12	RI3#	62	TRK0#/CIRTX
84	DCD5#/GP20	45	KRST#/GP36	21	RI4#/	69	VBAT
51	DENSEL#/PWROK2	41	LAD0	70	RI5#/I/GP21	4	VCC
57	DIR#/GP53	42	LAD1	85	RSMRST#/RTS6#/GP34/CIRRX1	35	VCC
54	DRVA#/GP51	43	LAD2	122	RTS1#/JP2	67	VCCH
65	DSKCHG#/IRRX	44	LAD3	2	RTS2/JP5	98	VIN0
123	DSR1#	38	LDREQ#	16	RTS3#/JP9	97	VIN1
3	DSR2#	40	LFRAME#	26	RTS4#	96	VIN2
17	DSR3#/	37	LRESET#	34	RTS5#/GP25	95	VIN3/ATXPG/DSR6#
27	DSR4#/	83	MCLK/GP10	25	SCK/GP16/PCIRST2#	94	VIN4//DCD6#
36	DSR5#/GP24	82	MDAT/GP11	39	SERIRQ	93	VIN5/FAN_TAC3/SIN6/GP30
121	DTR1#/JP1	52	MTRA#/GP50	24	SI/GP17/PCIRST3#	92	VIN6/CTS6#/GP31
1	DTR2#/JP4	75	PANSWH#/GP43	125	SIN1	91	VIN7/SO#/GP32
14	DTR3#/JP7	47	PCICLK	6	SIN2	90	VREF
23	DTR4#/	109	PD0/GP60	19	SIN3/	56	WDATA#/GP52
33	DTR5#/GP26	110	PD1/GP61	31	SIN4	60	WGATE#/GP56
29	DTR6#/GP15	111	PD2/GP62	48	SIN5#/GP23	64	WPT#/IRTX

5. Pin Description

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35	VCC	PWR	-	***+5V Power Supply***
99	AVCC	PWR	-	***+5V Analog Power Supply***
67	VCCH	PWR	-	***+5V VCC Help Supply***
69	VBAT	PWR	-	***+3.3V Battery Supply***
15, 50, 74, 117	GNDD	GND	-	***Digital Ground***
86	GNDA(D-)	GND	-	***Analog Ground (D-)***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
37	LRESET#	DI	VCC	***LPC RESET #*** EC block will not be reset by LRESET#, which is controlled by VCC PWRGD.
38	LDRQ#	DO16	VCC	***LPC DMA Request #*** An encoded signal for DMA channel select.
39	SERIRQ	DIO16	VCC	***Serial IRQ***
40	LFRAME#	DI	VCC	***LPC Frame #*** This signal indicates the start of the LPC cycle.
41-44	LAD[0:3]	DIO16	VCC	***LPC Address / Data 0-3*** 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
47	PCICLK	DI	VCC	***PCI Clock*** 33 MHz PCI clock input for LPC I/F and SERIRQ.
73	PME#/ GP45	DOD8/ DIOD8	VCCH	***Power Management Event # / General Purpose I/O 45*** • The first function of this pin is the power management event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state. • The second function of this pin is General Purpose I/O Port 4 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Infrared Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
65	DSKCHG#/ IRRX	DI/ DI	VCC	***DSKCHG# / Infrared Receive Input*** • The first function of this pin is FDD disk change input. • The second function of this pin is Infrared Receive Input. The function configuration of this pin is determined by programming the software configuration registers.
64	WPT#/ IRTX	DI/ DO8	VCC	***WPT#/ Infrared Transmit Output*** • The first function of this pin is FDC write protect input. • The second function of this pin is Infrared Transmit Output. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
125	**SIN1**	DI	VCC	***Serial Data Input 1*** This input receives serial data from the communications link.
124	**SOUT1/ JP3**	DO8/ DI	VCC	***Serial Data Output 1 / JP3*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. *During LRESET#, this pin is input for JP3 power-on strapping option.*
123	**DSR1#**	DI	VCC	***Data Set Ready 1 #*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
122	**RTS1#/ JP2**	DO8/ DI	VCC	***Request to Send 1 # / JP2*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during the Loop mode, RTS# is set to its inactive state. The second function of this pin is H/W strapping JP2(at internal VCC OK).
121	**DTR1#/ JP1**	DO8/ DI	VCC	***Data Terminal Ready 1 # / JP1*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. *During LRESET#, this pin is input for JP1 power-on strapping option.*
120	**CTS1#**	DI	VCC	***Clear to Send 1 #*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
119	**RI1#**	DI	VCC	***Ring Indicator 1 #*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
118	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-5. Pin Description of Serial Port 2 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
6	**SIN2**	DI	VCC	***Serial Data Input 2*** This input receives serial data from the communications link.
5	**SOUT2/ JP6**	DO8/ DI	VCC	***Serial Data Output 2 / JP6*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. The second function of this pin is H/W strapping JP6(at internal VCC OK).
3	**DSR2#**	DI	VCC	***Data Set Ready 2 #*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
2	**RTS2#/ JP5**	DO8/ DI	VCC	***Request to Send 2 # / JP5*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. ***The second function of this pin is H/W strapping JP5(at internal VCC OK).***
1	**DTR2#/ JP4**	DO8/ DI	VCC	***Data Terminal Ready 2 # / JP4*** DTR# indicates to the MODEM or data set that the device is ready to exchange data and is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. The second function of this pin is H/W strapping JP4(at internal VCC OK).
128	**CTS2#**	DI	VCC	***Clear to Send 2 #*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	**RI2#**	DI	VCC	***Ring Indicator 2 #*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
126	**DCD2#**	DI	VCC	***Data Carrier Detect 2 #*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-6. Pin Description of Serial Port 3 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
19	**SIN3**	DI	VCC	***Serial Data Input 3*** The function of this pin is to input the serial data received from the communications link.
18	**SOUT3/ JP8**	DO8/ DI	VCC	***Serial Data Output 3/JP8*** • The first function of this pin is to output the sent serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. • The second function of this pin is H/W strapping JP8(at internal VCC OK).
17	**DSR3#**	DI	VCC	***Data Set Ready 3 #*** The function of this pin is Data Set Ready 3#. When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
16	**RTS3#/ JP9**	DO8/ DI	VCC	***Request to Send 3 #/JP9*** • The first function of this pin is Request to Send 3#. When this signal is low, the output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. • The second function of this pin is H/W strapping JP9(at internal VCC OK).
14	**DTR3#/ JP7**	DO8/ DI	VCC	***Data Terminal Ready 3 # / JP7*** • The first function of this pin is Data Terminal Ready 3#, which indicates to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. • The second function of this pin is H/W strapping JP7 The function configuration of this pin is determined by programming the software configuration registers.
13	**CTS3#**	DI	VCC	***Clear to Send 3 #*** The function of this pin is Clear to Send 3 #. When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
12	**RI3#**	DI	VCC	***Ring Indicator 3 #*** The function of this pin is Ring Indicator 3 #. When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
11	**DCD3#**	DI	VCC	***Data Carrier Detect 3 #*** The function of this pin is Data Carrier Detect 3 #. When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-7. Pin Description of Serial Port 4 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
31	**SIN4**	DI	VCC	***Serial Data Input 4*** The function of this pin is to input the serial data received from the communications link.
28	**SOUT4**	DO8	VCC	***Serial Data Output 4*** The function of this pin is to output the sent serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
27	**DSR4#**	DI	VCC	***Data Set Ready 4 #*** The function of this pin is Data Set Ready 4#. When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
26	**RTS4#**	DO8	VCC	***Request to Send 4 #*** The function of this pin is Request to Send 4#. When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
23	**DTR4#**	DO8/	VCC	***Data Terminal Ready 4 #*** The function of this pin is Data Terminal Ready 4#, which indicates to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.
22	**CTS4#**	DI	VCC	***Clear to Send 4 #*** The function of this pin is Clear to Send 4 #. When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
21	**RI4#**	DI	VCC	***Ring Indicator 4 #*** The function of this pin is Ring Indicator 4 #. When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
20	**DCD4#**	DI	VCC	***Data Carrier Detect 4 #*** The function of this pin is Data Carrier Detect 4 #. When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-8. Pin Description of Serial Port 5 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
48	**SIN5/ GP23**	DI/ DIOD8	VCC	***Serial Data Input 5 / General Purpose I/O 23*** • The first function of this pin is Serial Data Input 5. • The second function of this pin is General Purpose I/O Port 2 Bit 3 The function configuration of this pin is determined by programming the software configuration registers.
66	**SOUT5 / GP22**	DO8/ DIOD8	VCC	***SOUT5 / General Purpose I/O 22*** • The first function of this pin is Serial Data Transmit output. • The second function of this pin is General Purpose I/O Port 2 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
36	**DSR5#/ GP24**	DI/ DIOD8	VCC	***Data Set Ready 5# / General Purpose I/O 24*** • The first function of this pin is Data Set Ready 5 #. • The second function of this pin is General Purpose I/O Port 2 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.
34	**RTS5#/ GP25**	DOD8/ DIOD8	VCC	***Request to Send 5# / General Purpose I/O 25*** • The first function of this pin is Request to Send 5#. • The second function of this pin is General Purpose I/O Port 2 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
33	**DTR5#/ GP26**	DOD8/ DIOD8	VCC	***Data Terminal Ready 5# / General Purpose I/O 26*** • The first function of this pin is Data Terminal Ready 5#. • The second function of this pin is General Purpose I/O Port 2 Bit 6. The function configuration of this pin is determined by programming the software configuration registers.
32	**RESETCON#/ CTS5#/ GP27**	DI/ DI/ DIOD8	VCC	***RESETCONNECT / Clear to Send 5#/ General Purpose I/O 27*** • The first function of this pin is RESET# Connect Input. • The second function of this pin is Clear to Send 5#. • The third function of this pin is General Purpose I/O Port 2 Bit 7. The function configuration of this pin is determined by programming the software configuration registers.
70	**RI5#/ GP21**	DI8/ DIOD8	VCC	***Ring Input 5 # / General Purpose I/O 21*** • The first function of this pin is Ring Indicator 5#. • The second function of this pin is General Purpose I/O Port 2 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
84	**DCD5#/ GP20**	DI/ DIOD8	VCC	***Data Carrier Detect 5# / General Purpose I/O 20*** • The first function of this pin is Data Carrier Detect 5#. • The second function of this pin is General Purpose I/O Port 2 Bit 0. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-9. Pin Description of Serial Port 6 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
93	**VIN5/ FAN_TAC3/ SIN6/ GP30**	AI/ DI/ DI/ DI	VCC	***VIN5/FAN Tachometer input 3/Serial Data Input 6/ General Purpose I/O 30*** • The first function of this pin is Analog Voltage CH5 Input. • The second function of this pin is FAN Tachometer Input 3. • The third function of this pin is Serial Data Input 6. • The fourth function of this pin is General Purpose I Port 3 Bit 0 (input mode only). The function configuration of this pin is determined by programming the software configuration registers.
92	**VIN6/ CTS6#/ GP31**	DO/ DI/ DI	VCC	***VIN6/CTS6#/General Purpose I/O 31*** • The first function of this pin Analog Voltage CH6 Input • The second function of this pin is CTS6# Input. • The third function of this pin is General Purpose I Port 3 Bit 1(input mode only). The function configuration of this pin is determined by programming the software configuration registers.
85	**RTS6#/ RSMRST#/ GP34/ CIRRX1**	DO/ DOD8/ DIOD8/ DI	VCC VCCH VCC VCCH	***Request to Send 6/ Resume Reset # / General Purpose I/O 34 / CIR Receiver input 1*** • The first function of this pin is Request to Send 6. • The second function of this pin is Resume Reset #. It is power good signal of VCCH. The high threshold is 4V ± 0.2V, and the low threshold is 3.5V ± 0.2V. • The third function of this pin is General Purpose I/O Port 3 Bit 4. • The fourth function of this pin is CIR Receiver input 1 The function configuration of this pin is determined by programming the software configuration registers.
95	**VIN3/ ATXPG/ DSR6#**	AI/ DI/ DI	VCC	***VIN3/ATX Power Good/Data Set Ready 6#*** • The first function of this pin is ADC Voltage Input of CH3. • The second function of this pin is ATX Power Good Input. • The third function of this pin is Data Set Ready 6 #. The function configuration of this pin is determined by programming the software configuration registers.
29	**DTR6#/ GP15**	DO8/ DIOD8	VCC	***Data Terminal Ready 6#/General Purpose I/O 15*** • The first function of this pin is Data Terminal Ready 6#. • The third function of this pin is General Purpose I/O Port 1 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
77	**SUSC#/ SOUT6/ GP35**	DI/ DO/ DOD8	VCCH VCC VCC	***SUSC#/SOUT6/Purpose I/O 35*** • The first function of this pin is SUSC# Input • The second function of this pin is Serial Output Data 6. • The third function of this pin is General Purpose I/O Port 3 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
87	**TMPIN3/ RI6#**	AI/ DI8	VCC	***TMPIN3/Ring Indicator 6#*** • The first function of this pin is Thermal input 3. • The second function of this pin is Ring Indicator 6#. The function configuration of this pin is determined by programming the software configuration registers.
94	**VIN4/ DCD6#**	AI/ DI	VCC	***VIN4/Data Carrier Detect 6#*** • The first function of this pin is ADC CH4 Input. • The second function of this pin is Data Carrier Detect 6#. The function configuration of this pin is determined by

Pin(s) No.	Symbol	Attribute	Power	Description
				programming the software configuration registers.

Table 5-10. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	**SLCT/ RI6#**	DI/ DI	VCC	***Printer Select/Ring Indicator 6#*** • The signal of the first function goes high when the line printer has been selected. • The second function of this pin is Ring Indicator 6#.
101	**PE/ CTS6#**	DI/ DI	VCC	***Printer Paper End/Clear to Send 6#*** • The signal of the first function is set high by the printer when it runs out of paper. • The second function of this pin is Clear to Send 6#.
102	**BUSY/ DSR6#**	DI/ DI	VCC	***Printer Busy/Data Set Ready 6#*** The signal of the first function goes high when the line printer has a local operation in progress and cannot accept data. The second function of this pin is Data Set Ready 6#.
103	**ACK#/ DTR6#**	DI/ DO	VCC	***Printer Acknowledge #/Data Terminal Ready 6#*** • The signal of the first function goes low to indicate that the printer has already received a character and is ready to accept another one. • The second function of this pin is Data Terminal Ready 6#.
104	**SLIN#/ SMBD_R/ SIN6**	DIO24/ IO_SW/ DI	VCC	***Printer Select Input #/SMBD_R/Serial Input Data 6*** • The first function of this pin is SLIN#. When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register. • The second function of this pin is SMBus isolation. • The third function of this pin is Serial Input Data 6 .
105	**INIT#/ SMBD_M/ SOUT6**	DIO24/ IO_SW/ DO	VCC	***Printer Initialize #/SMBD_M/ Serial Output Data 6*** • The first function of this pin is INIT#. When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register. • The second function of this pin is SMBus isolation. • The third function of this pin is Serial Output Data 6.
106	**ERR#/ RTS6#**	DI/ DO	VCC	***Printer Error #/ Request to Send 5#*** When the signal is low, it indicates that the printer has encountered an error. The error message can be read from bit 3 of the printer status register. • The second function of this pin is Request to Send 5#.
107	**AFD#/ SMBC_R/ DCD6#**	DIO24/ IO_SW/ DI	VCC	***Printer Auto Line Feed #/SMBC_R/ Data Carrier Detect 6#*** • The first function of this pin is AFD#. When the signal is low, it is derived from the complement of bit 1 of the printer control register and is used to advance one line after each line is printed. • The second function of this pin is SMBus isolation. • The third function of this pin is Data Carrier Detect 6#
108	**STB#/ SMBC_M**	DI/ IO_SW	VCC	***Printer Strobe #/SMBC_M*** • The first function of this pin is STB#. When the signal

Pin(s) No.	Symbol	Attribute	Power	Description
				is low, it is the complement of bit 0 of the printer control register and is used to strobe the printing data into the printer. • The second function of this pin is SMBus isolation.
109-116	**PD[0:7]/ GP60-67**	DIO24/ DIOD8	VCC	***Parallel Port Data [0:7] /General Purpose I/O 60-67*** • The first function of these pins is PD[0:7]. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected. • The second function of these pins is GP60-67.

Table 5-11. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
51	**DENSEL#/ PWROK2**	DO24L/ DOD8	VCC	***FDD Density Select #/PWROK2*** • The first function of this pin is DENSEL#. DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps). • The second function of this pin is Power OK 2. The function configuration of this pin is determined by programming the software configuration registers.
52	**MTRA#/ GP50**	DO24L/ DIOD8	VCC	***FDD Motor A Enable #/ General Purpose I/O 50*** • The first function of this pin is MTRA#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 0.
53	**SST/ MTRB#/ PCIRST1#/ PECIRQT**	SST/ DO24L/ DOD8/ OD	VCC	***External Thermal Sensor Data / FDD Motor B Enable #/ PCIRST1#/PECI Request*** • The first function of this pin is SST. • The second function of this pin is FDD Motor B #. This signal is active low. • The third function of this pin is PCIRST1# Output. • The fourth function of this pin is PECI Request Output. The function configuration of this pin is determined by programming the software configuration registers. When External Thermal Sensor Host is enabled (bit<6:4> of EC Index 0Ah), this pin is selected as SST or ETS_DAT.
54	**DRVA#/ GP51**	DO24L/ DIOD8	VCC	***FDD Drive A Enable #/ General Purpose I/O 51*** • The first function of this pin is DRVA#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 1.
55	**PECI/ DRVB#**	PECI/ DO24L	VCC	***PECI / FDD Drive B Enable #*** • The first function of this pin is PECI. • The second function of this pin is FDD Drive B #. This signal is active low. The function configuration of this pin is determined by programming the software configuration registers.
56	**WDATA#/ GP52**	DO24L/ DIOD8	VCC	***FDD Write Serial Data to the Drive #/ General Purpose I/O 52*** • The first function of this pin is WDATA#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 2.
57	**DIR#/**	DO24L/	VCC	***FDD Head Direction #/ General Purpose I/O 53***

Pin(s) No.	Symbol	Attribute	Power	Description
	GP53	DIOD8		• The first function of this pin is DIR#. Step in when this signal is low and step out when high during a SEEK operation. • The second function of this pin is General Purpose I/O Port 5 bit 3.
58	**STEP#/ GP54**	DO24L/ DIOD8	VCC	***FDD Step Pulse #/General Purpose I/O 54*** • The first function of this pin is STEP#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 4.
59	**HDSEL#/ GP55**	DO24L/ DIOD8	VCC	***FDD Head Select #/General Purpose I/O 55*** • The first function of this pin is HDSEL#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 5.
60	**WGATE#/ GP56**	DO24L/ DIOD8	VCC	***FDD Write Gage Enable #/ General Purpose I/O 56*** • The first function of this pin is WGATE#. This signal is active low. • The second function of this pin is General Purpose I/O Port 5 Bit 6.
61	**RDATA#/ GP57**	DI/ DIOD8	VCC	***FDD Read Disk Data #/ General Purpose I/O 57*** • The first function of this pin is RDATA#. This signal is active low. It is serial data input from FDD. • The second function of this pin is General Purpose I/O Port 5 Bit 7.
62	**TRK0#/ CIRTX**	DI/ DOD8	VCC	***FDD Track 0 # /CIR Transmit Output*** • The first function of this pin is TRK0#. This signal is active low. It indicates that the head of the selected drive is on track 0. • The second function of this pin is Consumer Infrared Transmit Input.
63	**INDEX#/ CIRRX**	DI/ DI	VCC	***FDD Index #/ CIR Receive Input*** • The first function of this pin is INDEX#. This signal is active low. It indicates the beginning of a disk track. • The second function of this pin is Consumer Infrared Receive Input.
64	**WPT#/ IRTX**	DI/ DO8	VCC	***FDD Write Protect #/Infrared Transmit Output*** • The first function of this pin is WPT#. This signal is active low. It indicates that the disk of the selected drive is write-protected. • The second function of this pin is Infrared Transmit Output.
65	**DSKCHG#/ IRRX**	DI/ DI	VCC	***FDD Disk Change #/Infrared Receive Input*** • The first function of this pin is DSKCHG#. This signal is active low. It senses whether the drive door has been opened or a diskette has been changed. • The second function of this pin is Infrared Receive Input.

Table 5-12. Pin Description of Keyboard Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
80	**KDAT/ GP13**	DIOD24/ DIOD24	VCCH VCC	***Keyboard Data/ General Purpose I/O 13*** • The first function of this pin is Keyboard Data. • The second function of this pin is General Purpose I/O Port 1 Bit 3. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
81	**KCLK/ GP12**	DIOD24/ DIOD24	VCCH VCC	***Keyboard Clock/ General Purpose I/O 12*** • The first function of this pin is Keyboard Clock. • The second function of this pin is General Purpose I/O Port 1 Bit 2. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
82	**MDAT/ GP11**	DIOD24/ DIOD24	VCCH VCC	***PS/2 Mouse Data/ General Purpose I/O 11*** • The first function of this pin is PS/2 Mouse Data. • The second function of this pin is General Purpose I/O Port 1 Bit 1. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
83	**MCLK/ GP10**	DIOD24/ DIOD24	VCCH VCC	***PS/2 Mouse Clock/ General Purpose I/O 10*** • The first function of this pin is PS/2 Mouse Clock. • The second function of this pin is General Purpose I/O Port 1 Bit 0. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
45	**KRST#/ GP36**	DO16/ DIOD16	VCC	***Keyboard Reset #/ General Purpose I/O 36*** • The first function of this pin is Keyboard Reset #. • The second function of this pin is General Purpose I/O Port 3 Bit 6. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers.
46	**GA20**	DO16	VCC	***Gate Address 20*** The function of this pin is CPU address 20.

Table 5-13. Pin Description of Hardware Monitor Signals

Pin(s) No.	Symbol	Attribute	Power	Description
98-91	**VIN[0:7]**	AI	AVCC	***Voltage Analog Inputs [0:7]*** The function of these pins is 0 to 4.096V FSR Analog Inputs.
95	**VIN3/ ATXPG/ DSR6#**	AI/ DI/ DI	AVCC	***Voltage Analog Input 3 / ATX Power Good/ Data Set Ready 6#*** • The first function of this pin is 0 to 4.096V Analog Inputs. • The second function of this pin is Power Good Input #. PWROK1/2 will be (VCC power-level-detect **AND** RESETCON# **AND** SUSB# **AND** ATXPG) if bit0 of Index 2Ch is 1, or (VCC power-level-detect **AND** RESETCON# **AND** SUSB#) if 0. • The third function of this pin is DSR6#. The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
90	**VREF**	AO	AVCC	***Reference Voltage Output*** Regulated and referred voltage for three external temperature sensors and negative voltage monitor.
89-88	**TMPIN[1:2]**	AI	AVCC	***External Thermal Inputs [1:2]*** These pins are connected to thermistors [1:2] or thermal temperature sensors.
87	**TMPIN3** **RI6#**	AI/ DI	AVCC	***External Thermal Inputs 3/RI6#*** • For the first function, this pin is connected to thermistor 1 or thermal temperature sensor. • The second function of this pin is Ring Input 6.
68	**COPEN#**	DO	VCCH or VBAT	***Case Open Indication #*** ***The function of this pin is Case Open Indication Output.***
7	**FAN_TAC1**	DI	VCC	***Fan Tachometer Input 1*** 0 to +5V amplitude Fan Tachometer Input.
9	**FAN_TAC2**	DI	VCC	***Fan Tachometer Input 2*** 0 to +5V amplitude Fan Tachometer Input.
93	**VIN5/** **FAN_TAC3/** **SIN6/** **GP30**	AI/ DI/ DI/ DI	VCC	***VIN5/FAN Tachometer Input 3/Serial Data Input 6/ General Purpose I/O 30*** • The first function of this pin is Analog Voltage CH5 Input. • The second function of this pin is FAN Tachometer Input 3. • The third function of this pin is Serial Data Input 6. • The fourth function of this pin is General Purpose I Port 3 Bit 0 (input mode only). The function configuration of this pin is determined by programming the software configuration registers.

Table 5-14. Pin Description of Fan Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
8	**FAN_CTL1**	DOD8	VCC	***Fan Control Output 1*** PWM output signal to Fan's FET.
10	**FAN_CTL2**	DOD8	VCC	***Fan Control Output 2*** PWM output signal to Fan's FET.
30	**CE_N/** **FAN_CTL3/** **GP14**	DO/ DOD8/ DIOD8	VCC	***CE_N/FAN Control Output 3 / General Purpose I/O 14*** • The first function of this pin is Flash Chip Select Output. • The second function of this pin is Fan Control Output 3. • The third function of this pin is General Purpose I/O Port 1 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-15. Pin Description of SFI Signals

Pin(s) No.	Symbol	Attribute	Power	Description
24	**SI/ GP17/ PCIRST3#**	DOD8/ DIOD8/ DIOD8	VCC	***Serial Flash Data-In / General Purpose I/O 17/ PCI Reset Output 3#*** • The first function of this pin is Serial Flash Data-In Output. • The second function of this pin is General Purpose I/O Port 1 Bit 7 • The third function of this pin is PCI Reset Output 3#. The function configuration of this pin is determined by programming the software configuration registers.
25	**SCK/ GP16/ PCIRST2#**	DOD8/ DIOD8/ DIOD8	VCC	***Serial Flash Clock / General Purpose I/O 16 / PCI Reset Output 2#*** • The first function of this pin is Serial Clock for Serial Flash. • The second function of this pin is General Purpose I/O Port 1 Bit 6. • The third function of this pin is PCI Reset Output 2#. The function configuration of this pin is determined by programming the software configuration registers.
91	**VIN7/ SO/ GP32**	AI/ DI/ DI	VCC	***VIN7/Serial Flash Data-Out / General Purpose I/O 32*** • The first function of this pin is Analog Voltage CH7 Input. • The second function of this pin is Serial Flash Data-Out Input. • The third function of this pin is General Purpose I Port 3 Bit 2 (input mode only) The function configuration of this pin is determined by programming the software configuration registers.
30	**CE_N/ FAN_CTL3/ GP14**	DO/ DOD8/ DIOD8	VCC	***CE_N/FAN Control Output 3 / General Purpose I/O 14*** • The first function of this pin is Flash Chip Select Output. • The second function of this pin is Fan Control Output 3. • The third function of this pin is General Purpose I/O Port 1 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-16. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	**CLKIN**	DI	VCC	***24 or 48 MHz Clock Input***
71	**SUSB#/ GP47**	DI/ DIOD8	VCCH	***SUSB# Input/ GP47*** • The first function of this pin is SUSB# Input. • The second function of this pin is General Purpose I/O Port 4 Bit 7. The function configuration of this pin is determined by programming the software configuration registers.
72	**PWRON#/ GP46**	DOD8/ DIOD8	VCCH	***Power On Request Output # / General Purpose I/O46*** • The first function of this pin is Power On Request Output #. • The second function of this pin is General Purpose I/O Port 4 Bit 6. The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
73	**PME#/ GP45**	DOD8/ DIOD8	VCCH	***Power Management Event# / General Purpose I/O 45*** • The first function of this pin is P Power Management Event #. • The second function of this pin is General Purpose I/O Port 4 Bit 5. **The function configuration of this pin is determined by programming the software configuration registers.**
75	**PANSWH#/ GP43**	DI/ DIOD8	VCCH	***Main Power Switch Button Input# / General Purpose I/O 43*** • The first function of this pin is Main Power Switch Button Input#. • The second function of this pin is General Purpose I/O Port 4 Bit 3. The function configuration of this pin is determined by programming the software configuration registers.
76	**PSON#/ GP42**	DOD8/ DIOD8	VCCH	***Power Supply On-Off Output # / General Purpose I/O 42*** • The first function of this pin is Power Supply On-Off Control Output #. • The second function of this pin is General Purpose I/O Port 4 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
77	**SUSC#/ SOUT6/ GP35**	DI/ DI/ DIOD8	VCCH VCC VCC	***SUSC# Input /SOUT6/ General Purpose I/O 35*** • The first function of this pin is SUSC# Input. • The second function of this pin is Serial Output Data 6. • The third function of this pin is General Purpose I/O Port 3 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
78	**PWROK1/ GP41**	DOD8/ DIOD8	VCCH	***Power OK1 of VCC / General Purpose I/O 41*** • The first function of this pin is Power OK1 of VCC. • The second function of this pin is General Purpose I/O Port 4 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
79	**3VSBSW#/ GP40**	DO8/ DIOD8	VCCH	***3VSBSW# / General Purpose I/O 40*** • The first function of this pin is 3VSBSW#. • The second function of this pin is General Purpose I/O Port 4 Bit 0. The function configuration of this pin is determined by programming the software configuration registers.

Note 1: In addition to providing a highly integrated chip, ITE also implements a “SmartGuardian Utility” hardware monitoring application, providing a total solution for customers. The “SmartGuardian Utility” and the application note on the hardware monitoring circuit (the functional arrangement of VIN0-7, TMPIN1-3, FAN_TAC1-3 and FAN_CTL1-3) are interdependent. That is to say, the “SmartGuardian Utility” is accurate only when programmed according to the application note on the hardware monitoring circuit. ITE strongly recommends customers follow the referenced application circuit of IT8783E/F to reduce the “time-to-market” schedule.

Pin No.	Symbol	Recommended Function Arrangement
98	VIN0	2 Volt for VCORE1 of CPU
97	VIN1	2 Volt for VCORE2 of CPU
96	VIN2	-5 Volt for system

95	VIN3	3.3 Volt for system
94	VIN4	+12 Volt for system
93	VIN5	VCC for system
92	VIN6	VBAT for system
91	VIN7	5 Volt for VCCH

IO Cell:
DO8: 8mA Digital Output buffer
DOD8: 8mA Digital Open-Drain Output buffer
DO16: 16mA Digital Output buffer
DO24: 24mA Digital Output buffer
DO24L: 24mA shink/8mA drive Digital Output buffer

DIO8: 8mA Digital Input/Output buffer
DIOD8: 8mA Digital Open-Drain Input/Output buffer
DIO16: 16mA Digital Input/Output buffer
DIOD16: 16mA Digital Open-Drain Input/Output buffer
DIO24: 24mA Digital Input/Output buffer
DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input
AI: Analog Input
AO: Analog Output

SST: special design for SST interface
PECI: special design for PECI interface
IO_SW: special type of input/output; this type of pins are connected in pairs through a switch.

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6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1 (Set 1)

Pin(s) No.	Symbol	Attribute	Description
83	MCLK/ GP10	DIOD24/ DIOD24	*PS/2 Mouse Clock/ General Purpose I/O 10*
82	MDAT/ GP11	DIOD24/ DIOD24	*PS/2 Mouse Data/ General Purpose I/O 11*
81	KCLK/ GP12	DIOD24/ DIOD24	*Keyboard Clock/ General Purpose I/O 12*
80	KDAT/ GP13	DIOD24/ DIOD24	*Keyboard Data/ General Purpose I/O 13*
30	CE_N/ FAN_CTL3/ GP14	DO/ DO/ DIOD8	*CE_N / FAN_CTL3 /General Purpose I/O 14*
29	DTR6#/ GP15	DO/ DIOD8	*DTR6#/General Purpose I/O 15*
25	SCK/ GP16/ PCIRST2#	DOD8/ DIOD8/ DOD	*Serial Flash Clock Output/General Purpose I/O 16/ PCI Reset Output 2#*
24	SI/ GP17/ PCIRST3#	DOD8/ DIOD8/ DOD	*Serial Flash In Data/ General Purpose I/O 17/ PCI Reset Output 3#*

Table 6-2. General Purpose I/O Group 2 (Set 2)

Pin(s) No.	Symbol	Attribute	Description
84	DCD5#/ GP20	DI/ DIOD8	*Data Carrier Detect 5 #/ General Purpose I/O 20*
70	RI5#/ GP21	DI/ DIOD8	*Ring Indicator 5 #/ General Purpose I/O 21*
66	SOUT5/ GP22	DO8/ DIOD8	*Serial Data Output 5 / General Purpose I/O 22*
48	SIN5/ GP23	DI/ DIOD8	*Serial Data Input 5 / General Purpose I/O 23*
36	DSR5#/ GP24	DI/ DIOD8	*Data Set Ready 5 #/ General Purpose I/O 24*
34	RTS5#/ GP25	DO/ DIOD8	*Request to Send 5# / General Purpose I/O 25*
33	DTR5#/ GP26	DO/ DIOD8	*Data Terminal Ready 5#/ General Purpose I/O 26*
32	RESETCON#/ CTS5#/ GP27	DI/ DI/ DIOD8	*RESET Input Connect#/Clear to Send 5#/ General Purpose I/O 27*

Table 6-3. General Purpose I/O Group 3 (Set 3)

Pin(s) No.	Symbol	Attribute	Description
93	VIN5/ FAN_TAC3/ GP30	AI/ DI/ DIOD8	*VIN5/FAN_TAC3 Input/ General Purpose I/O 30*
92	VIN6/ CTS6#/ GP31	AI/ DI/ DIOD8	*VIN6/Clear to Send 6#/ General Purpose I/O 31*
91	VIN7/ SO/ GP32	AI/ DI/ DIOD8	*VIN7/Seral Flash SO Input/ General Purpose I/O 32*
10	FAN_CTL2/ GP33	DOD/ DIOD8	*FAN Control Output 2/ General Purpose I/O 33*
85	RSMRST#/ RTS6#/ GP34/ CIRRX1	DOD8/ DO/ DIOD8/ DI	*Resume Reset Output/Request to Send 6#/ General Purpose I/O 34/ CIR Receive Input 1*
77	SUSC#/ SOUT6#/ GP35	DI/ DO/ DIOD8	*SUSC# Input/Serial Data Output 6# /General Purpose I/O 35*
45	KRST#/ GP36	DO8/ DIOD8	*Keyboard Reset Output# / General Purpose I/O 36*
9	FAN_TAC2/ GP37	DI/ DIOD8	*Fan Tachometer Input 2 / General Purpose I/O 37*

Table 6-4. General Purpose I/O Group 4 (Set 4)

Pin(s) No.	Symbol	Attribute	Description
79	3VSBSW#/ GP40	DO8/ DIOD8	*3VSBSW# / General Purpose I/O 40*
78	DTR6#/ PWROK/ GP41	DOD8/ DO8/ DIOD8	*Data Terminal Ready 6#/Power OK of VCC / General Purpose I/O 41*
76	PSON#/ GP42	DOD8/ DIOD8	*Power Supply On-Off Output# / General Purpose I/O 42*
75	PANSWH#/ GP43	DI/ DIOD8	*Main Power Switch Button Input# / General Purpose I/O 43*
73	PME#/ GP45	DOD8/ DIOD8	*Power Management Event Output# / General Purpose I/O 45*
72	PWRON#/ GP46	DOD8/ DIOD8	*Power On Request Output# / General Purpose I/O 46*
71	SUSB#/ GP47	DI/ DIOD8	*SUSB# Input/ General Purpose I/O 47*

Table 6-5. General Purpose I/O Group 5 (Set 5)

Pin(s) No.	Symbol	Attribute	Description
52	**MTRA#/ GP50**	DO24/ DIOD24	***FDD Motor A Enable# / General Purpose I/O 50***
54	**DRVA#/ GP51**	DO24/ DIOD24	***FDD Drive A Enable# / General Purpose I/O 51***
56	**WDATA#/ GP52**	DO24/ DIOD24	***FDD Write Select to Drive# / General Purpose I/O 52***
57	**DIR#/ GP53**	DO24/ DIOD24	***FDD Head Direction # / General Purpose I/O 53***
58	**STEP#/ GP54**	DO24/ DIOD24	***FDD Step Pulse # / General Purpose I/O 54***
59	**HDSEL#/ GP55**	DO24/ DIOD24	***FDD Head Select # / General Purpose I/O 55***
60	**WGATE#/ GP56**	DIO24/ DIOD24	***FDD Write Gage Enable/ General Purpose I/O 56***
61	**RDATA#/ GP57**	DI/ DIOD24	***FDD Read Disk Data # / General Purpose I/O 57***

Table 6-6. General Purpose I/O Group 6 (Set 6)

Pin(s) No.	Symbol	Attribute	Description
109	**PD0/ GP60**	DIO24/ DIO24	***Parallel Port Data 0 / General Purpose I/O 60***
110	**PD1/ GP61**	DIO24/ DIO24	***Parallel Port Data 1 / General Purpose I/O 61***
111	**PD2/ GP62**	DIO24/ DIO24	***Parallel Port Data 2 / General Purpose I/O 62***
112	**PD3/ GP63**	DIO24/ DIO24	***Parallel Port Data 3 / General Purpose I/O 63***
113	**PD4/ GP64**	DIO24/ DIO24	***Parallel Port Data 4 / General Purpose I/O 64***
114	**PD5/ GP65**	DIO24/ DIO24	***Parallel Port Data 5 / General Purpose I/O 65***
115	**PD6/ GP66**	DIO24/ DIO24	***Parallel Port Data 6 / General Purpose I/O 66***
116	**PD7/ GP67**	DIO24/ DIO24	***Parallel Port Data 7 / General Purpose I/O 67***

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7. Power On Strapping Options

Table 7-1. Power On Strapping Options

	Symbol	Value	Description
JP1 Pin 121	Flashseg1_EN	1	Disable
		0	Flash I/F Address Segment FFF0_0000~FFFF_FFFF & 000E_0000~000F_FFFF is enabled.
JP3 Pin 124	CHIP_SEL	1	When there are two IT8783E/F chips in a system, and CS(bit 7 of configuration select and chip version register) is set to '1', the chip with JP3=1 will be configured and chip with JP3=0 will exit the configuration mode.
		0	When there are two IT8783E/F chips in a system, and CS(bit 7 of configuration select and chip version register) is set to '0', the chip with JP3=0 will be configured and chip with JP3=1 will exit the configuration mode.
JP2 Pin 122	SPI WR LOCK	1	JP2=1; unlock LPC memory/FWM write to Serial Flash
		0	JP2=0; lock LPC memory/FWM write to Serial Flash
JP4 Pin 1	MOVE UART6	1	JP4 =1; pin100-106 for parallel port
		0	JP4=0; move UART6 to pin100~106
JP6 Pin 5	Enable GPIO 5	1	JP6=1; normal FDC function
		0	JP6=0; enable POWROK2
JP8, JP9 Pin18, 16	Enable PCIRST# Out	1	JP8=1; disable PCIRST#1 output JP9=1; disable PCIRST#2, 3 output
		0	JP8=0; enable PCIRST1# output JP9=0; enable PCIRST2, 3# output
JP5, JP7 Pin 2, 14	FAN_CTL_SEL	11	The default value of EC index 15/16/17h is 00h.
		10	The default value of EC index 15/16/17h is 20h.
		01	The default value of EC index 15/16/17h is 40h.
		00	The default value of EC index 15/16/17h is 60h.
JP7 Pin 14	WDT_EN	1	Disable WDT to rest PWROK.
		0	Enable WDT to rest PWROK.

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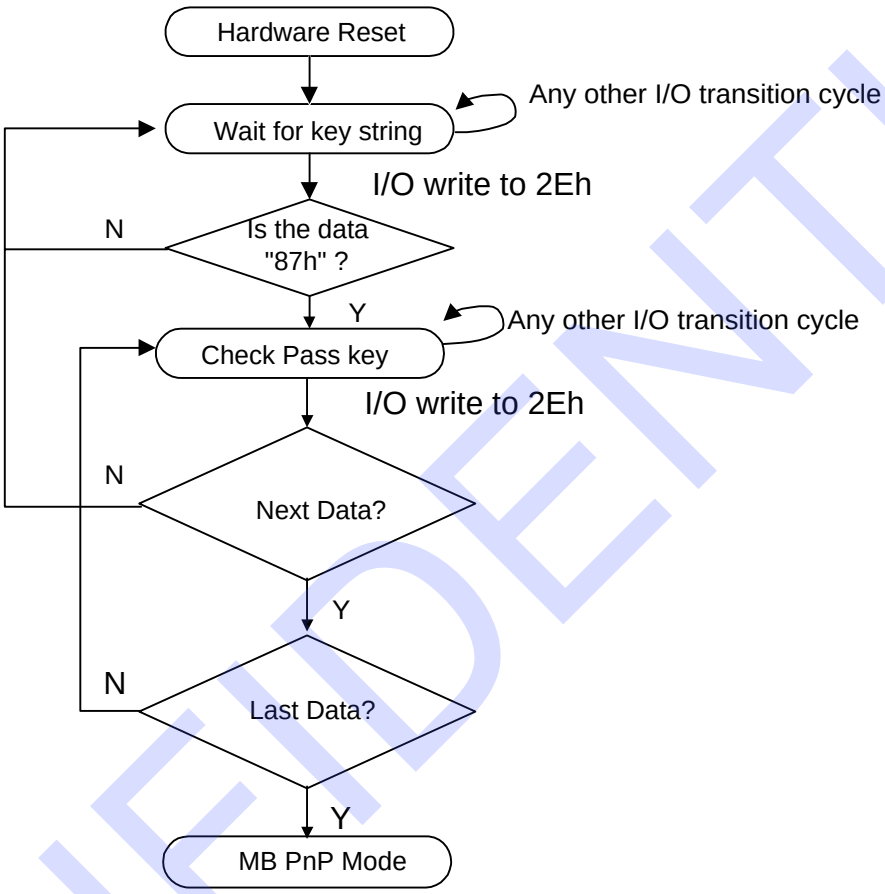
8. Configuration

8.1 Description of Configuring Sequence

After a hardware reset or power-on reset, the IT8783E/F enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is “1”.



There are three steps to completing the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. The undesired result may occur if the MB PnP Mode is not exited properly.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during the Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

		Address port	Data port
	87h, 01h, 55h, 55h;	2Eh	2Fh
or	87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modify the Data of configuration registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to “1” to exit the MB PnP Mode.

8.2 Description of Configuration Registers

All registers except APC/PME' registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	83h	Chip ID Byte 2
All	22h	W-R	00h	Configuration Select and Chip Version
All	23h	R/W	00h	Clock Selection Register
All	0ss0s0s0b	R/W	00h	Software Suspend and Flash I/F Control Register
07h Note1	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register Bit 0 powered by VCCH.
07h Note1	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register Bit 7-0 powered by VCCH.
07h Note1	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h Note1	28h	R/W	00h	GPIO Set 4 Multi-Function Pin Selection Register Bit 7-0 powered by VCCH.
07h Note1	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register Bit 3-5 powered by VCCH.
07h Note1	2Ah	R/W	00h	Extended 1 Multi-Function Pin Selection Register Bit 7-0 powered by VCCH.
All	2Bh	R/W	00h	Logical Block Lock Register
07h Note1	2Ch	R/W	03h	Extended 2 Multi-Function Pin Selection Register Bit 7-0 powered by VCCH.
07h Note1	2Dh	R/W	00h	GPIO Set 6 Enable Register
F4h Note1	2Eh	R/W	00h	Test 1 Register
F4h Note1	2Fh	R/W	00h	Test 2 Register

Note 1: These registers can be read from all LDNs.

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register 1

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select
03h	F0h	R/W	03h Note2	Parallel Port Special Configuration Register

Note 2: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

Table 8-6. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register
04h	F7h	R/W	-	APC/PME Control (PCR 7) Data Register

Table 8-7. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	01h	KBC(Keyboard) Activate
05h	60h	R/W	00h	KBC(Keyboard) Data Base Address MSB Register
05h	61h	R/W	60h	KBC(Keyboard) Data Base Address LSB Register
05h	62h	R/W	00h	KBC(Keyboard) Command Base Address MSB Register
05h	63h	R/W	64h	KBC(Keyboard) Command Base Address LSB Register
05h	70h	R/W	01h	KBC(Keyboard) Interrupt Level Select
05h	71h	R-R/W	02h	KBC(Keyboard) Interrupt Type Note3
05h	F0h	R/W	08h	KBC(Keyboard) Special Configuration Register

Table 8-8. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC(Mouse) Activate
06h	70h	R/W	0Ch	KBC(Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC(Mouse) Interrupt Type Note3
06h	F0h	R/W	00h	KBC(Mouse) Special Configuration Register

Note 3: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

Table 8-9. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	64h	R/W	00h	Serial Flash I/F Base Address MSB Register
07h	65h	R/W	00h	Serial Flash I/F Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer 1 Control Register
07h	72h	R/W	001s0000b	Watch Dog Timer 1 Configuration Register
07h	73h	R/W	38h	Watch Dog Timer 1 Time-out Value (LSB) Register
07h	74h	R/W	00h	Watch Dog Timer 1 Time-out Value (MSB) Register
07h	81h	R/W	00h	Watch Dog Timer 2 Control Register
07h	82h	R/W	001s0000b	Watch Dog Timer 2 Configuration Register
07h	83h	R/W	38h	Watch Dog Timer 2 Time-out Value (LSB) Register
07h	84h	R/W	00h	Watch Dog Timer 2 Time-out Value (MSB) Register
07h	91h	R/W	00h	Watch Dog Timer 3 Control Register

LDN	Index	R/W	Reset	Configuration Register or Action
07h	92h	R/W	001s0000b	Watch Dog Timer 3 Configuration Register
07h	93h	R/W	38h	Watch Dog Timer 3 Time-out Value (LSB) Register
07h	94h	R/W	00h	Watch Dog Timer 3 Time-out Value (MSB) Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	C0h	R/W	01h	Simple I/O Set 1 Enable Register Bit 7-0 powered by VCCH.
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register Bit 7-0 powered by VCCH.
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	40h	Simple I/O Set 4 Enable Register Bit 7-0 powered by VCCH.
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register Bit 7-0 powered by VCCH.
07h	C8h	R/W	01h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	40h	Simple I/O Set 4 Output Enable Register Bit 7-0 powered by VCCH.
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register Bit 7-0 powered by VCCH.
07h	CDh	R/W	00h	Simple I/O Set 6 Output Enable Register Bit 7-0 powered by VCCH.

07h	E0h	R/W	00h	Panel Button De-bounce 0 Input Pin Mapping Register
07h	E1h	R/W	00h	Panel Button De-bounce 1 Input Pin Mapping Register
07h	E2h	R/W	00h	IRQ External Routing 0 Input Pin Mapping Register
07h	E3h	R/W	00h	IRQ External Routing 1 Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ External Routing 1-0 Interrupt Level Selection Registers
07h	EFh	R/W	00001s0	SPI Function Pin Selection Register
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register Bit 7-0 powered by VCCH.
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register Bit 7-0 powered by VCCH.
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register Bit 7-0 powered by VCCH.
07h	FAh	R/W	00h	GP LED Blinking 2 Pin Mapping Register Bit 7-0 powered by VCCH.
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register Bit 7-0 powered by VCCH.
07h	FCh	R/W-R	--h	**Reserved**
07h	FDh	R/W	00h	**Reserved**
07h	FEh	R/W	00h	**Reserved**
07h	FFh	R/W	00h	**Reserved**

Table 8-10. Serial Port 3 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
08h	30h	R/W	00h	Serial Port 3 Activate
08h	60h	R/W	03h	Serial Port 3 Base Address MSB Register
08h	61h	R/W	F8h	Serial Port 3 Base Address LSB Register
08h	70h	R/W	04h	Serial Port 3 Interrupt Level Select
08h	F0h	R/W	00h	Serial Port 3 Special Configuration Register 1
08h	F1h	R/W	50h	Serial Port 3 Special Configuration Register 2

LDN	Index	R/W	Reset	Configuration Register or Action
08h	F2h	R/W	00h	Serial Port 3 Special Configuration Register 3

Table 8-11. Serial Port 4 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
09h	30h	R/W	00h	Serial Port 4 Activate
09h	60h	R/W	02h	Serial Port 4 Base Address MSB Register
09h	61h	R/W	F8h	Serial Port 4 Base Address LSB Register
09h	70h	R/W	04h	Serial Port 4 Interrupt Level Select
09h	F0h	R/W	00h	Serial Port 4 Special Configuration Register 1
09h	F1h	R/W	50h	Serial Port 4 Special Configuration Register 2
09h	F2h	R/W	00h	Serial Port 4 Special Configuration Register 3

Table 8-12. Serial Port 5 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ah	30h	R/W	00h	Serial Port 5 Activate
0Ah	60h	R/W	03h	Serial Port 5 Base Address MSB Register
0Ah	61h	R/W	F8h	Serial Port 5 Base Address LSB Register
0Ah	70h	R/W	04h	Serial Port 5 Interrupt Level Select
0Ah	F0h	R/W	00h	Serial Port 5 Special Configuration Register 1
0Ah	F1h	R/W	50h	Serial Port 5 Special Configuration Register 2
0Ah	F2h	R/W	00h	Serial Port 5 Special Configuration Register 3

Table 8-13. Serial Port 6 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Bh	30h	R/W	00h	Serial Port 6 Activate
0Bh	60h	R/W	02h	Serial Port 6 Base Address MSB Register
0Bh	61h	R/W	F8h	Serial Port 6 Base Address LSB Register
0Bh	70h	R/W	04h	Serial Port 6 Interrupt Level Select
0Bh	F0h	R/W	00h	Serial Port 6 Special Configuration Register 1

Table 8-14. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ch	30h	R/W	00h	Consumer IR Activate
0Ch	60h	R/W	03h	Consumer IR Base Address MSB Register
0Ch	61h	R/W	10h	Consumer IR Base Address LSB Register
0Ch	70h	R/W	0Bh	Consumer IR Interrupt Level Select
0Ch	F0h	R/W	06h	Consumer IR Special Configuration Register

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-15. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	UART1
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	UART2
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST data port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 KBC	Base1 + Base2	KBC
LDN=8, Serial Port 3	Base + (0 -7)	UART3
LDN=9, Serial Port 4	Base + (0 -7)	UART4
LDN=A, Serial Port 5	Base + (0 -7)	UART5
LDN=B, Serial Port 6	Base + (0 -7)	UART6
LDN=C, Consumer IR	Base + (0 -7)	CIR

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, which does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	Returns to the “Wait for Key” state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is **read/write**, which is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This register is Chip ID Byte 1 and is **read only**. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=83h)

This register is Chip ID Byte 2 and is **read only**. Bits [7:0]= 83h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=00h)

Bit	Description
7	**Configuration Select(CS)** This bit is to determine which chip to be configured. The chip with JP3=1 (power-on strapping value of SOUT1) will be configured and chip with JP3=0 will exit the configuration mode when there are two IT8783F/E chips in a system and this bit is written into '1'. Conversely, the chip with JP3=0 (power-on strapping value of SOUT1) will be configured and chip with JP3=1 will exit the configuration mode when this bit is written into '0'.
6-4	**Reserved**
3-0	**Version ID(VID)**

8.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-6	**XLOCK Select(XS)** These two bits determine the XLOCK function. 00: Software XLOCK (default) 01: Reserved 10: Pin 52 (GP50) 11: Pin 9 (GP37)
5	**Reserved**

Bit	Description
4	**Clock Source Select of Watch Dog Timer(CSSWDT)** 0: Internal oscillating clock (Default) 1: External CLKIN
3-2	**Delay Select of PWROK (SDP)** 00: PWROK will be delayed for 300~600ms from VCC5V > 4.0V. 01: PWROK will not be delayed from VCC5V > 4.0V. 10: PWROK will be delayed for 150 ~300ms from VCC5V > 4.0V. 11: Reserved.
1	**Reserved**
0	**CLKIN Frequency(CF)** 0: 48 MHz 1: 24 MHz

8.3.7 Software Suspend and Flash I/F Control Register (Index=24h, Default=0ss0s0s0b, MB PnP)

Bit	Description
7	**Reserved** (Must be 0)
6	**PCIRST2/3# Selection** 0: Disable PCIRST2/3# output 1: Pin 25/24 The initial value of this bit is set to “1” when JP9 pull-down at internal VCC is OK, and PCIRST#2 is output from pin 25, PCIRST#3 is output from pin 24.
5	**Function Selection of Pin 53 (FSP53)** 0: Disable PCIRST#1 1: Enable PCIRST#1 The initial value of this bit is set to “1” when JP8 pull-down at internal VCC is OK, and PCIRST#1 is output to pin 53.
4	**LPC Memory/FWM Write to Serial Flash I/F Enable (LMWSE)** 0: Disable (Default) 1: Enable
3	**Flash I/F Address Segment 3 (FAS3)** Range FFF0_0000h-FFFD_FFFFh, FFFE_0000h-FFFE_FFFFh) 0: Disable 1: Enable
2	**Flash I/F Address Segment 2 (FAS2)** Range (FFEF_0000h-FFEF_FFFFh, FFEE_0000h-FFEE_FFFFh) 0: Disable (Default) 1: Enable
1	**Flash I/F Address Segment 1 (FAS1)** Range (FFFE_0000h_FFFF_FFFFh, 000E_0000h-000F_FFFFh) 0: Disable 1: Enable
0	**Software Suspend (SS)** When bit 0 is set, the IT8783E/F enters the “Software Suspend” state. All the devices, except KBC, remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals RI1# (pin 119) and RI2# (pin 127). 0: Normal 1: Software Suspend

8.3.8 GPIO Set 1 Multi-function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original function. Conversely, if they are set, they will perform the GPIO function. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 24 (FSP)** 0: SI/PCIRST3# If bit 6 of index 24h is "1", pin 24 is PCIRST3# output; otherwise select SI output. 1: General Purpose I/O 17 (GP17)
6	**Function Selection of Pin 25 (FSP)** 0: SCK/PCIRST2# If bit 6 of index 24h is "1", pin 25 is PCIRST2# output; otherwise select SCK output. 1: General Purpose I/O 16 (GP16)
5	**Function Selection of Pin 29 (FSP)** If bit 5 of index 24h is "1", select SO input from this pin; otherwise select DTR6# output. 0: DTR6# 1: General Purpose I/O 15 (GP15)
4	**Function Selection of Pin 30 (FSP)** If bit 1 of index 2Ah is "0" when bit 0 of index EFh is set to "1", pin 30 is CE_N (Default); otherwise select FAN_CTL3. 0: CE_N/FAN_CTL3 1: General Purpose I/O 14 (GP14)
3	**Reserved**
2	**Function Selection of Pin 81, Pin 80 (FSP)** 0: KCLK/KDAT 1: General Purpose I/O 12 (GP12)/1: General Purpose I/O 13 (GP13)
1	**Reserved**
0	**Function Selection of Pin 83, Pin 82 (FSP)** 0: MCLK/MDAT 1: General Purpose I/O 10 (GP10)/General Purpose I/O 11 (GP11)

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original function. Conversely, if they are set, they will perform the GPIO function. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 32 (FSP)** 0: RESETCON#/CTS5# If bit 5 of index 2Ah is set to "1", RESETCON# input will be disabled. 1: General Purpose I/O 27 (GP27) if bit 5 of index 2Ah is set to 1 and bit 3 of index 2Ah is set to 0
6	**Function Selection of Pin 33 (FSP)** 0: DTR5# 1: General Purpose I/O 26 (GP26)
5	**Function Selection of Pin 34 (FSP)** 0: RTS5# 1: General Purpose I/O 25 (GP25)
4	**Function Selection of Pin 36 (FSP)**

Bit	Description
	0: DSR5# 1: General Purpose I/O 24 (GP24)
3	**Function Selection of Pin 48 (FSP)** 0: SIN5# (if bit 3 of index 2Ah is 1) 1: General Purpose I/O 23 (GP23)
2	**Function Selection of Pin 66 (FSP)** 0: SOUT5 (if bit 3 of index 2Ah is 1) 1: General Purpose I/O 22 (GP22)
1	**Function Selection of Pin 70 (FSP)** 0: RI5# 1: General Purpose I/O 21 (GP21)
0	**Function Selection of Pin 84 (FSP)** 0: DCD5# 1: General Purpose I/O 20 (GP20)

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original function. Conversely, if they are set, they will perform the GPIO function. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 9 (FSP)** 0: FAN_TAC2 (Fan Tachometer Input 2) 1: General Purpose I/O 37 (GP37)
6	**Function Selection of Pin 45 (FSP)** 0: KRST# 1: General Purpose I/O 36 (GP36)
5	**Function Selection of Pin 77 (FSP)** 0: SUSC#/SOUT6 If bit 3 of index 2Ch is 1, SOUT6 output is enabled; otherwise select SUSC# input. 1: General Purpose I/O 35 (GP35)
4	**Function Selection of Pin 85 (FSP)** 0: RSMRST#/RTS6# If bit 3 of index 2C is 1, RTS6# output is enabled; otherwise select RSMRST# output. 1: General Purpose I/O 34 (GP34)
3	**Function Selection of Pin 10 (FSP)** 0: FAN_CTL2 1: General Purpose I/O 33 (GP33)
2	**Function Selection of Pin 91 (FSP)** 0: VIN7/SO If bit 2 of index 2Ch is 1, SO input (bit 5 of index24h =0) is enabled; otherwise select VIN7 input. 1: General Purpose I/O 32 (GP32)
1	**Function Selection of Pin 92 (FSP)** 0: VIN6/CTS6# If bit 2 of index 2Ch is 1, CTS6# input is enabled; otherwise select VIN6 input. 1: General Purpose I/O 31 (GP31)
0	**Function Selection of Pin 93 (FSP)** 0: VIN5/FAN_TAC3/SIN6 If bit 2 of index 2Ch is 1, FAN_TAC3/SIN6 input is enabled; otherwise select VIN5 input. 1: General Purpose I/O 30 (GP30)

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original function. Conversely, if they are set, they will perform the GPIO function. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 71 (FSP)** 0: SUSB# 1: General Purpose I/O 47 (GP47)
6	**Function Selection of Pin 72 (FSP)** 0: PWRON# 1: General Purpose I/O 46 (GP46)
5	**Function Selection of Pin 73 (FSP)** 0: PME# 1: General Purpose I/O 45 (GP45)
4	**Reserved** 0: (must be 0) 1: Reserved
3	**Function Selection of Pin 75 (FSP)** 0: Main Power Switch Button Input # (PANSWH#) 1: General Purpose I/O 43 (GP43)
2	**Function Selection of Pin 76 (FSP)** 0: Power Supply On-Off Control Output (PSON#) 1: General Purpose I/O 42 (GP42)
1	**Function Selection of Pin 78 (FSP)** 0: PWROK1 1: General Purpose I/O 41 (GP41)
0	**Function Selection of Pin 79 (FSP)** 0: 3VSBSW# 1: General Purpose I/O 40 (GP40)

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original function. Conversely, if they are set, they will perform the GPIO function. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Function Selection of Pin 61 (FSP)** 0: RDATA# 1: General Purpose I/O 57 (GP57); FDC disabled.
6	**Function Selection of Pin 60 (FSP)** 0: WGATE# 1: General Purpose I/O 56 (GP56); FDC disabled.
5	**Function Selection of Pin 59 (FSP)** 0: HDSEL# 1: General Purpose I/O 55 (GP55); FDC disabled.
4	**Function Selection of Pin 58 (FSP)** 0: STEP# 1: General Purpose I/O 54 (GP54); FDC disabled.

Bit	Description
3	**Function Selection of Pin 57 (FSP)** 0: DIR# 1: General Purpose I/O 53 (GP53); FDC disabled.
2	**Function Selection of Pin 56 (FSP)** 0: WDATA# 1: General Purpose I/O 52 (GP52); FDC disabled.
1	**Function Selection of Pin 54 (FSP)** 0: DRVA# 1: General Purpose I/O 51 (GP51); FDC disabled.
0	**Function Selection of Pin 52 (FSP)** 0: MTRA# 1: General Purpose I/O 50 (GP50); FDC disabled.

8.3.13 Extended 1 Multi-Function Pin Selection Register (Index=2Ah, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Enable 3VSBSW# (E3VSBSW)** This function is for System Suspend-to-RAM. 0: Always inactive 1: Enabled It will be (NOT SUSB#) NAND SUSC#.s
6	**Multi-Function Selection of Pin 53 (MSP)** 0: MTRB#/PECIRQT#/PCIRST1# When bit 5 of index 24h is set to “1”, select PCIRST1# output, and bit 6 of index 2Ch is set to “1”, select PECIRQT# output; otherwise select MTRB#. 1: External Thermal Sensor Data/THERM_O# When bit 6-4 of EC index 0Ah is not equal to “000b”, the external thermal sensor host is enabled, and pin 53 becomes external thermal function.
5	**Extended Multi-Function Selection of Pin 32 (EMSP)** 0: RESETCON# enabled 1: RESETCON# disabled
4	**Reserved**
3	**Function Selection of Pin 66 (FSP)** 0: UART 5 pin selection disabled 1: Pin 66 determined by bit 2 of GPIO Set 2 Multi-function Selection Register (Index 26h) GPIO or SOUT5
2	**Function Selection of Pin 23 (FSP)** 0: UART 4 pin selection disabled 1: DTR4#
1	**SCR Reserved** 0: UART or GPIO (must be 0) 1: Reserved
0	**3VSBSW# Timing Control (3VSBSWTC)** 0: 3VSBSW# goes high leading PWROK for about 1ms. 1: 3VSBSW# goes high leading PWROK for about 120~160ms. **Note:** When E3VSBSW (bit7 of index 2Ah) is set to “1”, SDP(bit 3-2 of index 23h) are not allowed to be set to “01”.

8.3.14 Logical Block Lock Register (Index=2Bh, Default=00h)

When the lock function is enabled (bit7=1 or XLOCK# is low), configuration registers of the selected logical block and clock selection register (index = 23h), and this register will be read-only.

Bit	Description
7	**Software Lock Enable(SLE)** Once this bit is set to 1 by software, it only can be cleared by hardware reset. 0: The configuration lock is controlled by XLOCK#. (Default) 1: The logic blocks of the configuration register are selected by bit 6-0 and this register is read-only.
6	**GPIO Select (GPIOS)** 0: GPIO configuration registers are programmable. 1: GPIO configuration registers are read-only if LOCK is enabled.
5	**KBC(Keyboard) and KBC(Mouse) Select (KMS)** 0: KBC(Keyboard) and KBC(Mouse) configuration registers are programmable. 1: KBC(Keyboard) and KBC(Mouse) configuration registers are read-only if LOCK is enabled.
4	**EC Select (ECS)** 0: EC configuration registers are programmable. 1: EC configuration registers are read-only if LOCK is enabled.
3	**Parallel Port Select (PPS)** 0: Parallel Port configuration registers are programmable. 1: Parallel Port configuration registers are read-only if LOCK is enabled.
2	**Serial Port 2, 4, 6 Select (SP2S)** 0: Serial Port 2, 4, 6 configuration registers are programmable. 1: Serial Port 2, 4, 6 configuration registers are read-only if LOCK is enabled.
1	**Serial Port 1, 3, 5 Select (SP1S)** 0: Serial Port 1, 3, 5 configuration registers are programmable. 1: Serial Port 1, 3, 5 configuration registers are read-only if LOCK is enabled.
0	**FDC Select (FDCS)** The lock function will not affect bit 0 of FDC special configuration register (software write protect). 0: FDC configuration registers are programmable. 1: FDC configuration registers are read-only (except Software Write Protect bit) if LOCK is enabled.

8.3.15 Extended 2 Multi-Function Pin Selection Register (Index=2Ch, Default=03h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	**Enable SMB_D/C Switching On (ESMBSO)** 1: Disable 0: Enable SMB_ON (SMBD_M switch into SMBD_R, and SMBC_M switch into SMBC_R) when Parallel PORT is disabled.
6	**Enable PECI Request (EPECIRQT)** 0: Disable 1: Enable
5	**Reserved**
4	**Extended Multi-Function Selection of Pin 12 (EMSP)** 0: Reserved 1: Enable RI3# input
3	**Extended Multi-Function Selection of Pin 29, 77, 85 (EMSP)** This bit enables DTR6, SOUT6 RTS6 output of UART 6. 0: Disable 1: Enable
2	**Enable UART 6 Input of Pin 87, 92, 93, 94, 95 (EUI)** 0: Disable 1: Enable RI6#, CTS6#, SIN6, DCD6#, DSR6# input to UART 6 block.
1	**Enable VIN7 Internal Voltage Divider (EVIVD)** This bit enables and switches VIN7 (pin 91) to the internal voltage divider for VCCH5V. 0: Disable 1: Enable
0	**Enable ATXPG, VIN3 Internal Voltage Divider (EAVIVD)** This bit enables ATXPG (pin 95) and switches the VIN3 function to the internal voltage divider for VCC5V 0: Disable 1: Enable

8.3.16 GPIO Set 6 Enable Register (Index=2Dh, Default=00h)

Bit	Description
7	0: PD7 1: General Purpose I/O 67 (GP67)
6	0: PD6 1: General Purpose I/O 66 (GP66)
5	0: PD5 1: General Purpose I/O 65 (GP65)
4	0: PD4 1: General Purpose I/O 64 (GP64)
3	0: PD3 1: General Purpose I/O 63 (GP63)
2	0: PD2 1: General Purpose I/O 62 (GP62)
1	0: PD1 1: General Purpose I/O 61 (GP61)
0	0: PD0 1: General Purpose I/O 60 (GP60)

8.3.17 Test 1 Register (Index=2Eh, Default=00h)

This register cannot be configured because it is a test register and reserved for ITE only.

8.3.18 Test 2 Register (Index=2Fh, Default=00h)

This register cannot be configured because it is a test register and reserved for ITE only.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**FDC Enable(FDCE)** 1: Enable 0: Disable

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Base Address [15:12](BA)** Read only, with "0h" for Base Address [15:12].
3-0	**Base Address [11:8] (BA)** Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**Base Address [7:3](BA)** Read/write, mapped as Base Address [7:3].
2-0	**Reserved** Read only as "000b".

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	**Reserved** With default "0h".
3-0	**Select Interrupt Level for FDC(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	**Reserved** With default "00h"
2-0	**Select DMA Channel for FDC (SDMA)** Please refer to Table 8-17 DMA Channel Mapping Table on page 79.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-5	**Reserved** With default "00h".
4	**FDD I/F Input Pin Internal Pull-up Control (FIPU)** 0: Disable 1: Enable

Bit	Description
3	**IRQ Type (IT)** 1: IRQ sharing 0: Normal IRQ
2	**Swap Floppy Drive A, B Enable(SFDE)** 1: Swap Floppy Drive A, B 0: Normal
1	**Floppy Operation Mode(FOM)** 1: 3-mode 0: AT-mode
0	**Software Write Protect Enable(SWPE)** 1: Software Write Protect 0: Normal

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	**Reserved** With default “00h”.
3-2	**FDD B Data Rate Table Select (FBDRTS)** **(**DRT1-0)
1-0	**FDD A Data Rate Table Select (FADRTS)** (DRT1-0)

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 1 Enable (SP1E)** 1: Enable 0: Disable

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Base Address[7:3] (BA)** Read/write, mapped as Base Address[7:3]
2-0	**Reserved** Read only as “000b”

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	**Reserved** With default “0h”.
3-0	**Select Interrupt Level for Serial Port 1(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.5.5 Serial Port 1 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**RS485 Direction Control Enable(RS485DCE)** 0: Disable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver. 1: Enable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver.
6-4	**Reserved**
3	**Reserved** With default “0”
2-1	**Clock Source(CS)** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: 24 MHz 11: 24 MHz/1.625
0	**IRQ Type (IT)** 1: IRQ sharing 0: Normal

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 2 Enable(SP2E)** 1: Enable 0: Disable

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only with “0h” for Base Address [15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address [11:8]

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Base Address[7:3] (BA)** Read/write, mapped as Base Address [7:3]
2-0	**Reserved** Read only as “000b”

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	**Reserved** With default “0h”
3-0	**Select Interrupt Level for Serial Port 2(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**RS485 Direction Control Enable(RS485DCE)** 0: Disable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver. 1: Enable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver.
6-4	**Reserved**
3	**Reserved** With default “0”
2-1	**Clock Source (CS)** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: 24 MHz 11: 24 MHz/1.625
0	**IRQ Type(IT)** 1: IRQ sharing 0: Normal

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Parallel Port Enable (PPE)** 1: Enable 0: Disable

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If bit 2 is set to “1”, the EPP mode is disabled automatically.

Bit	Description
7-2	**Base Address[7:2] (BA)** Read/write, mapped as Base Address[7:2]
1-0	**Reserved** Read only as “00b”

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Base Address[7:2] (BA)** Read/write, mapped as Base Address[7:2]
1-0	**Reserved** Read only as “00b”

8.7.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	**Reserved** With default “0h”
3-0	**Select Interrupt Level for Parallel Port (SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.7.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	**Reserved** With default “00h”
2-0	**Select DMA Channel for Parallel Port(SDMA)** Please refer to Table 8-17 DMA Channel Mapping Table on page 79.

8.7.8 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-4	**Reserved**
3	**POST Data Port Enable (PDPE)** 1: Disable 0: Enable
2	**IRQ Type (IT)** 1: IRQ sharing 0: Normal
1-0	**Parallel Port Mode (PPM)** 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode These bits are independent. If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled except when Parallel Port Primary Base Address LSB Register bit 2 is set to “1” in accordance with the EPP specification.

8.8 Environment Controller Configuration Registers (LDN=04h)

8.8.1 Environment Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Environment Controller Enable (ECE)** 1: Enable 0: Disable This is a **read/write** register.

8.8.2 Environment Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.8.3 Environment Controller Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	**Base Address[7:3] (BA)** Read/write, mapped as Base Address[7:3]
2-0	**Reserved** Read only as “000b”

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	**Base Address[7:3] (BA)** Read/write, mapped as Base Address[7:3]
2-0	**Reserved** Read only as “000b”

8.8.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	**Reserved** With default “0h”
3-0	**Select Interrupt Level for Environment Controller (SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.8.7 APC/PME Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	**VCCH Power Off(VPO)** This bit is set to "1" when VCCH is off. Write 1 to clear it. This bit will become ineffective if 0 is written to it.
6	**Reserved**
5	**Reserved** With default "0h"
4	**PS2 Mouse Event Enable(PMEE)** 1: Enable 0: Disable
3	**Keyboard Event Enable(KEE)** 1: Enable 0: Disable
2-1	**Reserved** With default "00"
0	**CIR Event Enable (CIREE)** **1: Enable** **0: Disable**

8.8.8 APC/PME Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	**VCC Power On(VCCPO)** It is set to 1 when VCC is on at the previous AC power failure and 0 when VCC is off.
6	**Reserved**
5	**Reserved**
4	**PS2 Mouse Event Detect(PMED)** 0: No event detected 1: Event detected
3	**Keyboard Event Detect** 0: No event detected 1: Event detected
2-1	**Reserved** With default "00"
0	**CIR Event Detect** **0: No event detected** **1: Event detected**

8.8.9 APC/PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	**PER/PSR Normal Run Access Enable(PPNRAE)** 0: Enable 1: Disable
6	**PME# Output Control(POC)** 0: Enable 1: Disable
5	**Previous VCC State(PVS)** This bit is automatically restored to the previous VCC state before the power failure occurs.

Bit	Description
	1: Enable 0: Disable
4	**Reserved**
3	**Keyboard Event Selection(KES)** This bit is for Keyboard event mode selection when VCC is on (KEMSVO). 1: Determined by PCR 2 0: Pulse falling edge on KCLK
2	**Mouse Event at VCC Off(MEVF)** 1: Click key twice sequentially 0: Pulse falling edge on MCLK
1	**Mouse Event at VCC On(MEVO)** 1: Click key twice sequentially 0: Pulse falling edge on MCLK
0	**CIRRX Pin Selection(CIRRXPS)** 1: Pin 63 selected 0: Pin 85 selected

8.8.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-6	**Scan Frequency of H/W Monitor(SFHM)** 00: 1Hz 01: 2Hz 10: 4Hz 11: 8Hz
5-1	**Reserved**
0	**IRQ Type(IT)** 1: IRQ sharing 0: Normal

8.8.11 APC/PME Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	**Disable KCLK/KDAT and MCLK/MDAT Auto-Swap(DKMA)** 0: Enable 1: Disable
6	**Reserved**
5	**PSON# State at VCCH Switched from off to on(PSVS)** 0: High-Z The default is power-off. 1: Inverting of PSIN
4	**Mask PANSWH# Power-on Event(MPPOE)** 1: Enable 0: Disable
3-2	**Key Number of Keyboard Power-up Event(KNKPUE)** 00: 5 key string mode, 3 keys simultaneous mode 01: 4 key string mode, 2 keys simultaneous mode 10: 3 key string mode, 1 key simultaneous mode 11: 2 key string mode, Reserved (Not Valid for Simultaneous mode)
1-0	**Keyboard Power-up Event Mode Selection(KPEMS)** 00: KCLK falling edge

	01: Key string mode 10: Simultaneous key stroke mode 11: Reserved

8.8.12 APC/PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	**Reserved** Must be “00”.
5-0	**CIR Key Code Index[5:0](CKCI)** Indicate which identification key code or CIR code register to be read/written via 0xF6.

8.8.13 APC/PME Special Code Data Register (Index=F6h)

Bit	Description
7-0	**CIR Key Code Data[7:0](CKCD)** There are 5 bytes for the key string mode, 3 bytes for stroke key at the same time mode and CIR event codes.

8.8.14 APC/PME Control (PCR 7) Data Register (Index=F7h)

Bit	Description
7-0	**PCR 7 DATA[7:0] (PCR7DD)** Bit 7-0 are supplied by VBAT, and can be read/written directly.

8.9 KBC(Keyboard) Configuration Registers (LDN=05h)

8.9.1 KBC(Keyboard) Activate (Index=30h, Default=01h)

Bit	Description
7-1	**Reserved**
0	**KBC(Keyboard) Enable(KBCE)** 1: Enable 0: Disable

8.9.2 KBC (Keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Base Address[15:12](BA)** Read only as “0h” for Base Address [15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address [11:8]

8.9.3 KBC (Keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	**Base Address[7:0] (BA)** Read/write, mapped as Base Address[7:0]

8.9.4 KBC (Keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Base Address[15:12] (BA)** Read only as “0h” for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.9.5 KBC (Keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	**Base Address[7:0] (BA)** Read/write, mapped as Base Address[7:0]

8.9.6 KBC (Keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	**Reserved** With default “0h”
3-0	**Select Interrupt Level for KBC(Keyboard)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.9.7 KBC(Keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type set for KBC(Keyboard) and is **read only** as "02h" when bit 0 of the KBC(Keyboard) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	**Interrupt Level(IL)** 1: High level 0: Low level
0	**Interrupt Type(IT)** 1: Level type 0: Edge type

8.9.8 KBC(Keyboard) Special Configuration Register (Index=F0h, Default=08h)

Bit	Description
7-5	**Reserved**
4	**IRQ Type(IT)** 1: IRQ sharing 0: Normal
3	**KBC Clock(KC)** 1: 8 MHz 0: 12 MHz
2	**KBC Key Lock(KKL)** 1: Enable 0: Disable
1	**Interrupt Type Change Enable(ITCE)** 1: The interrupt type of KBC(Keyboard) can be changed. 0: The interrupt type of KBC(Keyboard) is fixed.
0	**Reserved**

8.10 KBC(Mouse) Configuration Registers (LDN=06h)

8.10.1 KBC(Mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**KBC(Mouse) Enable(KE)** 1: Enable 0: Disable

8.10.2 KBC(Mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	**Reserved** With default “0h”
3-0	**Select Interrupt Level for KBC(Mouse)(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.10.3 KBC(Mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the interrupt type used for KBC(Mouse) and is **read only** as “02h” when bit 0 of the KBC(Mouse) Special Configuration Register is cleared. When bit 0 is set, the interrupt type can be selected as level or edge trigger.

Bit	Description
7-2	**Reserved**
1	**Interrupt Level(IL)** 1: High level 0: Low level
0	**Interrupt Type(IT)** 1: Level type 0: Edge type

8.10.4 KBC (Mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	**Reserved** With default “00h”
1	**IRQ Type(IT)** 1: IRQ sharing 0: Normal
0	**Interrupt Type Change Enable(ITCE)** 1: The interrupt type of KBC(Mouse) can be changed. 0: The interrupt type of KBC(Mouse) is fixed.

8.11 GPIO Configuration Registers (LDN=07h)

8.11.1 SMI# Normal Run Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Base Address [15:12] (BA)** Read only as “0h” for Base Address [15:12]
3-0	**Base Address [11:8] (BA)** Read/write, mapped as Base Address [11:8]

8.11.2 SMI# Normal Run Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-2	**Base Address [7:2] (BA)** Read/write, mapped as Base Address [7:2]
1-0	**Read only** as “00b”

8.11.3 Simple I/O Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Base Address [15:12] (BA)** Read only as “0h” for Base Address [15:12]
3-0	**Base Address [11:8] (BA)** Read/write, mapped as Base Address [11:8]

8.11.4 Simple I/O Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**Base Address [7:0] (BA)** Read/write, mapped as Base Address[7:0]

8.11.5 Serial Flash I/F Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Base Address [15:12] (BA)** Read only as “0h” for Base Address [15:12]
3-0	**Base Address [11:8] (BA)** Read/write, mapped as Base Address [11:8]

8.11.6 Serial Flash I/F Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-3	**Base Address [7:3] (BA)** Read/write, mapped as Base Address [7:3]
2-0	**Read only** as “000b”

8.11.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	**Reserved**
3-0	**Select Interrupt Level for Panel Button De-bounce(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.11.8 Watch Dog Timer 1, 2, 3 Control Register (Index=71h, 81h, 91h Default=00h)

Bit	Description
7	**Reserved**
6	**WDT Reset upon Mouse Interrupt(WRKMI)** 0: Disable 1: Enable
5	**WDT Reset upon Keyboard Interrupt(WRKBI)** 0: Disable 1: Enable
4	**Reserved**
3-2	**Reserved**
1	**Force Time-out(FTO)** This bit is self-cleared.
0	**WDT Status(WS)** 1: WDT value is equal to 0. 0: WDT value is not equal to 0.

8.11.9 Watch Dog Timer 1, 2, 3 Configuration Register (Index=72h, 82h, 92h Default=001s0000b)

Bit	Description
7	**WDT Time-out Value Select 1 (WTVS)** 1: Second 0: Minute
6	**WDT Output through KRST (Pulse) Enable(WOKE)** 1: Enable 0: Disable
5	**WDT Time-out Value Extra Select(WTVES)** 1: 64ms x WDT Timer-out value (default = 4s) 0: Determined by WDT Time-out Value Select 1 (bit 7 of this register)
4	**WDT Output through PWROK (Pulse) Enable(WOPE)** 1: Enable 0: Disable During LRESET#, this bit is selected by JP7 power-on strapping option.
3-0	**Select Interrupt Level for WDT(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.11.10 Watch Dog Timer 1, 2, 3 Time-Out Value (LSB) Register (Index=73h, 83h, 93h, Default=38h)

Bit	Description
7-0	**WDT Time-out Value 7-0(WTV)**

8.11.11 Watch Dog Timer 1, 2, 3 Time-Out Value (MSB) Register (Index=74h, 84h, 94h Default=00h)

Bit	Description
7-0	**WDT Time-out Value 15-8(WTV)**

8.11.12 GPIO Pin Set 1, 2, 3, 4, and 5 Polarity Registers (Index=B0h, B1h, B2h, B3h, and B4h , Default=00h)

These registers are used to program the GPIO pin type as polarity inverting or non-inverting.

Bit	Description
7-0	**GPIO Polarity Select(GPIOPS)** 1: Inverting 0: Non-inverting

8.11.13 GPIO Pin Set 1, 2, 3, 4, and 5 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh, and BCh, Default=00h)

These registers are to enable the GPIO pin internal pull-up.

Bit	Description
7-0	**GPIO Pin Internal Pull-up(GPIOPIP)** 1: Enable 0: Disable

8.11.14 Simple I/O Set 1, 2, 3, 4 and 5 Enable Registers (Index=C0h, C1h, C2h, C3h, and C4h, Default=01h, 00h, 00h, 40h, and 00h)

These registers are to select the function as the Simple I/O function or the Alternate function.

Bit	Description
7-0	1: Simple I/O function 0: Alternate function

8.11.15 Simple I/O Set 1, 2, 3, 4, 5, and 6 Output Enable Registers (Index=C8h, C9h, CAh, CBh, CCh, and CDh Default=01h, 00h, 00h, 40h, 00h, and 00h)

These registers are to determine the direction of the Simple I/O.

Bit	Description
7-0	0: Input mode 1: Output mode GP30(P93), GP31(P92), GP32(P91) are GPI only

8.11.16 Panel Button De-bounce 0 Input Pin Mapping Register (Index=E0h, Default=00h)

Bit	Description
7	**Reserved**
6	**IRQ Enable(IRQE)** 1: Enable 0: Disable
5-0	**Input Pin Location(IPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.17 Panel Button De-bounce 1 Input Pin Mapping Register (Index=E1h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Input Pin Location(IPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.18 IRQ External Routing 1-0 Input Pin Mapping Registers (Index=E3h-E2h, Default=00h)

Bit	Description
7	**Reserved**
6	**IRQ Enable(IE)** 1: Enable 0: Disable
5-0	**Input Pin Location(IPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.19 IRQ External Routing 1-0 Interrupt Level Selection Registers (Index=E4h, Default=00h)

Bit	Description
7-4	**Routing 1 Interrupt Level Select(R1ILS)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.
3-0	**Routing 0 Interrupt Level Select(R0ILS)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.11.20 SPI Function Pin Selection Register (Index=EFh, Default=00001s0)

Bit	Description
7-2	**Reserved**
1-0	**SPI Chip-Sel Select(SPICSS)** Bit 1 and bit 0 need to be kept at the same polarity. 11: Pin 30 is CE_N output and pin 25 is SCK output (Default). 00: Reserved

8.11.21 SMI# Control Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**Enable Generation of SMI# due to Serial Port 3's IRQ (EN_S3IRQ)**
6	**Enable Generation of SMI# due to KBC(Mouse)'s IRQ (EN_MIRQ)**
5	**Enable Generation of SMI# due to KBC(Keyboard)'s IRQ (EN_KIRQ)**
4	**Enable Generation of SMI# due to Environment Controller's IRQ (EN_ECIRQ)**
3	**Enable Generation of SMI# due to Parallel Port's IRQ (EN_PIRQ)**
2	**Enable Generation of SMI# due to Serial Port 2's IRQ (EN_S2IRQ)**
1	**Enable Generation of SMI# due to Serial Port 1's IRQ (EN_S1IRQ)**
0	**Enable Generation of SMI# due to FDC's IRQ (EN_FIRQ)**

8.11.22 SMI# Control Register 2 (Index=F1h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI Trigger Type(STT)** 0: Edge trigger 1: Level trigger
5-4	**Enable Generation of SMI# due to Serial Port 6, 5's IRQ (EN_S6,5IRQ)**
3	**Reserved**
2	**Enable Generation of SMI# due to WDT's IRQ (EN_WDT)**
1	**Enable Generation of SMI# due to Serial Port 4's IRQ (EN_S4IRQ)**
0	**Enable Generation of SMI# due to PBD's IRQ (EN_PBD)**

8.11.23 SMI# Status Register 1 (Index=F2h, Default=00h)

This register is used to read the status of SMI# input.

Bit	Description
7	**Serial Port 3's IRQ(SP3I)** 0: None detected 1: Detected
6	**KBC(PS/2 Mouse)'s IRQ(KMI)** 0: None detected 1: Detected
5	**KBC(Keyboard)'s IRQ(KBI)** 0: None detected 1: Detected
4	**Environment Controller's IRQ(ECI)** 0: None detected 1: Detected
3	**Parallel Port's IRQ(PPI)** 0: None detected 1: Detected
2	**Serial Port 2's IRQ(SP2I)** 0: None detected 1: Detected
1	**Serial Port 1's IRQ(SP1I)** 0: None detected 1: Detected
0	**FDC's IRQ(FI)** 0: None detected 1: Detected

8.11.24 SMI# Status Register 2 (Index=F3h, Default=00h)

This register is used to read the status of SMI# input.

Bit	Description
7-6	**Panel Button De-bounce Status 1-0(PBDS)** Writing 1 will reset the status 0: None detected 1: Detected
5-4	**Serial Port 6,5's IRQ(SP65I)** 0: None detected 1: Detected
3	**Reserved**
2	**WDT's IRQ(WI)** 0: None detected 1: Detected
1	**Serial Port 4's IRQ(SP4I)** 0: None detected 1: Detected
0	**PBD's IRQ(PBDI)** 0: None detected 1: Detected

8.11.25 SMI# Pin Mapping Register (Index=F4h, Default=00h)

Bit	Description
7	**Reserved**
6	**SMI Normal Access Enable(SNAE)** 1: Enable (may directly access base_address + F0h ~ F3h) 0: Disable
5-0	**SMI# Pin Location(SPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.26 Hardware Monitor Thermal Output Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Thermal Output Pin Location(TOPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.27 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Alert Beep Pin Location(ABPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.28 Keyboard Lock Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**Keyboard Lock Pin Location(KLPL)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.29 GP LED Blinking 1 Pin Mapping Register (Index=F8h, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 1 Location(GLB1L)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.30 GP LED Blinking 1 Control Register (Index=F9h, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 1 Short Low Pulse Enable(GLB1SLPE)** 1: Enable 0: Disable
2-1	**GP LED 1 Frequency Control(GL1FC)** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 1 Output Low Enable(GLB1OLE)** 1: Enable 0: Disable

8.11.31 GP LED Blinking 2 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	**Reserved**
5-0	**GP LED Blinking 2 Location(GLB2L)** Please refer to Table 8-18 Location Mapping Table on page 80.

8.11.32 GP LED Blinking 2 Control Register (Index=FBh, Default=00h)

Bit	Description
7-4	**Reserved**
3	**GP LED Blinking 2 Short Low Pulse Enable(GLB2SLPE)** 1: Enable 0: Disable
2-1	**GP LED 2 Frequency Control (GL2FC)** 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	**GP LED Blinking 2 Output Low Enable(GLB2OLE)** 1: Enable 0: Disable

8.12 Serial Port 3, 4, 5, 6 Configuration Registers (LDN=08h, 09h, 0Ah, 0Bh)

8.12.1 Serial Port 3, 4, 5, 6 Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Serial Port 3, 4, 5, 6 Enable(SPE)** 1: Enable 0: Disable

8.12.2 Serial Port 3, 4, 5, 6 Base Address MSB Register (Index=60h, Default= 03h, 02h, 03h, 02h)

Bit	Description
7-4	**Base Address[15:12](BA)** Read only as "0h" for Base Address[15:12]
3-0	**Base Address[11:8] (BA)** Read/write, mapped as Base Address[11:8]

8.12.3 Serial Port 3, 4, 5, 6 Base Address LSB Register (Index=61h, Default= F8h)

Bit	Description
7-3	**Base Address[7:3] (BA)** Read/write, mapped as Base Address[7:3]
2-0	**Reserved** Read only as "000b"

8.12.4 Serial Port 3, 4, 5, 6 Interrupt Level Select Register (Index=70h, Default= 04h, 03h, 04h, 03h)

Bit	Description
7-4	**Reserved** With default "0h"
3-0	**Select Interrupt Level for Serial Port 3(SIL)** Please refer to Table 8-16 Interrupt Level Mapping Table on page 79.

8.12.5 Serial Port 3, 4, 5, 6 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	**RS485 Direction Control Enable(RS485DCE)** 0: Disable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver. 1: Enable RTSN asserted for RS485 automatic direction control when transmitting data to or receiving data from RS485 transceiver. **Note:** Function supported by Serial Port 1, 2, 3, 4 only
6-4	**Serial Port 3, 4, 5, 6 Mode(SPM)** Note3 000: Standard (Default) 001: IrDA 1.0 (HP SIR) 010 : ASKIR 100 : Reserved else : Reserved **Note:** Except the standard mode, COM1 and COM2 cannot be selected in the same mode.
3	**Reserved** With default "0"

Bit	Description
2-1	**Clock Source(CS)** 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: 24 MHz 11: 24 MHz/1.625
0	**IRQ Type(IT)** 1: IRQ sharing 0: Normal

8.13 Consumer IR Configuration Registers (LDN=0Ch)

8.13.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**Consumer IR Enable** 1: Enable 0: Disable

8.13.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12]
3-0	**Read/write**, mapped as Base Address[11:8]

8.13.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3]
2-0	**Read only** as "000b"

8.13.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	**Reserved** with default "0h"
3-0	Select the interrupt level Note1 for Consumer IR

8.13.5 Consumer IR Special Configuration Register (Index=F0h, Default=06h)

Bit	Description
7-1	**Reserved** with default "00h"
0	1: IRQ sharing 0: Normal

Table 8-16 Interrupt Level Mapping Table

Value	Description
Fh-Dh	Invalid
Ch	IRQ12
3h	IRQ3
2h	Invalid
1h	IRQ1
0h	No Interrupt Selected

Table 8-17 DMA Channel Mapping Table

Value	Description
7h-5h	Invalid
4h	Invalid
3h	DMA3
2h	DMA2

Value	Description
1h	DMA1
0h	DMA0

Table 8-18 Location Mapping Table

Location	Description
001 000	GP10 (pin 83). Powered by VCCH.
001 001	GP11 (pin 82). Powered by VCCH.
001 010	GP12 (pin 81).
001 011	GP13 (pin 80).
001 100	GP14 (pin 30).
001 101	GP15 (pin 29)
001 110	GP16 (pin 25).
001 111	GP17 (pin 24)
010 000	GP20 (pin 84). Powered by VCCH
010 001	GP21 (pin 70).
010 010	GP22 (pin 66).
010 011	GP23 (pin 48).
010 100	GP24 (pin 36).
010 101	GP25 (pin 34).
010 110	GP26 (pin 33).
010 111	GP27 (pin 32)
011 011	GP33 (pin 10).
011 100	GP34 (pin 85).
011 101	GP35 (pin 77).
011 110	GP36 (pin 45).
011 111	GP37 (pin 9).
100 000	GP40 (pin 79). Powered by VCCH.
100 001	GP41 (pin 78). Powered by VCCH.
100 010	GP42 (pin 76). Powered by VCCH.
100 011	GP43 (pin 75). Powered by VCCH.
100 101	GP45 (pin 73)
100 110	GP46 (pin 72). Powered by VCCH.
100 111	GP47 (pin 71).
101 000	GP50 (pin 52).
101 001	GP51 (pin 54).
101 010	GP52 (pin 56).
101 011	GP53 (pin 57).
101 100	GP54 (pin 58).
101 101	GP55 (pin 59).
101 110	GP56 (pin 60).
101 111	GP57 (pin 61).
Else	**Reserved**

9. Functional Description

9.1 LPC Interface

The IT8783E/F supports the peripheral side of the LPC I/F as described in the LPC Interface Specification Rev.1.1. In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (the same as PCICLK.)), the IT8783E/F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8783E/F supports the required transfer cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will react according to the DMA requests from the DMA devices in the Super I/O modules, and decide whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and respond with an SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. Nevertheless, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there are at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8783E/F follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface most PC chipsets. The IT8783E/F encodes the parallel interrupts to an SERIRQ, which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turn-around state of the current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enters the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when the situation that one SIRQ Slave detects its input IRQn/events have been changed happens, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

Figure 9-1. Start Frame Timing

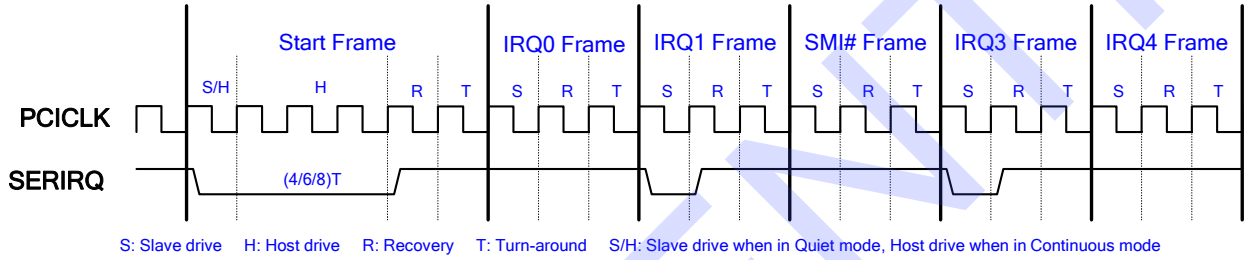
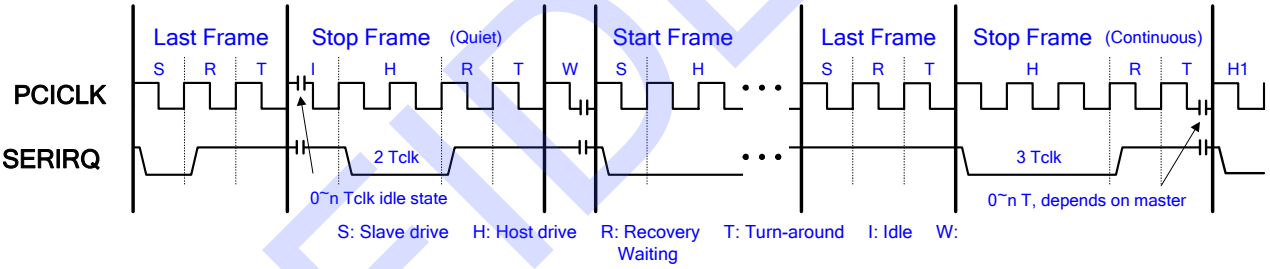


Figure 9-2. Stop Frame Timing



9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn/ Event	#of Clocks Past Start	IT8783E/F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8783E/F provides five sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 25h, 26h, 27h, 28h and 29h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=07h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into five registers. The accessed I/O ports are programmable and are five consecutive I/O ports (Base Address+0, Base Address+1, Base Address+2, Base Address+3, Base Address+4). Base Address is programmed on the registers of GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=60h and 61h).

The Alternate function provides several special functions for users, including Watch Dog Timer, SMI# output routing, External Interrupt routing, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, Thermal output routing, and Beep output routing. The last two are the sub-functions of the Hardware Monitor.

The Panel Button De-bounce is an input function. After it is enabled, a related status bit will be set when an active low pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. Panel Button De-bounce Interrupt will be issued if any of the status bit is set. However, the newly set status will not issue another interrupt unless the previous status bit is cleared before being set.

The Key Lock function locks the keyboard to inhibit the keyboard interface. The way pf programming is by setting bit 2 on the register Index F0h of KBC(Keyboard) (LDN=5). The pin location mapping, Index F7h also must be programmed correctly.

The Blinking function provides a low frequency blink output. By connecting to some external components, it can be used to control a power LED. There are several frequencies for selection.

The Watch Dog Timer (WDT) function is constituted by a time counter, a time-out status register, and the timer reset control logic. The time-out status bit may be mapped to an interrupt or KRST# through the WDT configuration register. The WDT has a programmable time-out ranging from 1 to 65535 minutes or 1 to 65535 seconds. The unit, either a minute or a second, is also programmable via bit 7 of the WDT configuration register. In real time, the clock divider provides 68.8 msec per timer cycle to WDT operation when the time unit is selected as 64 ms, 1.1 sec per timer cycle to WDT operation when the time unit is selected as 1 sec, and 1.1 minute per timer cycle to WDT operation when the time unit is selected as 1 minute. When the WDT Time-out Value register is set to a non-zero value, the WDT loads the value and begins counting down from the value. When the value reaches to 0, the WDT status register will be set. There are two system events including a Keyboard Interrupt and a Mouse Interrupt that can reload the non-zero value into the WDT. The effect on the WDT for each of the events may be enabled or disabled through bits in the WDT control register. No matter what the value is in the time counter, the host may force a time-out to occur by writing a "1" to the bit 1 of the WDT configuration register.

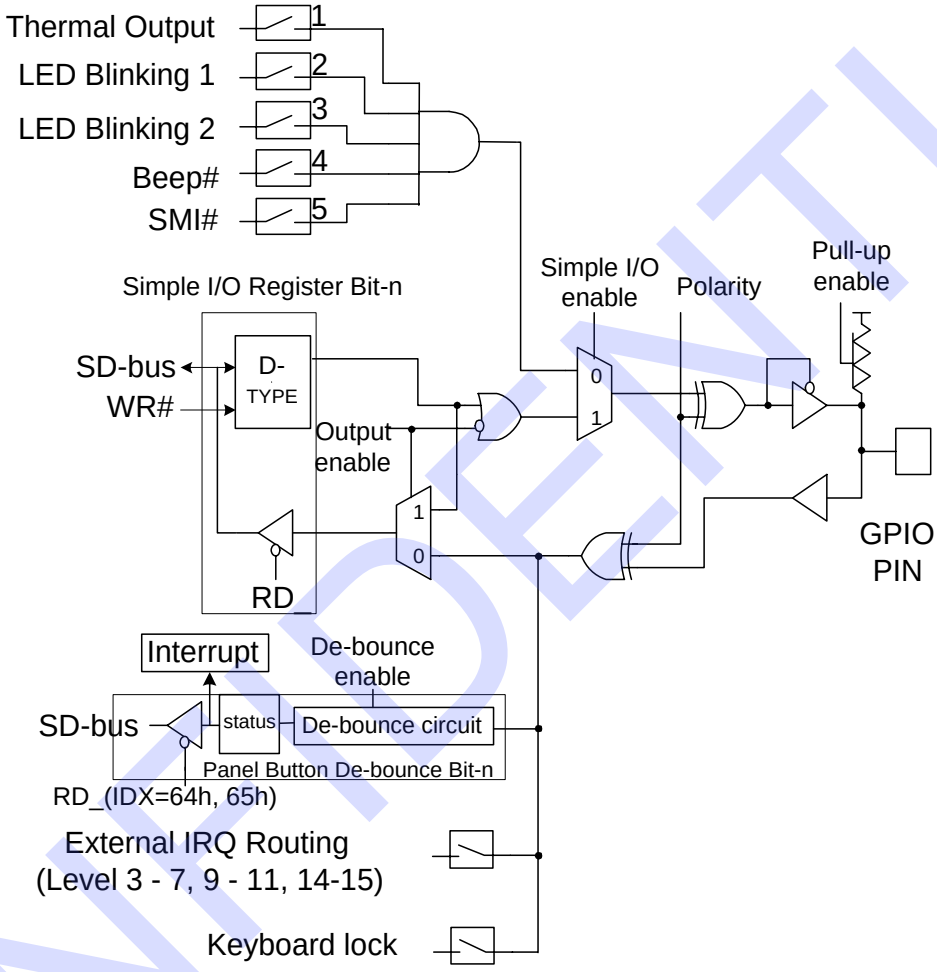
The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8783E/F. The interrupts are redirected as the SMI# output via the SMI# Control Register 1 and SMI# Control Register 2. The SMI# Status Register 1 and 2 are used to read the status of the SMI input event. All the SMI# Status Register bits can be cleared when the corresponding source events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# Control Register 2 no matter whether the events of the corresponding sources are invalidated or not. The SMI# events can be programmed as the pulse mode or level mode whenever an SMI#

event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_PBDIRQ or PBDIRQ) or (EN_KIRQ and KIRQ) or (EN_MIRQ and MIRQ) or (EN_WDT and WDT_IRQ) or (EN_STPCLK and STPCLK_IRQ)

Figure 9-3. General Logic of GPIO Function



9.4 Advanced Power Supply Control and Power Management Event (PME#)

The circuit for advanced power supply control (APC) provides two power-up events, Keyboard and Mouse. When any of these two events is true, PWRON# will perform a low state until VCC is switched to the ON state. The two events include the followings:

1. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously.
2. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means clicking on any mouse button twice sequentially.

The PANSWH# and PSON# are especially designed for the system. PANSWH# serves as a main power switch input, which is wire-AND to the APC output PWRON#. PSON# is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the PSIN input until PANSWH# becomes active when the VCCH is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, index F4h, bit 5). The gating circuit also provides an auto-restore function. After bit 5 of PCR1 is set, the previous PSON# state will be restored when the VCCH is switched from OFF to ON.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all power-up events except switch-on event when the VCCH state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the keyboard power-up event and APC condition. Bit 4 is used to mask the PANSWH# power-on event on the PWRON# pin. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

All APC registers (Index=F0h, F2h, F4h, F5h and F6h) are powered by back-up power (VBAT) when VCCH is OFF.

PME# is used to wake up the system from low-power states (S1-S5). Except the five events of the APC, there will be other events to generate PME#: They are RI1# and RI2# events. RI1# and RI2# are Ring Indicator of Modem status in ACPI S1 or S2 state. A falling edge on these pins issues PME# events if the enable bits are set.

9.5 SPI Serial Flash Controller

9.5.1 Overview

The SPI Serial Flash controller is a LPC to the serial Flash I/F controller.

9.5.2 Features

SPI Interface
LPC memory cycle and firmware memory cycle supported

9.5.3 Register Description

Table 9-1. Memory Stick Register List

Address	R/W	Default	Name
Base + 0h	R/W	20h	Control Register (SPI_CTRL)
Base + 1h	R/W	00h	Command Register (SPI_CMD)
Base + 2h	R/W	00h	Address 0 Register (SPI_ADDR0)
Base + 3h	R/W	00h	Address 1 Register (SPI_ADDR1)
Base + 4h	R/W	00h	Address 2 Register (SPI_ADDR2)
Base + 5h	R	--	Input Data 0 Register (SPI_IDATA0)
Base + 6h	R	--	Input Data 1 Register (SPI_IDATA1)
Base + 7h	R/W-R	00h/--	Output Data Register (SPI_ODATA)/ Input Data 2 Register (SPI_IDATA2)

9.5.3.1 Control Register (SPI_CTRL)

Address: Base address + 0h

Bit	R/W	Default	Description
7	R	-	**SPI Status(SPIS)** This bit reports the SPI I/F status. 0: Idle. 1: Busy.
6	R/W	0b	**Start IO Transfer(SIOT)** This bit starts the SPI cycle with the instruction/parameter given through I/O port. 0: No Start IO 1: Enable Start IO/going
5	R/W	1b	**Multiple Byte Mode(MBM)** This bit enables the multiple byte mode in LPC memory write/read cycle. 0: Disable 1: Enable
4	R/W	0b	**SCK Selection(SCKS)** This bit selects the SCK frequency. 0: 33MHz/2. 1: 33MHz.

Bit	R/W	Default	Description
3-2	R/W	00b	**Input Data Byte(IDB)** These bits determine the byte number of the input data in the Start IO mode. 00: None. 01: 1 byte. (SPI_DATAI0) 10: 2 bytes. (SPI_DATAI0, SPI_DATAI1). 11: 3 bytes. (SPI_DATAI0, SPI_DATAI1, SPI_DATAI2).
1-0	R/W	00b	**Output Data Byte(ODB)** These bits determine the byte number of the output data (including Instruction, Address, Data) in the Start IO mode. 00: 1 byte. (SPI_CMD) 01: 2 bytes. (SPI_CMD, SPI_DATAO) 10: 4 bytes. (SPI_CMD, ADDR2, ADDR1, ADDR0) 11: 5 bytes. (SPI_CMD, ADDR2, ADDR1, ADDR0, SPI_DATAO)

9.5.3.2 Command Register (SPI_CMD)

Address: Base address + 1h

Bit	R/W	Default	Description
7-0	R/W	00h	**Command Register (SPI_CMD [7:0])** This register will set the Instruction command code in the Start IO mode. (The first byte)

9.5.3.3 Address 0 Register (SPI_ADDR0)

Address: Base address + 2h

Bit	R/W	Default	Description
7-0	R/W	00h	**Address 0 Register (SPI_ADDR0 [7:0])** This register will set the Address [7:0] in the Start IO mode.

9.5.3.4 Address 1 Register (SPI_ADDR1)

Address: Base address + 3h

Bit	R/W	Default	Description
7-0	R/W	00h	**Address 1 Register (SPI_ADDR1 [7:0])** This register will set the Address [15:8] in the Start IO mode.

9.5.3.5 Address 2 Register (SPI_ADDR2)

Address: Base address + 4h

Bit	R/W	Default	Description
7-0	R/W	00h	**Address 2 Register (SPI_ADDR2 [7:0])** This register will set the Address [23:16] in the Start IO mode.

9.5.3.6 Input Data 0 Register (SPI_IDATA0)

Address: Base address + 5h

Bit	R/W	Default	Description
7-0	R	--	**Input Data 0 Register (SPI_IDATA0 [7:0])** This register will set the Input Data 0 byte in the Start IO mode.

9.5.3.7 Input Data 1 Register (SPI_IDATA1)

Address: Base address + 6h

Bit	R/W	Default	Description
7-0	R	--	**Input Data 1 Register (SPI_IDATA1 [7:0])** This register will set the Input Data 1 byte in the Start IO mode.

9.5.3.8 Output Data/Input Data 2 Register (SPI_ODATA/ SPI_IDATA2)

Address: Base address + 7h

Bit	R/W	Default	Description
7-0	R/W	00h	**Output Data Register/Input Data 2 Register (SPI_ODATA [7:0]/SPI_IDATA2 [7:0])** This register will set the Output Data byte in the Start IO mode, or Input Data 2 when the input data byte number is 3.

9.5.4 Function Descriptions

Programming sequence: For the instruction code and byte number, please refer to the Serial Flash product specification.

Start IO mode:

```
// 1:   Check SPI I/F
  IOR  [SPI_CTRL];              // check bit7 SPI status

// 2:   Set the parameters in any order of write sequence.

  IOW [SPI_CMD]     XXh:      // Set SPI Instruction
  IOW [SPI_ADDR0]   XXh:      // Set SPI Address0, if necessary
  IOW [SPI_ADDR1]   XXh:      // Set SPI Address1, if necessary
  IOW [SPI_ADDR2]   XXh:      // Set SPI Address2, if necessary
  IOW [SPI_ODATA]   XXh:      // Set SPI Output Data, if necessary

// 3:   Start SPI I/F
  IOW [SPI_CTRL]          {4'h1, Input_data_byte, Output_data_byte};
```

LPC memory cycle:

When the host issues a LPC memory read cycle with the matching memory space, the controller will issue a corresponding SPI read cycle automatically. The controller will pre-read from 0 to 3 byte(s) of data into the read buffers. The number of pre-read data byte(s) is determined by the starting address 0 and 1. The byte number will be 3 bytes if the two addresses are 00b. The number will be 2 bytes if the two addresses are 01b. The number will be 1 byte if the two addresses are 10b. There is no pre-read data if the two addresses are 11b.If the address of the next coming LPC memory cycle matches the

buffers' address, no SPI read cycle will be issued.

For most types of serial flash products, the Write-Enable instruction through the Start IO mode should be given before issuing the LPC memory writes cycle. Normally, each LPC memory cycle will issue a one byte SPI programming cycle (Instruction, Addresses, 1 Data byte). If the Multiple Byte mode is enabled, a multi-byte SPI programming cycle will be issued. For example:

```
// LPC Memory Write Multiple byte mode
// 1:   Write-Enable command
  IOR  [SPI_CTRL];                          // check bit7 SPI status
  IOW [SPI_CMD]          06h:       // Set SPI Instruction
  IOW [SPI_CTRL]         {4'h3, 2'b00, 2'b00};
                                    // Start IO SPI cycle and enable the LPC memory Multiple Byte mode

// 2:   LPC memory write cycles: The first LPC memory cycle will start an SPI cycle and determine the
//      Programming page address. The following LPC memory write cycles must be contiguous addresses.
// And, the total bytes cannot exceed 256 – [starting address 7-0]. These conditions should be
// confirmed by the programmer. The controller will not check them. During this period, the SPI cycle
// will not be finished. Between the two MEMW cycles, the HOLD# pin will be asserted and SCK will be forced low.
  MEMW   [Starting address]:        // Set SPI Address and the first byte data.
  MEMW   [Starting address+1]:      // Set SPI second byte data.
  MEMW   [Starting address+2]:      // Set SPI third byte data.
           :
  MEMW   [Starting address+N]:      // Set SPI Nth byte data.

// 3:   Terminate SPI I/F
  IOW [SPI_CTRL]         {4'h0, 2'b00, 2'b00};
                                    // Terminate LPC memory write Page Program mode and SPI cycle

// LPC Memory Read Multiple byte mode
// 1:   Write-Enable command
  IOW [SPI_CTRL]         {4'h2, 2'b00, 2'b00};
                                    // Enable LPC memory Multiple Byte mode

// 2:   LPC memory read cycles: The first LPC memory cycle will start the SPI cycle and determine the
//      reading address. The following LPC memory read cycles must be the contiguous addresses.
// And, the total bytes will not be limited. The programmer should confirm these conditions.
// The controller will not check them. During this period, the SPI cycle will not be finished. Between the two // MEMR cycles, the HOLD# pin will be asserted and SCK will be forced low.
  MEMR   [Starting address]:        // Set SPI Address and the first byte data.
  MEMR   [Starting address+1]:      // Set SPI second byte data.
  MEMR   [Starting address+2]:      // Set SPI third byte data.
           :
  MEMR   [Starting address+N]:      // Set SPI Nth byte data.

// 3:   Terminate SPI I/F
  IOW [SPI_CTRL]         {4'h0, 2'b00, 2'b00};
                                    // Terminate LPC memory Read Multiple Byte mode and SPI cycle
```

9.6 Environment Controller

The Environment Controller (EC), built in the IT8783E/F, includes eight voltage inputs, three temperature sensor inputs, five FAN Tachometer inputs, and three sets of advanced FAN Controllers. The EC monitors the hardware environment and implements the environmental control for personal computers.

The IT8783E/F contains an 8-bit ADC (Analog-to-Digital Converter), which is responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs ranging from 0V to 4.096V into 8-bit digital byte. With additional external components, the analog inputs can be made to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 4.096V. Through external thermistors or thermal diodes, the temperature sensor inputs can be converted into 8-bit digital byte, enabling the sensor inputs to monitoring the temperature of various components. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

FAN Tachometer inputs are digital inputs with an acceptable input range of 0V to 5V, and are responsible for measuring the FAN's Tachometer pulse periods.

The EC of the IT8783E/F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs. Both of LPC Bus and Serial Bus interfaces are supported to accommodate the needs for various applications.

9.6.1 Interfaces

LPC Bus: The Environment Controller of the IT8783E/F decodes two addresses.

Table 9-2. Address Map on LPC Bus

Register or Port	Address
Address register of EC	Base+05h
Data register of EC	Base+06h

Note 1: The Base Address is determined by Environment Controller Base Address MSB Register (Index=60h, Default=02h) (refer to page 61) and Environment Controller Base Address LSB Register (Index=61h, Default=90h) (refer to page 61).
To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

9.6.2 Registers

9.6.2.1 Address Port (Base+05h, Default=00h)

Bit	Description
7	**Outstanding; read only** This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	**Index** Internal Address of RAM and Registers.

Table 9-3. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration Register
01h	R	00h	Interrupt Status c 1
02h	R	00h	Interrupt Status Register 2
03h	R	00h	Interrupt Status Register 3
04h	R/W	00h	SMI# Mask Register 1
05h	R/W	00h	SMI# Mask Register 2
06h	R/W	00h	SMI# Mask Register 3
07h	R/W	00h	Interrupt Mask Register 1
08h	R/W	00h	Interrupt Mask Register 2
09h	R/W	80h	Interrupt Mask Register 3
0Ah	R/W	54h	Interface Selection Register
0Bh	R/W	09h	Fan PWM Smoothing Step Frequency Selection Register
0Ch	R/W	00h	Fan Tachometer 16-bit Counter Enable Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	07h	Fan Controller Main Control Register
14h	R/W	50h	FAN_CTL Control Register
15h	R/W	00h/20h/40h/60h	FAN_CTL1 PWM Control Register Bit7 must be 0.
16h	R/W	00h/20h/40h/60h	FAN_CTL2 PWM Control Register Bit7 must be 0.
17h	R/W	00h/20h/40h/60h	FAN_CTL3 PWM Control Register Bit7 must be 0.
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
20h	R	-	VIN0 Voltage Reading Register
21h	R	-	VIN1 Voltage Reading Register
22h	R	-	VIN2 Voltage Reading Register
23h	R	-	VIN3 Voltage Reading Register

Index	R/W	Default	Registers or Action
24h	R	-	VIN4 Voltage Reading Register
25h	R	-	VIN5 Voltage Reading Register
26h	R	-	VIN6 Voltage Reading Register
27h	R	-	VIN7 Voltage Reading Register
28h	R	-	VBAT Voltage Reading Register
29h	R	-	TMPIN1 Temperature Reading Register
2Ah	R	-	TMPIN2 Temperature Reading Register
2Bh	R	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register
52h	R/W	7Fh	TMPIN1 Thermal Output Limit Register
53h	R/W	7Fh	TMPIN2 Thermal Output Limit Register
54h	R/W	7Fh	TMPIN3 Thermal Output Limit Register
55h	R/W	00h	ADC Temperature Extra Channel Enable Register
56h	R/W	00h	Thermal Diode 1 Zero Degree Adjust Register
57h	R/W	00h	Thermal Diode 2 Zero Degree Adjust Register

Index	R/W	Default	Registers or Action
58h	R	90h	ITE Vendor ID Register
59h	R/W	00h	Thermal Diode 3 Zero Degree Adjust Register
5Bh	R	12h	Core ID Register
5Ch	R/W	60h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
63h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Start PWM Register
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Control Register
65h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode △-Temperature Register
68h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
6Ah	R/W	7Fh	Reserved
6Bh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Start PWM Register
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Control Register
6Dh	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode △-Temperature Register
70h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Fan Start Register
72h	R/W	7Fh	Reserved
73h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Start PWM Register
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Control Register
75h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode △-Temperature Register
88h	R/W	---00000b	External Temperature Sensor Host Status Register
89h	R/W	00h	External Temperature Sensor Host Target Address Register
8Ah	R/W	00h	External Temperature Sensor Host Write Length Register
8Bh	R/W	00h	External Temperature Sensor Host Read Length Register
8Ch	R/W	00h	External Temperature Sensor Host Command (Write Data 1) Register
8Dh	R/W	--h	External Temperature Sensor Write Data (2-8) Register
8Eh	R/W	02h	External Temperature Sensor Host Control Register
8Fh	R	00h	External Temperature Sensor Read Data (1-16) Register

9.6.2.2 Register Description

9.6.2.2.1 Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	**Initialization(INIT)** A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0”.
6	R/W	**Update VBAT Voltage Reading(UVVR)**
5	R/W	**COPEN# Cleared(CCW)** Write “1” to clear COPEN#. **Note:** The Case Open Status register (Index 01h<bit4>) will be cleared when first writing this register and then reading Index 01h<bit4>.
4	R	**Reserved** Read only; always “1”
3	R/W	**INT_Clear(INTC)** A “1” disables the SMI# and IRQ outputs while the contents of interrupt status bits remain unchanged.
2	R/W	**IRQ Enable (IRQE)** This bit is to enable the IRQ Interrupt output.
1	R/W	**SMI# Enable(SMIE)** A “1” enables the SMI# Interrupt output.
0	R/W	**Start(START)** A “1” enables the startup of monitoring operations and a “0” sets the monitoring operation in the STANDBY mode.

9.6.2.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7	R	**Reserved**
6	R	**Reserved**
5	R	**Reserved**
4	R	**Case Open Status(COS)** A "1" indicates a Case Open event has occurred. **Note:** The Case Open Status register (Index 01h<bit4>) will be cleared when first writing Index 00h<bit5> and then reading this register.
3	R	**Reserved**
2-0	R	**Count Limit Reached(CLR)** A "1" indicates the FAN_TAC3-1 Count limit has been reached.

9.6.2.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	**VIN7-0 Limit Reached(VLR)** A "1" indicates a High or Low limit of VIN7-0 has been reached.

9.6.2.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	**Reserved**
2-0	R	**Temperature limit Reached (TLR)** A "1" indicates a High or Low limit of Temperature 3-1 has been reached.

9.6.2.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6	R/W	**Reserved**
5	R/W	**Reserved**
4	R/W	**Case Open Interrupt SMI#(COISMI)** A "1" disables the Case Open Intrusion interrupt status bit for SMI#.
3	R/W	**Reserved**
2-0	R/W	**FAN_TAC3-1 Interrupt SMI#(FISMI)** A "1" disables the FAN_TAC3-1 interrupt status bit for SMI#.

9.6.2.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	**VIN7-0 Interrupt SMI#(VISMI)** A "1" disables the VIN7-0 interrupt status bit for SMI#.

9.6.2.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	**Reserved**
2-0	R/W	**Temperature3-1 Interrupt SMI#(TISMI)** A "1" disables the Temperature 3-1 interrupt status bit for SMI#.

9.6.2.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7	R/W	**Reserved**
6	R/W	**Reserved**
5	R/W	**Reserved**
4	R/W	**Case Open Interrupt IRQ(COIIRQ)** A "1" disables the Case Open Intrusion interrupt status bit for IRQ.
3	R/W	**Reserved**
2-0	R/W	**FAN_TAC3-1 Interrupt IRQ(FIIRQ)** A "1" disables the FAN_TAC3-1 interrupt status bit for IRQ.

9.6.2.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	**VIN7-0 Interrupt IRQ(VIIRQ)** A "1" disables the VIN7-0 interrupt status bit for IRQ.

9.6.2.2.10 Interrupt Mask Register 3 (Index=09h, Default=80h)

Bit	R/W	Description
7	R/W	**Ext Thermal Interrupt(ETI)** A "1" disables the External Thermal Sensor interrupt.
6-3	R/W	**Reserved**
2-0	R/W	**Temperature3-1 Interrupt IRQ(TIIRQ)** A "1" disables the Temperature3-1 interrupt status bit for IRQ.

9.6.2.2.11 Interface Selection Register (Index=0Ah, Default=54h)

Bit	R/W	Description
7	R/W	**Pseudo-EOC (End of conversion of ADC)(PEOC)** A Pseudo-EOC bit can speed up the setup time of FAN speed in the SmartGuardian automatic mode. (Write 1 to the bit then write 0.)
6-4	R/W	**External Thermal Sensor Host Selection(ETSHS)** 000: Disable 100: Reserved 101: SST Slave Device 110: PECI 111: SST Host Others: Reserved
3	R/W	**SST/PECI Host Controller Clock Selection(HCS)** 0: 32 MHz generated internally 1: 24 MHz

Bit	R/W	Description
2	R/W	**SST/PECI Host Controller (Auto speed no-change tolerance) tbit 1 Setting(HCTB)** 0: (2 host clocks) no less than 1 host clock 1: (1 host clock) less than 1 host clock
1	R/W	**Reserved** (must be 0)
1-0	R	**SST/PECI Host Controller Transition Speed Mode Selection(HCTSMS)** 00: Auto 01: Fixed at 1 MHz 10: Fixed at 0.5 MHz 11: Fixed at 0.25 MHz

9.6.2.2.12 Fan PWM Smoothing Step Frequency Selection Register (Index=0Bh, Default=09h)

Bit	R/W	Description
7-0	R/W	**Reserved**

9.6.2.2.13 Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7	R/W	**TMPIN3 Enhanced Interrupt Mode Enable(T3EIME)** 0: Original mode 1: The interrupt will be generated when the TMPIN3 is higher than the high limit or lower than the low limit.
6	R/W	**TMPIN2 Enhanced Interrupt Mode Enable(T2EIME)** 0: Original mode 1: The interrupt will be generated when the TMPIN2 is higher than the high limit or lower than the low limit.
5-4	R/W	**Reserved**
3	R/W	**TMPIN1 Enhanced Interrupt Mode Enable(T1EIME)** 0: Original mode. 1: The interrupt will be generated when the TMPIN1 is higher than the high limit or lower than the low limit.
2	R/W	**FAN_TAC3 16-bit Counter Divisor Enable(F3CDE)** 1: Enable 0: Disable
1	R/W	**FAN_TAC2 16-bit Counter Divisor Enable(F2CDE)** 1: Enable 0: Disable
0	R/W	**FAN_TAC1 16-bit Counter Divisor Enable(F1CDE)** 1: Enable 0: Disable

9.6.2.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	**Tachometer Reading Value(TRV)** The count number of the internal clock per revolution

9.6.2.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	**Limit Value(LV)**

9.6.2.2.16 Fan Controller Main Control Register (Index=13h, Default=07h)

Bit	R/W	Description
7	R	**Reserved**
6-4	R/W	**FAN_TAC3-1 Enable(FE)** 1: Enable 0: Disable
3	R/W	**Full Speed Control of FAN_CTL Automatic Mode(FSCFAM)** 0: The full speeds of FAN_CTL1-3 automatic mode are independent. 1: All FAN_CTL1-3 will enter their respective full speeds when the temperature exceeds the full Speed Temperature Limit.
2-0	R/W	**FAN_CTL3-1 Output Mode Selection(FCOMS)** 0: ON/OFF mode 1: SmartGuardian mode

9.6.2.2.17 FAN_CTL Control Register (Index=14h, Default=50h)

Bit	R/W	Description
7	R/W	**FAN_CTL Polarity (For all FANs)(FP)** 0: Active low 1: Active high
6-4	R/W	**FAN_CTL PWM Base Clock Selection(PBCS)** 000: 48 MHz(PWM Frequency=375 kHz) 001: 24 MHz(PWM Frequency=187.5 kHz) 010: 12 MHz(PWM Frequency=93.75 kHz) 011: 8 MHz(PWM Frequency=62.5 kHz) 100: 6 MHz(PWM Frequency=46.875 kHz) 101: 3 MHz(PWM Frequency=23.43 kHz) 110: 1.5 MHz(PWM Frequency=11.7 kHz) 111: 0.75 MHz(PWM Frequency=5.86 kHz)
3	R/W	**Reserved** (Must be 0)
2-0	R/W	**FAN_CTL ON/OFF Mode Control (FCOFMC)** These bits are only available when the relative output modes are selected in the ON/OFF mode. 0: OFF 1: ON

9.6.2.2.18 FAN_CTL1 PWM Control Register (Index=15h, Default=00h/20h/40h/60h)

The default value of this register is selected by JP5 and JP7.

Bit	R/W	Description
7	R/W	**FAN_CTL1 PWM Mode Automatic/Software Operation Selection (F1PASOS)** 0: Software operation 1: Automatic operation
6-0	R/W	**PWM Control Temperature Input Selection (PCTIS)** 128 steps of PWM control when in Software operation (bit 7=0)

9.6.2.2.19 FAN_CTL2 PWM Control Register (Index=16h, Default=00h/20h/40h/60h)

The default value of this register is selected by JP5 and JP7.

Bit	R/W	Description
7	R/W	**FAN_CTL2 PWM Mode Automatic/Software Operation Selection(F2PASOS)** 0: Software Operation 1: Automatic operation
6-0	R/W	**PWM Control Temperature Input Selection (PCTIS)** 128 steps of PWM control when in Software operation (bit 7=0) 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.6.2.2.20 FAN_CTL3 PWM Control Register (Index=17h, Default=00h/20h/40h/60h)

The default value of this register is selected by JP5 and JP7.

Bit	R/W	Description
7	R/W	**FAN_CTL3 PWM mode Automatic/Software Operation Selection(F3PASOS)** 0: Software Operation 1: Automatic operation
6-0	R/W	**PWM Control Temperature Input Selection(PCTIS)** 128 steps of PWM control when in Software operation (bit 7=0) Bit [1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.6.2.2.21 Fan Tachometer 1-3 Extended Reading Registers (Index=18h, 19h, 1Ah)

Bit	R/W	Description
7-0	R	**Count Number of Internal Clock Per Revolution [15:8]**

9.6.2.2.22 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh, 1Ch, 1Dh)

Bit	R/W	Description
7-0	R/W	**Limit Value [15:8]**

9.6.2.2.23 VIN7-0 Voltage Reading Registers (Index=27h-20h)

Bit	R/W	Description
7-0	R	**Voltage Reading Value (VRV)**

9.6.2.2.24 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R	**VBAT Voltage Reading Value (VVRV)**

9.6.2.2.25 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R	**Temperature Reading Value (TRV)**

9.6.2.2.25.1 VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	**High Limit Value(HLV)**

9.6.2.2.26 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value(LLV)**

9.6.2.2.27 TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	**High Limit Value(HLV)**

9.6.2.2.28 TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	**Low Limit Value(LLV)**

9.6.2.2.29 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	**ADC VIN7-0 Scan Enable(ADCVSE)** 1: Enable 0: Disable

9.6.2.2.30 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	**Reserved**
5-3	R/W	**TMPIN Enable Thermal Mode(TETM)** TMPIN3-1 is enabled in the Thermal Resistor mode. 1: Enable 0: Disable
2-0	R/W	**TMPIN Enable Diode Mode(TEDM)** TMPIN3-1 is enabled in the Thermal Diode (or Diode-connected Transistor) mode. 1: Enable 0: Disable

9.6.2.2.31 TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Thermal Output Limit Value(TOLV)**

9.6.2.2.32 ADC Temperature Extra Channel Enable Register (Index=55h, Default=00h)

Bit	R/W	Description
7	R/W	**TEMPIN3 Temperature Reading Source Selection(TTRSS)** 0: TEMPIN3 thermal sensor 1: External Temperature Sensor Host
6-4	R/W	**FAN_CTRL2 PWM Base Clock Selection (FPWMCLKS)** 000: 48MHz (PWM Frequency=375kHz) 001: 24MHz(PWM Frequency=187.5kHz) 010: 12MHz(PWM Frequency=93.75kHz) 011: 8MHz(PWM Frequency=62.5kHz) 100: 6MHz(PWM Frequency=46.875kHz) 101: 3MHz(PWM Frequency=23.43kHz) 110: 1.5MHz(PWM Frequency=11.7kHz) 111: 0.75MHz(PWM Frequency=5.86kHz)
3	R/W	**Reserved** (Must be 0)
2-0	R/W	**VIN6-4 Thermal Resistor Mode(VTRM)** VIN6-4 is enabled in the Thermal Resistor mode. 0: Disable 1: Enable

9.6.2.2.33 Thermal Diode 1 Zero Degree Adjust Register (Index=56h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 1 Zero Degree Voltage Value(T1DZDV)**

9.6.2.2.34 Thermal Diode 2 Zero Degree Adjust Register (Index=57h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 2 Zero Degree Voltage Value(T2DZDV)**

9.6.2.2.35 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID; read only (IVID)**

9.6.2.2.36 Thermal Diode 3 Zero Degree Adjust Register (Index=59h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	**Thermal Diode 3 Zero Degree Voltage Value(T3DZDV)**

9.6.2.2.37 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	**ITE Vendor ID; read only (IVID)**

9.6.2.2.38 Beep Event Enable Register (Index=5Ch, Default=60h)

Bit	R/W	Description
7	R/W	**Thermal Diode Zero Degree Adjust Register Write Enable(TDZDARWA**) 1: Enable 0: Disable
6-4	R/W	**ADC Clock Selection (ADCS)**. 000: 500kHz 001: 250kHz 010: 125K 011: 62.5kHz 100: 31.25kHz 101: 24MHz 110: 1MHz(Default) 111: 2MHz
3	R/W	**Reserved**
2	R/W	**Beep Enable TMPIN Exceed(BETE)** This bit can enable the beep action when TMPINs exceed the limit.

Bit	R/W	Description
		1: Enable 0: Disable
1	R/W	**Beep Enable VIN Exceed(BEVE)** This bit can enable the beep action when VINs exceed the limit. 1: Enable 0: Disable
0	R/W	**Beep Enable FAN_TAC Exceed(BEFE)** This bit can enable the beep action when FAN_TACs exceed the limit. 1: Enable 0: Disable

9.6.2.2.39 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor(TD)** Tone=500/(bits[7:4]+1)
3-0	R/W	**Frequency Divisor(FD)** Frequency=10K/(bits[3:0]+1)

9.6.2.2.40 Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor(TD)** Tone=500/(bits[7:4]+1)
3-0	R/W	**Frequency Divisor(FD)** Frequency=10K/(bits[3:0]+1)

9.6.2.2.41 Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	**Tone Divisor(TD)** Tone=500/(bits[7:4]+1)
3-0	R/W	**Frequency Divisor(FD)** Frequency=10K/(bits[3:0]+1)

9.6.2.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan OFF(TLVFO)**

9.6.2.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	**Temperature Limit Value of Fan Start(TLVFS)**

9.6.2.2.44 FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers (Index=73h, 6Bh, 63h, Default=00h)

For Original Fan Control Mode:

Bit	R/W	Description
7	R/W	**Slope PWM Bit[6]** Please refer to FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h) on page 107 for the detail.
6-0	R/W	**Start PWM Value (SPWMV)**

9.6.2.2.45 FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h)

Bit	R/W	Description
7	R/W	**FAN Smoothing(FANSMT)** This bit enables the FAN PWM smoothing change. 1: Enable 0: Disable
6	R/W	**Reserved**
5-0	R/W	**Slope PWM Bit[5:0](SPWMB)** Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/℃

9.6.2.2.46 FAN_CTL3-1 SmartGuardian Automatic Mode △-Temperature Registers (Index=75h, 6Dh, 65h, Default=7Fh)

Bit	R/W	Description
7	R/W	**Reserved**
6-5	-	**Reserved**
4-0	R/W	**△-Temperature Interval [4:0](DeltaTI)**

9.6.2.2.47 External Temperature Sensor Host Status Register (Index=88h, Default=---00000b)

Bit	R/W	Description
7	R/W	**Reserved**
6	R/WC	**SST Bus Abnormal/Contention Error(SSTBAE)** This bit reports the SST/PECI line status. 0: No error 1: Abnormal/Contention error
5	R/WC	**SST Slave Message Phase T-bit Extends over Error(SSMTOE)** This bit reports the SST/PECI line status and receives error code (8000h-81FFh). 0: No error 1: Error found
4	R/WC	**SST/PECI Line High-Z Status/Failed(SLHS)** This bit reports the SST/PECI line High-Z status. 0: SST/PECI line does not drive High-Z. 1: SST/PECI line drives High-Z.
3	R/WC	**Write_FCS_ERR/ Bus Error(WFCSBE)** Writing “1” clears this bit. In the SST/PECI mode, it reports Write FCS error. 0: No Error 1: Write FCS error

Bit	R/W	Description
2	R/WC	**Read_FCS_ERR/ Device Error(RFEE)** In the SST/PECI mode, it reports Read FCS error. 0: No Error 1: Read FCS error
1	R/WC	**Finish (FNSH)** Writing "1" clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	**Host Busy (BUSY)** 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.6.2.2.48 External Temperature Sensor Host Target Address Register (Index=89h, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Target Address Register (HAddr [7:0])** This register is the Target Address field of the SST/PECI protocol.

9.6.2.2.49 External Temperature Sensor Host Write Length Register (Index=8Ah, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Write Length Register (HW_length [7:0])** This register is the Write Length field of the SST/PECI protocol.

9.6.2.2.50 External Temperature Sensor Host Read Length Register (Index=8Bh, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Read Length Register (HR_length [7:0])** This register is the Read Length field of the SST/PECI protocol.

9.6.2.2.51 External Temperature Sensor Host Command (Write Data 1) Register (Index=8Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	**Host Command Register (HCMD [7:0])** This register is the command field of the protocol. In the PECI/SST mode, it is the command (Write Data 1) byte.

9.6.2.2.52 External Temperature Sensor Write Data (2-8) Register (Index=8Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	**Write Data (2-8) [7:0] (in SST/PECI mode)** This is a 7-byte FIFO register and only valid in the PECI/SST mode.

9.6.2.2.53 External Temperature Sensor Host Control Register (Index=8Eh, Default=01h)

Bit	R/W	Description
7-6	R/W	**Auto-Start Control (Auto-START)** The host will start the transaction in a regular rate automatically. 00: 32 Hz 01: 16 Hz 10: 8 Hz 11: 4 Hz
5	R/W	**Auto-Start (Auto-START)** 1: Enable 0: Disable The host will start the transaction in a regular rate, which is determined by bit 7-6 automatically.
4	R/W	**SST/PECI Host Auto-abort at FCS Error(HAA)** This bit enables the SST/PECI host to abort the transaction when an error occurs to FCS. 1: Enable 0: Disable
3	R/W	**Data FIFO Pointer Clear(DFPC)** Writing “1” clears the Read/Write Data FIFO pointers. 0: No action It always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers cleared Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
2	R/W	**SST Contention Control(SCC)** This bit enables the SST bus contention control. 0: Disable 1: Enable When the SST bus is contentious, the host will abort the transaction.
1	R/W	**SST_idel_high** This bit sets the SST bus idle-high in the SST host mode. 0: SST idle low 1: SST idle high
0	R/W	**Start (START)** This bit is write-only. Writing 0 to it during transaction will issue a “kill process” and bit 4 of 8Bh register will be set. Writing 1 to it during the “NOT BUSY” state (bit 0 of 88h=0) will start a transaction. Writing 1 to it during the “BUSY” state (bit 0 of 88h=1) will not issue any transaction. So, the programmer should check the “BUSY” status before issuing a transaction. 0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.

9.6.3 Operation

9.6.3.1 Power on Reset and Software Reset

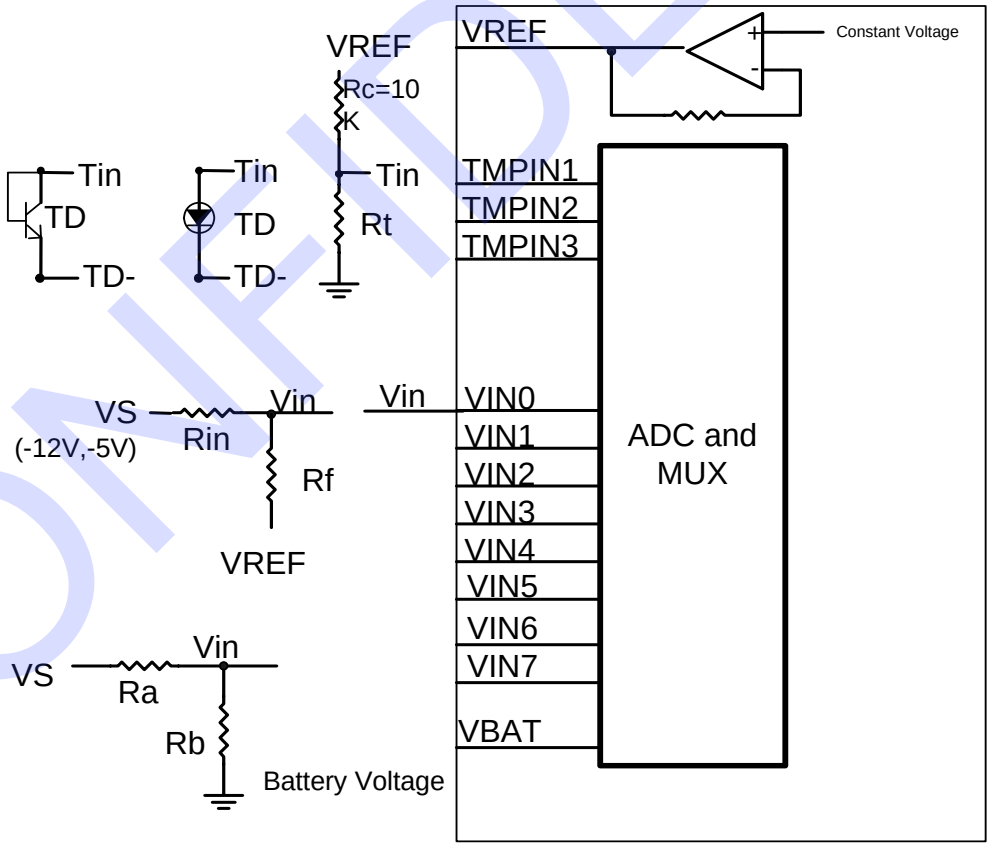
When the system power is first applied, the Environment Controller performs “power on reset” on the registers, making them return to their individual default values during a system hardware reset, and the EC will acquire a monitored value before it goes inactive. The ADC is activated to monitor the VBAT pin and then goes inactive. A software reset through bit 7 of Configuration Register (Index=00h, Default=18h) (refer to page 97) performs the same functions as the hardware reset except the function of the Serial Bus Interface Address register.

9.6.3.2 Starting Conversion

The monitoring function in the EC is activated when bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, this function will be enabled by setting several enabled bits, which are categorized into three groups, positive voltages, temperatures and FAN Tachometer inputs. Before the EC monitoring function is able to be executed then the monitoring process can then be started.

1. Set the limits.
2. Set the interrupt masks.
3. Set the enable bits.

Figure 9-4. Application Example



Note: The resistor should provide approximately 2V at the Analog Inputs.

9.6.3.3 Voltage and Temperature Inputs

The 8-bit ADC has a 16mV LSB with an input range from 0V to 4.096V. The 2.5V and 3.3V supplies of PC applications can be directly connected to the inputs. It is necessary to divide the 5V and 12V inputs into an acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider, which is connected to VREF (constant voltage, 4.096V), and do not attempt to measure it with the divider connected to the ground. The EC temperature measurement system converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage, an external thermistor, a constant resistance, the ADC and a conversion table ROM..

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated below:

Positive Voltage: Vs = Vin X (Ra+Rb) / Rb
Negative Voltage: Vs = (1+Rin/Rf) X Vin – (Rin/Rf) X VREF

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground; nevertheless, the current limiting input resistor is recommended since no dividing circuit is available.

9.6.3.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is essential to achieve accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as closely as possible to IT8783E/F. However, the thermistors of the temperature loops should be positioned within the measuring area. In addition, the power supply bypass and the parallel combination of 10μF and 0.1μF bypass capacitors connected between VCC and analog ground also need to be located as closely as possible to IT8783E/F.

Due to the small differential voltage of thermal diode (diode-connected transistor), designers should adhere to the following PCB layout:

- Position the sensor as closely as possible to the EC.
- The sensor ground should be directly shorted to GNDA with excellent noise immunity.
- Keep traces away from any noise sources. (High voltage, fast data bus, fast clock , CRTs …)
- Use trace width of 10 mil minimum and provide guard ground (flanking and under)
- Position 0.1μF bypass capacitors as closely as possible to IT8783E/F.

9.6.3.5 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or 16-bit counter (maximum count=255 or 65535) for one period of the input signals. Counts are based on two pulses per revolution for tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor) ; (Default Divisor = 2)

The maximum input signal range is from 0 to VCC. An additional external circuit is needed to clamp the input voltage and current.

9.6.3.6 Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled by Configuration Register (Index=00h, Default=18h) (refer to page 97). The Interrupt Status Registers will be reset after a read operation. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. It takes EC 1.5 seconds to allow all the EC Registers to be safely updated between completed read operations. When bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume after this bit is cleared.

All analog voltage inputs have both high and low Limit Registers to generate interrupts whereas FAN monitoring inputs only have low Limit Register to warn the host. The IT8783E/F provides three modes dedicated to temperature interrupts in the EC: “Interrupt” mode, “Enhanced Interrupt” mode and “Comparator” mode.

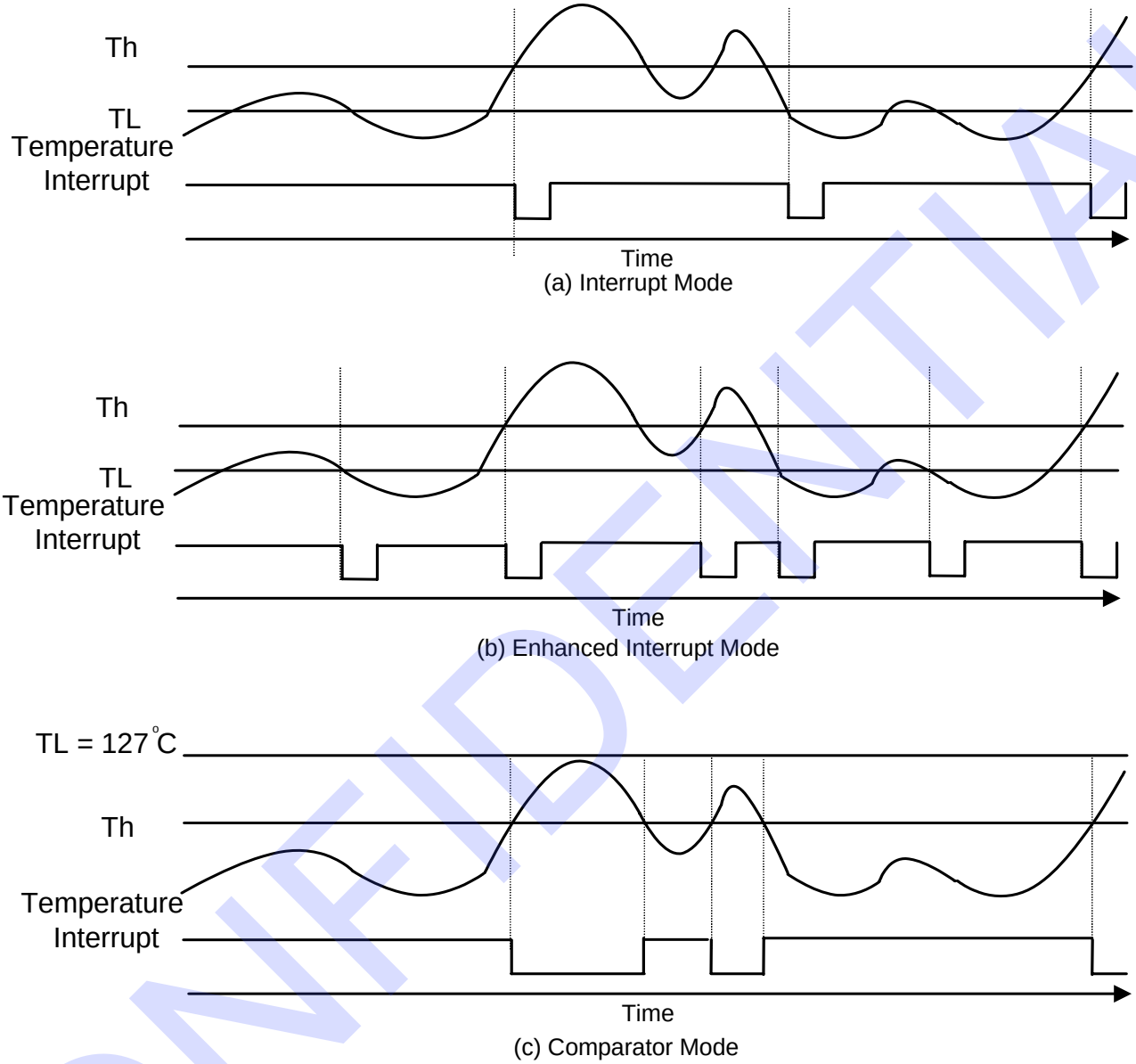
Interrupt Mode
An interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 98). Once an interrupt event occurs by exceeding Th limit, an interrupt will only occur again when the temperature goes below TL limit after being reset. Again, it will set the corresponding status bit to high until being reset by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 98).

Enhanced Interrupt Mode
When the enhanced interrupt mode is enabled (bit 3, 6 and 7 of EC index 0Ch for TMPIN1, 2, and 3 respectively), an interrupt will be generated when the temperature is higher than the high limit or lower than the low limit.

When the enhanced interrupt mode is enabled (bit 3, 6 and 7 of Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h) for TMPIN1, 2, and 3 respectively) (refer to page 100), an interrupt will be generated when the temperature is higher than the high limit or lower than the low limit.

Comparator Mode
This mode is entered when the TL limit register is set to 127°C. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading Interrupt Status Register 3 (Index=03h, Default=00h) (refer to page 98), but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

Figure 9-5. Temperature Interrupt Response Diagram



9.6.3.7 FAN Controller FAN_CTL's ON-OFF and SmartGuardian Modes

The IT8783E/F provides an advanced FAN Controller. Two modes, ON_OFF and SmartGuardian, are provided for each controller. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application circuits, the FAN's voltage values can be varied easily.

In the SmartGuardian Mode, there is only one operational choice, software control.

While under software control, the PWM value is subject to the changes in the values of bit 6-0 of FAN_CTL 1-3 PWM Control Registers (Index=15h, 16h, 17h). With the application circuits, FAN_CTL can generate 128 steps of voltage. So, FAN_CTL 1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speeds or other voltage control cooling devices can be varied in 128 steps.

9.7 Floppy Disk Controller (FDC)

9.7.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in the PC/AT mode and supports the 3-mode type drive. Additionally, the FDC is software compatible with the 82077.

The FDC can be configured by software and a set of configuration registers. The status, data, and control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors of the data or operation of the FDC/FDD.

The controller manages data transfer using a set of data transfer and control commands, which are processed in three phases, Command, Execution, and Result, but not all of them will be utilized.

9.7.2 Reset

The IT8783E/F device implements both software and hardware reset options for the FDC. Either option will reset the FDC, terminating all operations and making the FDC entering an idle state. A reset during a write to the disk will disorder the data and the corresponding CRC.

9.7.3 Hardware Reset (LRESET# Pin)

When the FDC receives an LRESET# signal, all registers of the FDC core will be cleared, except those programmed by the SPECIFY command. To exit the reset state, the host must clear the DOR bit.

9.7.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core will be cleared. A reset performed by setting the reset bit in the DOR has a higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit will be self-cleared when the host clears the DOR bit.

9.7.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is to separate the encoded clock from data pulses.

9.7.6 Write Precompensation

Write precompensation is a method to adjust the effects of bit shifting on data as it is written to the disk. It is harder for the data separator to read data that have been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions.

Write precompensation can be selected by bit 4-2 of Data Rate Select Register (DSR, FDC Base Address + 04h) (refer to page 117).

9.7.7 Data Rate Selection

Selecting one of the four possible data rates for the floppy disk can be achieved by setting bit 1-0 of Data Rate Select Register (DSR, FDC Base Address + 04h) (refer to page 117) or Diskette Control Register (DCR, FDC Base Address + 07h) (refer to page 119). The data rate is determined by the last value written to either DSR or DCR. After the data rate is set, the data separator clock will be scaled appropriately.

9.7.8 Status, Data and Control Registers

9.7.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register, which controls drive selection as well as motor, software reset, and DMA enable. The I/O interface reset may be used anytime to clear DOR's contents.

Bit	Symbol	Description
7-6	-	**Reserved**
5	MOTB EN	**Drive B Motor Enable(MOTBEN)** 1: Enable 0: Disable
4	MOTA EN	**Drive A Motor Enable(MOTAEN)** 1: Enable 0: Disable
3	DMAEN	**Disk Interrupt and DMA Enable(DMAEN)** 1: Enable 0: Disable (DRQx, DACKx#, TC and INTx)
2	RESET#	**FDC Function Reset(RESET)** 0: Function reset 1: Function of reset cleared This reset has no impact on the DSR, DCR or DOR.
1	-	**Reserved**
0	DVSEL	**Drive Selection(DVSEL)** 0: Drive A selected 1: Drive B selected

9.7.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register compatible with 82077 software. The contents of this register are not used internally for the device.

Bit	Symbol	Description
7-2	-	**Reserved**
1-0	TP_SEL[1:0]	**Tape Drive Selection(TPSEL)** TP_SEL[1:0]: Drive selected 00: None 01: 1 10: 2 11: 3

9.7.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register, which indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except

when it is in the DMA mode.

Bit	Symbol	Description
7	RQM	**Request for Master(RQM)** 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and can receive data from the host.
6	DIO	**Data I/O Direction(DIO)** It indicates the direction of data transfer once an RQM has been set. 0: Write 1: Read
5	NDM	**Non-DMA Mode(NDM)** 0: DMA mode selected 1: Non-DMA mode selected This mode is selected via the SPECIFY command during the command Execution phase.
4	CB	**Diskette Control Busy(CB)** It indicates whether a command is in progress (FDD busy) or not. 0: A command has been executed and the end of the Result phase reached. 1: A command is being executed.
3-2	-	**Reserved**
1	DBB	**Drive B Busy(DBB)** It indicates whether Drive B is in the SEEK portion of a command. 0: Not busy 1: Busy
0	DAB	**Drive A Busy(DAB)** It indicates whether Drive A is in the SEEK portion of a command. 0: Not busy 1: Busy

9.7.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register, which determines the data rate, write precompensation selection, power-down mode, and software reset. The data rate of the FDC is determined by the last value written to either DSR or DCR. The DSR is unaffected by a software reset and can be set to “02h” by a hardware reset. The “02h” represents the default precompensation, and 250 Kbps indicates the data transfer rate.

Bit	Symbol	Description
7	S/W RESET	**Software Reset(SWRESET)** It is active high and has the same function as the RESET# of the DOR except that this bit is self-cleared.
6	POWER DOWN	**Power-Down(POWERDOWN)** When “1” is written to this bit, the FDC will enter the manually low-power mode. The clocks of the FDC and data separator circuits will be turned off until software reset, Data Register or Main Status Register is accessed.
5	-	**Reserved**
4-2	PRE-COMP 2-0	**Precompensation Select(PRECOMP)** These three bits are to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default of the starting track number, which can be changed by the CONFIGURE command for precompensation. **PRE_COMP** | **Precompensation Delay**

Bit	Symbol	Description
		111 0.0 ns 001 41.7 ns 010 83.3 ns 011 125.0 ns 100 166.7 ns 101 208.3 ns 110 250.0 ns 000 Default **Default Precompensation Delay** **Data Rate** / **Precompensation Delay** 1 Mbps 41.7 ns 500 Kbps 125.0 ns 300 Kbps 125.0 ns 250 Kbps 125.0 ns
1-0	DRATE1-0	**Data Rate Select(DRATE)** **Bit 1-0** / **Data Transfer Rate** 00 500 Kbps 01 300 Kbps **10 250 Kbps (Default)** 11 1 Mbps

9.7.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register, which transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer the information or status to the data bus at a time.

Bit	Symbol	Description
7-0	-	**Data(DATA)** Command information, diskette drive status, or result phase status data.

9.7.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register, which shares this address with Diskette Control Register (DCR, FDC Base Address + 07h).

Bit	Symbol	Description
7	DSKCHG	**Diskette Change(DSKCHG)** It indicates the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	**Reserved**

9.7.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register, which shares this address with Digital Input Register (DIR, FDC Base Address + 07h) and controls the data transfer rate for the FDC.

Bit	Symbol	Description
7-2	-	**Reserved** Always 0
1-0	DRATE1-0	**Data Rate Select(DRATE)** **Bit 1-0** — **Data Transfer Rate** 00 — 500 Kbps 01 — 300 Kbps 10 — 250 Kbps 11 — 1 Mbps

9.7.9 Controller Phases

The FDC is to process data transfer and control commands in three phases, Command, Execution and Result, and not all of them will be utilized.

9.7.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that Main Status Register (MSR, FDC Base Address + 04h) bit 7 (RQM) = 1 and bit 6 (DIO) = 0 (refer to page 116), indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. Refer to section 9.7.11 Data Transfer Command on page 132 and 9.7.12 Control Command on page 135 for details of various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.7.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfer occurs between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in the DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.7.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. Bit 7 (RQM) and bit 6 (DIO) of Main Status Register (MSR, FDC Base Address + 04h) must equal 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.7.9.4 Result Phase Status Registers

For commands containing a Result phase, these **read only** registers indicate the status of the latest executed command.

Table 9-4. Status Register 0 (ST0)

Bit	Symbol	Description
7-6	IC	**Interrupt Code(IC)** 00: The execution of the command has been completed successfully. 01: The execution of the command is activated but fails to be completed successfully. 10: It means an invalid command. 11: The execution of the command is not completed successfully due to a polling error.
5	SE	**Seek End(SE)** The FDC executes a SEEK or RE-CALIBRATE command.
4	EC	**Equipment Check(EC)** The TRK0# pin is not set after a RE-CALIBRATE command is issued.
3	NU	**Not Used(NU)**
2	H	**Head Address(HA)** The current head address
1	DSB	**Drive B Select(DSB)** 0: Disable 1: Enable
0	DSA	**Drive A Select(DSA)** 0: Disable 1: Enable

Table 9-5. Status Register 1 (ST1)

Bit	Symbol	Description
7	EN	**End of Cylinder(EN)** It indicates the FDC attempts to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	NU	**Not Used(NU)**
5	DE	**Data Error(DE)** A CRC error occurs in either the ID field or the data field of a sector.
4	OR	**Overrun / Underrun(OR)** An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by CPU or DMA within the required time interval.
3	NU	**Not Used(NU)**
2	ND	**No Data(ND)** No data are available for the FDC when any of the following conditions occurs: • The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are being executed. • While a READ ID command is being executed, an error occurs upon reading the ID field. • While a READ A TRACK command is being executed, the FDC cannot find the starting sector.
1	NW	**Not Writeable(NW)** It is set when WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	**Missing Address Mark(MA)** This flag bit is set when either of the following conditions is met: • The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track. • The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin.

Table 9-6. Status Register 2 (ST2)

Bit	Symbol	Description
7	NU	**Not Used(NU)**
6	CM	**Control Mark(CM)** This flag bit is set when either of the following conditions is met: • The FDC finds a Deleted Data Address Mark during a READ DATA command. • The FDC finds a Data Address Mark during a READ DELETED DATA command.
5	DD	**Data Error in Data Field(DD)** This flag bit is set when a CRC error is found in the data field.
4	WC	**Wrong Cylinder(WC)** This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	**Scan Equal Hit(SH)** This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	**Scan Not Satisfied(SN)** This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.

Bit	Symbol	Description
1	BC	**Bad Cylinder(BC)** This flag bit is set when the track address equals to “FFh” and is different from the track address in the FDC.
0	MD	**Missing Data Address Mark(MD)** This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-7. Status Register 3 (ST3)

Bit	Symbol	Description
7	FT	**Fault(FT)** It indicates the current status of the Fault signal from the FDD.
6	WP	**Write Protect(WP)** It indicates the current status of the Write Protect signal from the FDD.
5	RDY	**Ready(RDY)** It indicates the current status of the Ready signal from the FDD.
4	TK0	**Track 0(TK0)** It indicates the current status of the Track 0 signal from the FDD.
3	TS	**Two Side(TS)** It indicates the current status of the Two Side signal from the FDD.
2	HD	**Head Address(HD)** It indicates the current status of the Head Address signal to the FDD.
1-0	US1, US0	**Unit Select(US)** It indicates the current status of the Unit Select signal to the FDD.

9.7.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte containing the op-code and a series of additional bytes containing the required set of parameters and results. For the description of the common set of parameter byte symbols, please refer to the following table. The FDC commands may be executed whenever it is in the Command phase and will check whether the first byte is a valid command or not. If yes, it will proceed. If not, an interrupt will be issued.

Table 9-8. Command Set Symbol

Symbol	Description
C	**Cylinder Number(CN)** The current/selected cylinder (track) number, 0-255.
D	**Data(D)** The data pattern to be written into a sector.
DC3–DC0	**Drive Configuration Bit3-0(DC)** Designate which drives are the perpendicular drives on the PERPENDICULAR MODE command.
DIR	**Direction Control(DIR)** Head Step Direction Control of Read/Write. 0: Step out 1: Step in
DR0, DR1	**Disk Drive Selection(DR)** The selected drive number, 0 or 1.
DTL	**Data Length(DTL)** When N is defined as 00h, DTL designates the number of data bytes to be read out or written into the Sector. When N is not 00h, DTL is undefined.

Symbol	Description
DFIFO	**Disable FIFO(DFIFO)** 0: Enable 1: Disable (Default)
EC	**Enable Count(EC)** If EC=1, DTL of VERIFY command will be SC.
EIS	**Enable Implied Seek(EIS)** If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	**End of Track(EOT)** This is the final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	**Gap 2 Length(GAP)** By PERPENDICULAR MODE command, this parameter changes the length format of Gap 2.
GPL	**Gap Length(GPL)** During a FORMAT command, it determines the length of Gap 3.
H	**Head Address(H)** The Head number, 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	**Head(HD)** The selected Head number, 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	**Head Load Time(HLT)** The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	**Head Unload Time(HUT)** The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK	**LOCK(LOCK)** If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.
MFM	**FM or MFM Mode(MFM)** If MFM is low, FM mode (single density) is selected. If MFM is high, MFM mode (double density) is selected.
MT	**Multi-Track(MT)** If MT is high, a Multi-Track operation will be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation in the last sector on side 0.
N	**Number(N)** The number of data bytes written into a sector, where: 00: 128 bytes (PC standard) 01: 256 bytes 02: 512 bytes … 07: 16 Kbytes
NCN	**New Cylinder Number(NCN)** A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	**Non-DMA Mode(ND)** When ND is high, the FDC operates in the Non-DMA mode.
OW	**Overwrite(OW)** If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.

Symbol	Description
PCN	**Present Cylinder Number(PCN)** This is the cylinder number at the completion of a SENSE INTERRUPT STATUS command, indicating the present head position
POLLD	**Polling Disable(POLLD)** If POLLD=1, the internal polling routine is disabled.
PRETRK	**Precompensation Starting Track Number(PRETRK)** Programmable from track 0-255.
R	**Record(R)** The sector number to be read or written.
RCN	**Relative Cylinder Number(RCN)** To determine the relative cylinder offset from the present cylinder used by the RELATIVE SEEK command.
SC	**Number of Sector Per Cylinder(SC)**
SK	**Skip(SK)** If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Otherwise, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	**Step Rate Time(SRT)** The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The stepping rate is applied to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	**Status 0(ST0)** **Status 1(ST1)** **Status 2(ST2)** **Status 3(ST3)** ST0-3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (MSR, FDC Base Address + 04h) (refer to page 116) (selected by A0 = 0). ST0-3 may be read only after a command has been executed and contains information associated with that particular command.
STP	**STP** If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-9. Command Set Summary

READ DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

FORMAT A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution	W	C								Input Sector Parameters per-sector FDC formats an entire cylinder
	W	H								
	W	R								
	W	N								
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

SCAN EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

VERIFY									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ ID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information during execution phase
	R	H								
	R	R								
	R	N								

CONFIGURE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	1	DIR	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	R	0	DIS	DFIFO	POLLD	FIFOTHR				
	R	PRETRK								

LOCK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

VERSION										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each SEEK operation
	R	PCN								

SENSE DRIVE STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Result	R	ST3								Status information about FDD

SPECIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

PERPENDICULAR MODE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into the standby state)
Result	R	ST0								ST0 = 80h

9.7.11 Data Transfer Command

All data transfer commands utilize bytes with the same parameter (except for FORMAT A TRACK command) and return data bytes with the same result. The only difference between them is the five bits (bit0 - bit4) of the first byte.

9.7.11.1 READ DATA Command

The READ DATA command contains nine command bytes that make the FDC enter the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. After the data from the given sector are read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector are read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops sending data, but continues reading data from the current sector and checks the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:

Sector Size = $2^{(7+N\ value)}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, set the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If it occurs to a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operations, the FDC can also perform Multi-Track Read operations. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-10 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-10. Effects of MT and N Bit

MT	N	Maximum Data Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X16 =16384	16 on side 1

9.7.11.2 READ DELETED DATA Command

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.7.11.3 READ A TRACK Command

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowable under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark is found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

9.7.11.4 WRITE DATA Command

The WRITE DATA command contains nine command bytes that make the FDC enter the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data fields with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC

will set the IC code in the ST0 to 01 and the DE bit in the ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.7.11.5 WRITE DELETED DATA Command

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.7.11.6 FORMAT A TRACK Command

The FORMAT A TRACK command is to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) required to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.7.11.7 SCAN Command

The SCAN command allows the data read from the disk to be compared with the data sent from the system. Followings are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The execution of SCAN command will not be terminated until the scan condition has been met, EOT has been reached, or TC is asserted. Read errors on the disk have the same error condition as that for the READ DATA command. If the SK bit is set, sectors with Deleted Data Address Marks are ignored. If all sectors' read is skipped, the command terminates with D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 9-11. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.7.11.8 VERIFY Command

The VERIFY command is to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data are transferred to the host. This command is designed for post-format or post-write verification. Data are read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data are transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value is equal to the final sector to be checked.

Table 9-12. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

9.7.12 Control Command

The control commands do not transfer any data and are used to monitor and manage the data transfer instead. Three of them, READ ID, RE-CALIBRATE and SEEK, will generate an interrupt after data transfer is completed. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

9.7.12.1 READ ID Command

The READ ID command is to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark before the second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.7.12.2 CONFIGURE Command

The CONFIGURE command determines some specific operation modes of the controller and does not need to be issued if the default values of the controller meet the system requirements.

EIS: Enable Implied Seek. A SEEK operation is performed before a READ, WRITE, SCAN, or VERIFY command.
0: Disable (Default)
1: Enable

DFIFO: Disable FIFO.
0: Enable
1: Disable (Default)

POLLD: Disable polling of drives.
0: Enable (Default) When enabled, a single interrupt is generated after a reset.
1: Disable

FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 byte to 16 bytes). The default is 1 byte.

PRETRK: The Precompensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). The default is track 0.

9.7.12.3 RE-CALIBRATE Command

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, SE [and EC bits] of the ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 to high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and the drives attached.

9.7.12.4 SEEK Command

The SEEK command controls the FDC read/write head movement from one track to the other. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head if required. The direction of movement is determined by the followings:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses.
PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses.
PCN = NCN — Terminate the command by setting the ST0 SE bit to 1.

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.7.12.5 RELATIVE SEEK Command

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is to determine whether to step in or out. RCN (Relative Cylinder Number) is to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other commands except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.7.12.6 DUMPREG Command

The DUMPREG command is designed for system run-time diagnostics, application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of the parameter set in other commands.

9.7.12.7 LOCK Command

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters of DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after a software reset.

9.7.12.8 VERSION Command

The VERSION command is to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.7.12.9 SENSE INTERRUPT STATUS Command

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of the ST0, as shown in Table 9-13. Interrupt Identification below.

It is necessary to generate an interrupt under any of the following conditions:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (without Result phase)
- When a data transfer is required during Execution phase in the non-DMA mode

Table 9-13. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling
1	00	Normal termination of SEEK or RE-CALIBRATE command
1	01	Abnormal termination of SEEK or RE-CALIBRATE command

9.7.12.10 SENSE DRIVE STATUS Command

The SENSE DRIVE STATUS command is to acquire drive status information and there is no Execution phase for this command.

9.7.12.11 SPECIFY Command

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in the following three tables respectively. The FDC is operated in DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-14. HUT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
-	-	-	-	-
E	112	224	373	448
F	120	240	400	480

Table 9-15. SRT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
-	-	-	-	-
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-16. HLT Value

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
-	-	-	-	-
7E	126	252	420	504
7F	127	254	423	508

9.7.12.12 PERPENDICULAR MODE Command

The PERPENDICULAR MODE command is to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operate in “Extra High Density” mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used (not set to 00), the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to the Perpendicular mode. DC3-DC0 are unaffected by a software reset, but

WG and GAP are both cleared to 0 after a software reset.

Table 9-17. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-18. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional	22 bytes	0 bytes
	Perpendicular	22 bytes	19 bytes
1 Mbps	Conventional	22 bytes	0 bytes
	Perpendicular	41 bytes	38 bytes

9.7.12.13 INVALID Command

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set Main Status Register (MSR, FDC Base Address + 04h) bit 7 (RQM) and bit 6 (DIO) to 1 (refer to page 116) and terminate the command without issuing an interrupt.

9.7.13 DMA Transfer

DMA transfer is enabled by the SPECIFY command and initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycle.

9.7.14 Low-Power Mode

When writing “1” to bit 6 of Data Rate Select Register (DSR, FDC Base Address + 04h) (refer to page 117), the controller will enter the low-power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit, will be gated. The FDC can be resumed from the low-power state in two ways. One is a software reset via the DOR or DSR, and the other is a read or write to either the Data Register or Main Status Register. The latter is preferred since all internal register values are retained.

9.8 Serial Port (UART)

The IT8783E/F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-19. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.8.1 Data Registers

The Receiver Buffer Register (RBR) and Transmitter Buffer Register (TBR)individually hold five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. Bit 0 of any word is first received and transmitted.

9.8.1.1 Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

9.8.1.2 Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before data transmission.

9.8.2 Control Register

9.8.2.1 Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is to enable or disable four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Bit	Default	Description

7-4	-	**Reserved**
3	0	**Enable Modem Status Interrupt(EMSI)** Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt(ERLSI)** Set this bit high to enable the receiver line status interrupt, which happens when overrun, parity, framing or break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt(ETHREI)** Set this bit high to enable the transmitter holding register empty interrupt.
0	0	**Enable Received Data Available Interrupt(ERDAI)** Set this bit high to enable the received data available interrupt and time-out interrupt in the FIFO mode.

9.8.2.2 Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine the interrupt priority and its source. The four existing interrupts are listed below in priority order.

4. Receiver Line Status (highest priority)
5. Received Data Ready
6. Transmitter Holding Register Empty
7. Modem Status (lowest priority)

When a privileged interrupt is pending and the interrupt type is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the Host. Any new interrupts will not be acknowledged until the Host access is completed. Please refer to Table 9-20. Interrupt Identification Register on page 142 for the detail.

Table 9-20. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Function			
Bit 3	Bit 2	Bit 1	Bit 0	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last four character times and there is at least one character in it during this period.	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not Defined
IIR(7), IIR(6): Set when FCR(0) = 1.
IIR(5), IIR(4): Always logic 0.
IIR(3): In the non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
IIR(2), IIR(1): Used to identify the highest priority interrupt pending.
IR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

9.8.2.3 FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to not only enable and clear the FIFO but also set the RCVR FIFO trigger level.

Bit	Default	Description
7-6	-	**Receiver Trigger Level Selection** These bits are to set the trigger level for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	**Reserved** (This bit does not affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.)
2	0	**Transmitter FIFO Reset(TFR)** This self-cleared bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1".
1	0	**Receiver FIFO Reset(RFR)** Setting this self-cleared bit to a logic "1" will clear all contents of the RCVR FIFO and resets its related counter to "0" (except the shift register).
0	0	**FIFO Enable(FIFOE)** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT whereas disabled and cleared respectively when this bit is cleared to low. This bit must be a logic "1" if data are written to the other bits of the FCR, or they will not be properly programmed. When this register is switched to the non-FIFO mode, all of its contents will be cleared.

Table 9-21. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

9.8.2.4 Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in 16-bit binary format. They are loaded during initialization to generate a desired baud rate.

9.8.2.5 Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG, which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The number of DLL or DLM is in 16-bit format, providing the divisor ranging from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-22. Baud Rate Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

9.8.2.6 Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

9.8.2.7 Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line.

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** This bit must be set high to access the Divisor Latches of the baud rate generator during READ or WRITE operation whereas set low to access Data Registers (refer to page 140) or Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 140).
6	0	**Set Break(SB)** This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, which will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	**Stick Parity(SP)** When this bit and LCR(3) are high at the same time, the parity bit is transmitted and then detected by a receiver in an opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Selection(EPS)**

		When the parity is enabled (LCR(3) = 1), 0: Odd parity 1: Even parity
3	0	**Parity Enable(PE)** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bit (NSB)** This bit specifies the number of stop bit in each serial character, as summarized in Table 9-23. Stop Bit Number Encoding on page 145.
1-0	00	**Word Length Select [1:0](WLS)** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-23. Stop Bit Number Encoding

LCR (2)	Word Length	No. of Stop Bit
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

9.8.2.8 Modem Control Register (MCR) (Read/Write, Address offset=4)

This register controls the interface by the modem or data set (or device emulating a modem).

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loopback(IL)** This bit provides a loopback feature for diagnostic test of the serial channel when set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high then the transmitted data are immediately received, allowing the processor to verify the transmitted and received data path of the serial channel.
3	0	**OUT2(OUT2)** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	**OUT1(OUT1)** This bit does not have an output pin and can only be read or written by CPU.
1	0	**Request to Send (RTS)** This bit controls the Request to Send (RTS#), which is in an inverse logic state with that of MCR(1).
0	0	**Data Terminal Ready (DTR)** This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with that of the MCR(0).

9.8.3 Status Register

9.8.3.1 Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides the status indication and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel.

Bit	Default	Description
7	0	**Error in Receiver FIFO(ERF)** In the 16450 mode, this bit is always 0 whereas in FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit will be cleared when CPU reads LSR if there are no subsequent errors in FIFO.
6	1	**Transmitter Empty(TE)** This **read only** bit indicates that the Transmitter Holding Register (THR) and Transmitter Shift Register are both empty. Otherwise, this bit is "0" and has the same function as that in FIFO mode.
5	1	**Transmitter Holding Register Empty(THRE)** This **read only** bit indicates that the Transmitter Buffer Register (TBR) is empty and ready to accept a new character for transmission. It is set high when a character is transferred from Transmitter Holding Register (THR) into Transmitter Shift Register, causing priority 3 interrupt (THRE) of Interrupt Identification Register (IIR) (Read only, Address offset=2) (refer to page 141), which is cleared by a read of IIR. In FIFO mode, it is set when XMIT FIFO is empty whereas cleared when at least one byte is written to XMIT FIFO.
4	0	**Line Break(LB)** The Line Break (LB) Interrupt status bit indicates that the last character received is a break character, which is invalid but complete. It includes parity and stop bits. This situation occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in IIR, with bit 2 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) previously enabled(refer to page 140).
3	0	**Framing Error(FE)** A logic 1 indicates that the stop bit in the received character is not valid. It will be reset low when CPU reads the contents of the LSR.
2	0	**Parity Error(PE)** A logic 1 indicates that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever LSR is read by CPU.
1	0	**Overrun Error(OE)** A logic 1 indicates that the RBR has been overwritten by the next character before it had been read by CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when LSR is read by the CPU.
0	0	**Data Ready(DR)** A "1" indicates a character has been received by the RBR. A logic "0" indicates all the data in RBR or RCVR FIFO have been read.

9.8.3.2 Modem Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits, MSR(4) - MSR(7), can provide the state change information when the modem control input changes the state. It is reset low when the Host reads the MSR.

Bit	Default	Description
7	0	**Data Carrier Detect(DCD)** It indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator(RI)** It indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready(DSR)** It indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# of MCR.
4	0	**Clear to Send(CTS)** It indicates the complement of CTS# input. When the serial channel is in the Loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# of MCR.
3	0	**Delta Data Carrier Detect(DDCD)** It indicates that the DCD# input state has been changed since being read by the Host last time.
2	0	**Trailing Edge Ring Indicator(TERI)** It indicates that the RI input state to the serial channel has been changed from low to high since being read by the Host last time. The change in a logic “1” does not activate the TERI.
1	0	**Delta Data Set Ready(DDSR)** A logic "1" indicates that the DSR# input state to the serial channel has been changed since being read by the Host last time.
0	0	**Delta Clear to Send(DCTS)** This bit indicates the CTS# input to the chip has changed the state since MSR was read last time.

9.8.4 Reset

The reset of the IT8783F/E should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the internal clock counters of transmitter and receiver.

Table 9-24. Reset Control of Register and Pinout Signal

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high; others are low
Modem Status Register	Reset	
SOUT1, SOUT2	Reset	Bits 0-3 low; bits 4-7 input signals
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High
		High Impedance

9.8.5 Programming

Each serial channel of the IT8783E/F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though these control registers can be written in any given order, the IER should be the last register written because it controls whether the interrupt is enabled or not. After the port is programmed, these registers still can be updated whenever the port does not transfer data.

9.8.6 Software Reset

This approach allows the serial port to return to a completely known state without a system reset. It is achieved by writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.8.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

9.8.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 143) and bit 0 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 140) high, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The receive data available interrupt will be issued only when the FIFO has reached its programmed trigger level and cleared as soon as the FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the Host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from RCVR FIFO.

For the RCVR FIFO time-out interrupt, it will occur under the following conditions by enabling the RCVR FIFO and receiver interrupts:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in FIFO whenever the interval between the most recently received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the Host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FIFO Control Register (FCR) (Write Only, Address offset=2) (refer to page 143) and bit 1 of Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0) (refer to page 140) high, the XMIT FIFO and transmitter interrupts are enabled. The XMIT interrupt occurs under the following conditions:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed for one character time minus the last stop bit time whenever the following condition occurs:

   THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication will be delayed for one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts have the same priority as the received data available interrupt. The XMIT FIFO empty has the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via LSR described below:

LSR(7): RCVR FIFO error indication
LSR(6): XMIT FIFO and Shift register empty
LSR(5): The XMIT FIFO empty indication

LSR(4) - LSR(1): Specify that errors have occurred. The character error status is handled in the same way as that in the interrupt mode. The IIR is not affected since IER(2)=0.
LSR(0): High whenever RCVR FIFO contains at least one byte.
No trigger level is reached or time-out condition indicated in FIFO Polled Mode.

9.9 Consumer Remote Control (TV Remote) IR (CIR)

9.9.1 Overview

CIR is applied to the consumer remote control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisors and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

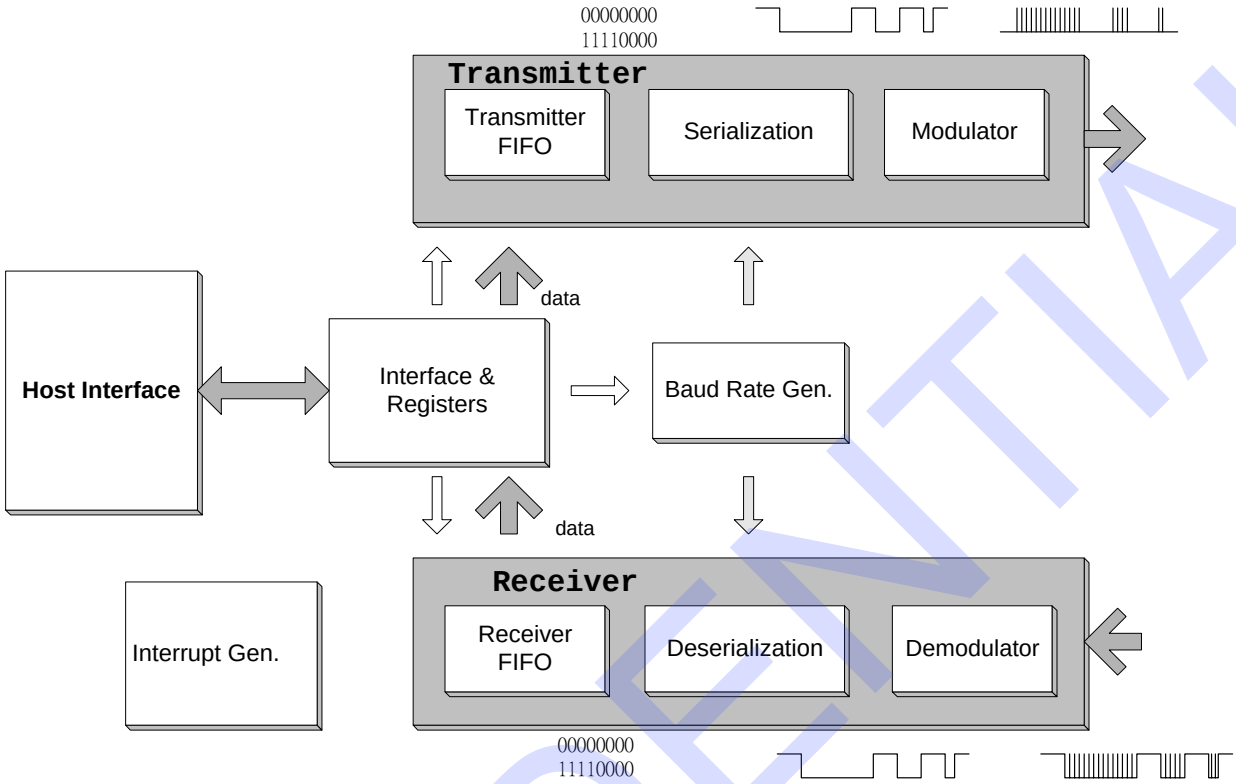
9.9.2 Features

- Supports 30 kHz - 57 kHz (low frequency) or 400 kHz – 500 kHz (high frequency) carrier transmission
- Baud rate up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral function
- 32-byte FIFO for data transmission or data reception

9.9.3 Block Diagram

CIR consists of two parts, transmitter and receiver. Regarding the transmitter, it is responsible for transmitting data to FIFO, processing FIFO data by serialization and modulation and sending out data through the LED device. As for the receiver, it is responsible for receiving data, processing data by demodulation and deserialization and storing data in the Receiver FIFO.

Figure 9-6. CIR Block Diagram



9.9.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with the carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can be started, code byte write operation must be performed to the Transmitter FIFO DR. The bit TXRLE in the TCR1 should be set to "1" before the run-length decode data can be written into the Transmitter FIFO. Setting TXENDF in the TCR1 will enable the data transmission deferral, and avoid the transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers, BDLR and BDHR. When the two bits, HCFS and CFQ[4:0], are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bit TXMPM[1:0] and TXMPW[2:0] specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic "0" can activate the Transmitter LED in the format of a series of modulating pulses.

9.9.5 Receive Operation

The Receiver function will be enabled if bit RXEN in RCR is set to "1". Either demodulated or modulated RX# signal is loaded into Receiver FIFO, and bit RXEND in RCR determines whether the demodulation logic should be used or not. It determines the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequency by programming bit HCFS and CFQ[4:0]. Set RDWOS to "0" to sync. Bit RXACT in RCR is set to "1" when the serial data or the selected carrier is incoming, and the sampled data will then be kept in Receiver FIFO. Write "1" to bit RXACT to stop the Receiver operation; "0" to bit RXEN to disable the Receiver.

9.9.6 Register Description and Address

Table 9-25. List of CIR Registers

Register Name	R/W	Address	Default
CIR Data Register (DR)	R/W	Base + 0h	FFh
CIR Interrupt Enable Register (IER)	R/W	Base + 1h	00h
CIR Receiver Control Register (RCR)	R/W	Base + 2h	01h
CIR Transmitter Control Register 1 (TCR1)	R/W	Base + 3h	00h
CIR Transmitter Control Register 2 (TCR2)	R/W	Base + 4h	5Ch
CIR Transmitter Status Register (TSR)	R	Base + 5h	00h
CIR Receiver Status Register (RSR)	R	Base + 6h	00h
CIR Baud Rate Divisor Low Byte Register (BDLR)	R/W	Base + 5h	00h
CIR Baud Rate Divisor High Byte Register (BDHR)	R/W	Base + 6h	00h
CIR Interrupt Identification Register (IIR)	R	Base + 7h	01h

9.9.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through this register.

Address: Base Address + 0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**CIR Data Register (DR[7:0])** Writing data to this register causes data to be written to Transmitter FIFO. Reading data from this register causes data to be received from Receiver FIFO.

9.9.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is used to enable the CIR interrupt request.

Address: Base Address + 1h

Bit	R/W	Default	Description
7	R/W	0b	**Transmitter Data Output Select (TX_sel)** This bit is used to select transmitter data output. 0: CIRTX1 (Default) 1: CIRTX2
6	R/W	0b	**Receiver Data Input Select (RX_sel)** This bit is used to select receiver data input. 0: CIRRX1 (Default) 1: CIRRX2
5	R/W	0b	**Reset (Reset)** This bit is for software reset. Writing “1” to this bit resets register DR, IER, TCR1, BDLR, BDHR and IIR. This bit is then cleared to the initial value automatically.
4	R/W	0b	**Baud Rate Register Enable Function Enable (BR)** This bit is used to control whether the baud rate register can enable read/write function. Set this bit to “1” to enable the baud rate registers for CIR. Set this bit to “0” to disable the baud rate registers for CIR.
3	R/W	0b	**Interrupt Enable Function Control (IEC)** This bit is used to control whether the interrupt function can be enabled. Set this bit to “1” to enable the interrupt request for CIR. Set this bit to “0” to disable the interrupt request for CIR.
2	R/W	0b	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to “1” to enable Receiver FIFO Overrun Interrupt request. Set this bit to “0” to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0b	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in FIFO exceed the FIFO threshold level. Set this bit to “1” to enable Receiver Data Available Interrupt request. Set this bit to “0” to disable Receiver Data Available Interrupt request.

Bit	R/W	Default	Description
0	R/W	0b	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in FIFO are less than the FIFO threshold Level. Set this bit to “1” to enable Transmitter Low Data Level Interrupt request. Set this bit to “0” to disable Transmitter Low Data Level Interrupt request.

9.9.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is used to control the CIR Receiver.

Address: Base Address + 2h (Powered by VBAT)

Bit	R/W	Default	Description
7	R/W	0b	**Receiver Data without Sync. (RDWOS)** This bit is used to control the sync. logic for receiving data. Set this bit to “1” to obtain the receiving data without sync. logic. Set this bit to “0” to obtain the receiving data in sync. logic.
6	R/W	0b	**High-Speed Carrier Frequency Select (HCFS)** This bit is used to select whether the carrier frequency is the high-speed or low-speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
5	R/W	0b	**Receiver Enable (RXEN)** This bit is used to enable the Receiver function. Receiver Enable and RXACT will be activated if the selected carrier frequency is received. Set this bit to ”1” to enable the Receiver function. Set this bit to “0” to disable the Receiver function.
4	R/W	0b	**Receiver Demodulation Enable (RXEND)** This bit is used to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to “1”. Set this bit to “1” to enable Receiver Demodulation logic. Set this bit to “0” to disable Receiver Demodulation logic.
3	R/W	0b	**Receiver Active (RXACT)** This bit is used to control the Receiver operation. It is set to “0” when the Receiver is inactive. This bit will be set to “1” when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with the correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a “1” to this bit to clear the Receiver Active condition and make it enter the inactive mode.
2-0	R/W	001b	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are used to set the tolerance of the Receiver. For the detailed demodulation carrier frequency, please refer to Table 9-27. Receiver Demodulation Low Frequency (HCFS = 0) and Table 9-28. Receiver Demodulation High Frequency (HCFS = 1) on page 158 and 159.

9.9.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base Address + 3h

Bit	R/W	Default	Description
7	R/W	0b	**FIFO Clear (FIFOCLR)** Writing a "1" to this bit clears FIFO. This bit is then cleared to "0" automatically.
6	R/W	0b	**Internal Loopback Enable (ILE)** This bit is used to execute internal loopback for test and must be "0" in normal operation. Set this bit to "0" to disable the Internal Loopback mode. Set this bit to "1" to enable the Internal Loopback mode.
5-4	R/W	0b	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO threshold level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in the internal loopback mode (ILE = 1). **16-Byte Mode** / **32-Byte Mode** 00 — 1 — 1 (Default) 01 — 3 — 7 10 — 7 — 17 11 — 13 — 25
3	R/W	0b	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bit 6-0. Set this bit to "1" to enable the Transmitter Run Length mode. Set this bit to "0" to disable the Transmitter Run Length mode.
2	R/W	0b	**Transmitter Deferral (TXENDF)** This bit is used to avoid Transmitter underrun condition. When it is set to "1", the Transmitter FIFO data will be kept until the transmitter time-out condition occurs, or FIFO reaches full.
1-0	R/W	0b	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are used to define the Transmitter modulation pulse mode. **TXMPM[1:0] — Modulation Pulse Mode** C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit time. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6_pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved.

9.9.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is used to determine the carrier frequency.

Address: Base Address + 4h (Powered by VBAT)

Bit	R/W	Default	Description
7-3	R/W	01011b	**Carrier Frequency (CFQ[4:0])** These five bits are used to determine the modulation carrier frequency. Please refer to the following table.
2-0	R/W	100b	**Transmitter Modulation Pulse Width (TXMPW[2:0])** These three bits are used to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the settings of the carrier frequency and the selection of Transmitter Modulation pulse width.

TXMPW[2:0]	HCFS = 0	HCFS = 1
000	Reserved	Reserved
001	Reserved	Reserved
010	6 μs	0.7 μs
011	7 μs	0.8 μs
100	**8.7 μs**	**0.9 μs (Default)**
101	10.6 μs	1.0 μs
110	13.3 μs	1.16 μs
111	Reserved	Reserved

Table 9-26. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (default)**	**480 kHz (default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-27. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-28. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.9.6.6 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BDLR[7:0])** These bits are the low byte of the register, which is to divide the Baud Rate clock.

9.9.6.7 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BDHR[7:0])** These bits are the high byte of the register, which is to divide the Baud Rate clock.

Baud rate divisor = 115200 / baud rate
Ex1: 2400 bps → 115200 /2400 = 48 → 48(d) = 0030(h) → BDHR = 00h, BDLR = 30h
Ex2: bit width = 0.565 ms (1770 bps (115200 / 1770 = 65(d) = 0041(h) (BDHR = 00(h), BDLR = 41(h)

9.9.6.8 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit read only register, provides the Transmitter FIFO status.

Address: Base Address + 5h

Bit	R/W	Default	Description
7-6	R	-	**Reserved**
5-0	R	000000b	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in the Transmitter FIFO.

9.9.6.9 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base Address + 6h

Bit	R/W	Default	Description
7	R	0b	**Receiver FIFO Time-out (RXFTO)** This bit will be set to "1" when a Receiver FIFO time-out condition occurs. Following is the condition required for the occurrence of Receiver FIFO time-out: When at least one byte of data is queued in the Receiver FIFO for more than 64 ms and the receiver has been inactive (RXACT=0) for more than 64 ms.
6	-	-	**Reserved**
5-0	R	000000b	**Receiver FIFO Byte Count (RXFBC)** Return the number of bytes left in Receiver FIFO.

9.9.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit register, is used to identify the pending interrupts.

Address: Base address + 7h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-1	R	00b	**Interrupt Identification** These two bits are used to identify the source of the pending interrupt. **IIR[1:0] Interrupt Source** 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	**Interrupt Pending** This bit will be set to "1" while an interrupt is pending.

9.10 Parallel Port

The IT8783E/F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). For enabling/ disabling, changing the base address of the parallel port, and operation mode selection, please refer to configuration registers for the detail.

Table 9-29. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	11	STB#	WRITE#	NStrobe
2-9	12- 19	PD0 - 7	PD0 - 7	PD0-7
10	6	ACK#	INTR	nAck
11	5	BUSY	WAIT#	Busy PeriphAck(2)
12	4	PE	(NU) (1)	PError nAckReverse(2)
13	3	SLCT	(NU) (1)	Select
14	10	AFD#	DSTB#	nAutoFd HostAck(2)
15	9	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	8	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	7	SLIN#	ASTB#	nSelectIn

Note 1: NU: Not used.
Note 2: Fast mode.
Note 3: For more information, please refer to the IEEE 1284 standard.

9.10.1 SPP and EPP Modes

Table 9-30. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

9.10.1.1 Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register, which forwards the direction when the bit is low and reverses the direction when the bit is high.

9.10.1.2 Status Port (Base Address 1 + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7 - BUSY#: Inverse of printer BUSY signal; a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge; a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end; a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected; a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal; a logic "0" means an error has been detected.
Bits 2, 1 - Reserved: These bits are always "1" at read.
Bit 0 - TMOUT: This bit is valid only in the EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurs and a logic “1” means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic “1” to it. When the IT8783E/F is selected as the non-EPP mode (SPP or ECP), this bit is always a logic "1" at read.

9.10.1.3 Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.
Bit 6, 7- Reserved: These two bits are always "1" at read.
Bit 5 - PDDIR: Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus, and "1" to input from PD bus.
Bit 4 - IRQE: Interrupt request enable. Setting this bit "1" enables the interrupt request from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3 - SLIN: Inverse of SLIN# pin; setting this bit to "1" selects the printer.
Bit 2 - INIT: Initiate printer; setting this bit to "0" initializes the printer.
Bit 1 - AFD: Inverse of the AFD# pin; setting this bit to "1" causes the printer to automatically advance one line after each line is printed.
Bit 0 - STB: Inverse of the STB# pin; this pin controls the data strobe signal to the printer.

9.10.1.4 EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes data to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP ADDRESS WRITE cycle. When the Host reads data from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP ADDRESS READ cycle.

9.10.1.5 EPP Data Ports 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes data to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is at this address) causes an EPP DATA WRITE cycle. When the Host reads data from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is at this address) causes an EPP DATA READ cycle.

9.10.2 EPP Mode Operation

When the parallel port of the IT8783E/F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active,

the IT8783E/F will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted. If a time-out occurs, the current EPP READ/WRITE cycle will be aborted and a logic "1" will be read in the bit 0 of the status port register. The Host must write 0 to bit 0, 1, 3 of the control port register before any EPP READ/WRITE cycle (EPP spec.). Pin STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

9.10.2.1 EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.10.2.2 EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the Host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.10.2.3 EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

9.10.2.4 EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.10.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or the ECP mode in both forward and reverse directions. A 16-byte FIFO is

implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8783E/F does not support hardware RLE compression. For the detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-31. Bit Map of ECP Register

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

9.10.3.1 ECP Register Definitions

Table 9-32. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	R	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

Note 2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

9.10.3.2 ECP Mode Description

Table 9-33. ECP Mode Description

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: For the mode selection, please refer to the ECP Register Description for the detail.

9.10.3.3 ECP Pin Description

Table 9-34. ECP Pin Description

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device.
PD0-PD7	I/O	Address or data or RLE data.
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
Perror (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
Select	I	Printer On-Line Indication.
nAutoFd (HostAck)	O	In the reverse direction, this signal is used for handshaking between the nAck and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0 - PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while entering the ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low, and nSelectIn is high.
NSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

9.10.3.4 Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a WRITE operation, the contents of the LPC data fields are latched by the Data Register. The contents are then sent without being inverted to PD0-PD7. In an READ operation, the contents of data ports are read and sent to the host.

9.10.3.5 ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data byte written to this port is placed in FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends these data to the peripheral. Operation of this port is only valid in the forward direction (dcr(5)=0).

9.10.3.6 Device Status Register (dsr) (Base 1 +01h, Mode All)

Bit 0, 1 and 2 of this register are not implemented. The states of these bits remain high in a READ operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

9.10.3.7 Device Control Register (dcr) (Base 1+02h, Mode All)

Bit 6 and 7 of this register have no function. They are set high during the READ operation, and cannot be written any data. Contents in bit 0-5 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.
dcr(5): Except in mode 000 and 010, setting this bit low means that the PD bus is in output operation whereas setting it high means that it is in input operation. This bit will be forced to low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.
dcr(3): It is inverted and output to SelectIn.
dcr(2): It is output to nInit without inversion.
dcr(1): It is inverted and output to nAutoFd.
dcr(0): It is inverted and output to nStrobe.

9.10.3.8 Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

9.10.3.9 ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can receive these bytes by performing READ operation or DMA transfer from this FIFO.

9.10.3.10 Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfer to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a READ from an empty tFifo causes the last data byte to return.

9.10.3.11 Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

9.10.3.12 Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

cnfgB(7): A logic "0" read indicates that the chip does not support hardware RLE compression.
cnfgB(6): Reserved.
cnfgB(5)-cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)-cnfg(0): A value 000 read indicates that the DMA channel is set to 8-bit DMA.

9.10.3.13 Extended Control Register (ecr) (Base 2+02h, Mode All)

This is an ECP function control register.
ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-35. Mode and Description of Extended Control Register (ECR)

ECR	Mode and Description
000	**Standard Parallel Port Mode(SPPM)** The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	**PS/2 Parallel Port Mode(PPPM)** It is similar to the SPP mode, except that the dcr(5) is **read/write**. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	**Parallel Port Data FIFO Mode(PPDFM)** This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	**ECP Parallel Port Mode(EPPM)** In the forward direction, bytes in the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	**Reserved; undefined**
110	**Test Mode(TM)** In this mode, FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	**Configuration Mode(CM)** In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode
1: Disable the interrupt generated on the asserting edge of the nFault input.
0: Enable the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE
1: Enable DMA. DMA is started when serviceIntr (ecr(2)) is 0.
0: Disables DMA unconditionally.

ecr(2): ServiceIntr, READ/WRITE
1: Disable DMA and all service interrupts.
0: Enable the service interrupts. This bit will be set to "1" by hardware when one of the three service

interrupts occurs.
Writing “1” to this bit will not generate an interrupt.

Case 1: dmaEn=1
During DMA, this bit will be set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0
This bit is set to 1 (a service interrupt generated) whenever there is writeIntrThreshold or more bytes space free in FIFO.

Case 3: dmaEn=0, dcr(5)=1
This bit is set to 1 (a service interrupt generated) whenever there is readIntrThreshold or more valid bytes to be read from FIFO.

ecr(1): full, **read only**
1: FIFO is full and cannot accept another byte.
0: FIFO has at least one free data byte space.

ecr(0): empty, **read only**
1: FIFO is empty.
0: FIFO contains at least one data byte.

9.10.3.14 Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting the mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

For mode 000 and 001, they may be immediately switched. To change the direction, the mode must be set to 001 first.

In the extended forward mode, FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In the ECP reverse mode, all data must be read from FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking when the mode is changed during a data transfer. In such a condition, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

9.10.3.15 Software Operation (ECP)

Before the ECP operation can be started, it is necessary for the host to switch the mode to 000 first in order to negotiate with the parallel port. During this process, the Host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfer is PWord-wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change the direction, the host has to switch the mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches the mode to 001. If the direction is set to 1, the hardware performs the handshaking for each ECP data byte read, and then tries to fill FIFO. At this time, PWords may be read from the ecpDFifo while retaining data. It is also possible to perform the ECP transfer by handshaking with individual bytes under programmed control in mode 001 or 000 even though this is a comparatively time-consuming approach.

9.10.3.16 Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets the direction and state. Next, the desired count and memory addresses are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents of FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing transfer, the host DMA controller is disabled, serviceIntr is then set to 1, and dmaEn is next set to 0. If the contents in FIFO are empty or full, DMA will start again. This is first done by enabling the host DMA controller, and then setting dmaEn to 1. Finally, serviceIntr is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

9.10.3.17 Interrupt

It is necessary to generate an interrupt when any of the following states is reached.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.
2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.
3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.
4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
5. ackIntEn = 1. In current implementation of using existing parallel ports, the generated interrupt may be either edge or level trigger type.

9.10.3.18 Interrupt-driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

For any PC LPC bus implementation adjusted to expedite DMA or I/O transfer, it is necessary to ensure that the bandwidth on ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

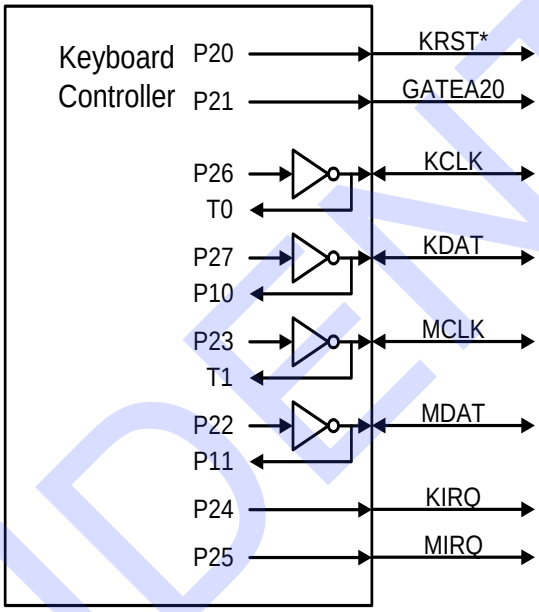
(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

9.11 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter the power-down mode by executing two types of power-down instructions.

Figure 9-7. Keyboard and Mouse Interface



9.11.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The following table shows how the interface decodes the control signals.

Table 9-36. Data Register READ/WRITE Controls

Host Address [Note]	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (Set F1)

Note:
These are the default values of LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.
WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared

and the IBF bit is set.
READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.
WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

9.11.2 Data Registers and Status Register

The keyboard controller provides two data registers: one is DBIN for data input, and the other is DBOUT for data output. Both are 8-bit wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of the DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 9-37. Status Register on page 171. The bit 0 OBF is set to “1” when the microcontroller writes data into DBOUT, and is cleared when the system initiates a DATA READ operation. The bit 1 IBF is set to “1” when the system initiates a WRITE operation, and is cleared when the microcontroller executes an “IN A, DBB” instruction. The F0 and F1 flags can be set or reset when the microcontroller executes clear and complement flag instructions. F1 also holds the system WRITE information when the system performs the WRITE operation.

Table 9-37. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.11.3 Keyboard and Mouse Interface

KCLK is the keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin; its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin; its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software controlled or user defined outputs. External pull-ups may be required for these pins.

9.11.4 KIRQ and MIRQ

KIRQ is the interrupt request for the keyboard (Default IRQ1), and MIRQ is the interrupt request for the mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

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10. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage .....-0.5V to 5.5V

Input Voltage (Vi)..... -0.5V to VCC+0.5V

Output Voltage (Vo)..... -0.5V to VCC + 0.3V

Operation Temperature (Topt) ..... -40°C to +100°C

Storage Temperature ..... -55°C to +100°C

Power Dissipation 300mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = -40°C to + 100°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DO8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
DOD8 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
DO16 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
DO24 Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
DO24L Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
DIO8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -8 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = -40°C to + 100°C)[cont'd]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 8 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIO16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 16 mA			0.4	V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DIO24 Type Buffer						
V_{OL}	Low Output Voltage	I_{OL} = 24 mA			0.4	V
V_{OH}	High Output Voltage	I_{OH} = -16 mA	2.4			V
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA
I_{OZ}	3-state Leakage				20	µA
DI Type Buffer						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.2			V
I_{IL}	Low Input Leakage	V_{IN} = 0		10		µA
I_{IH}	High Input Leakage	V_{IN} = VCC			-10	µA

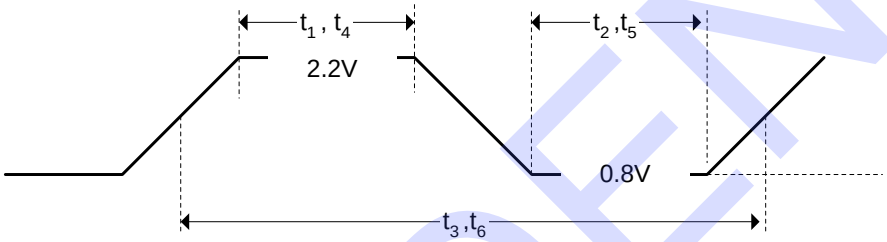
11. AC Characteristics (VCC = 5V ± 5%, Ta = -40°C to + 100°C)

11.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz [1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz [1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz [1]	40	42	44	nsec

Not tested. Guaranteed by design.

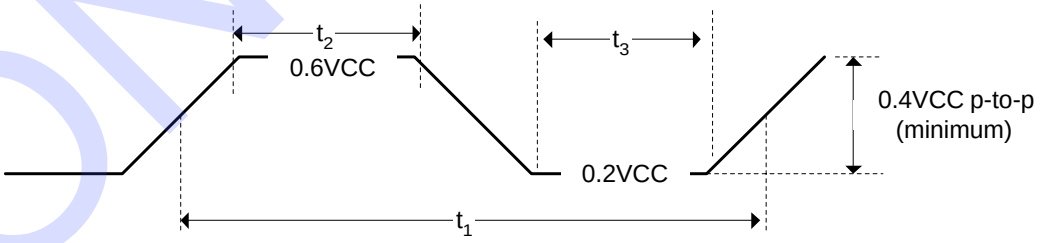
Figure 11-1. Clock Input Timings



11.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			μsec

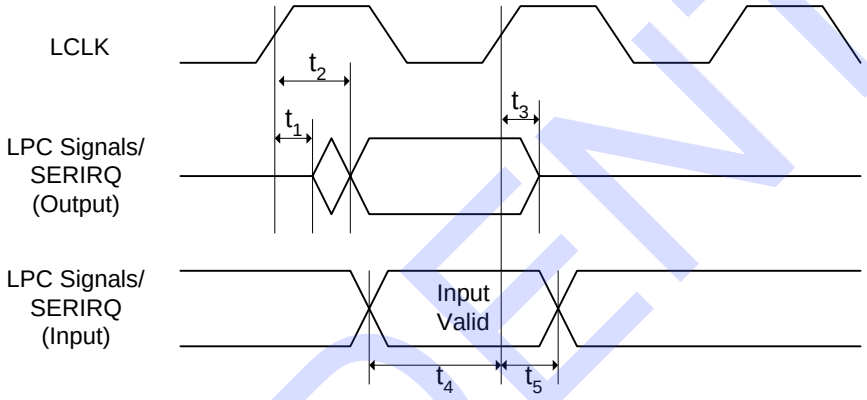
Figure 11-2. LCLK (PCICLK) and LRESET Timings



11.3 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

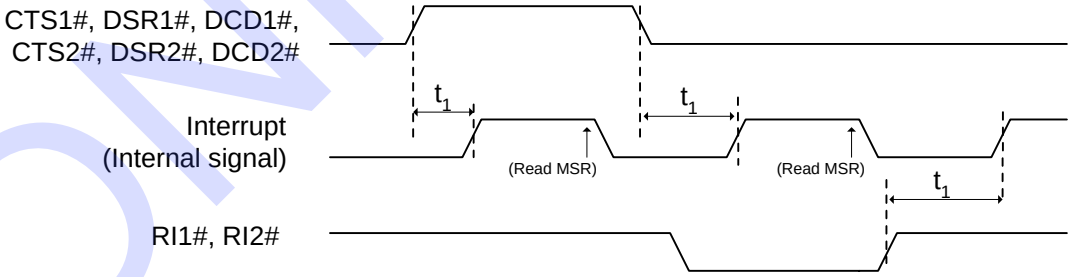
Figure 11-3. LPC and SERIRQ Timings



11.4 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

Figure 11-4. Modem Control Timings



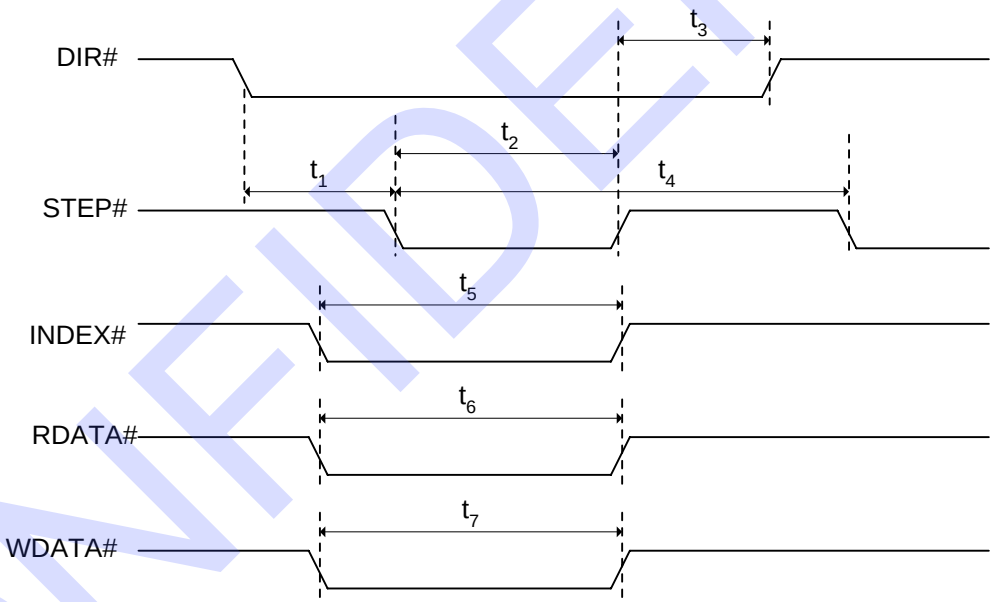
11.5 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} Note1		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} Note2		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. t_{mclk} =8M/ 4M/ 2.4M/ 2M for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.

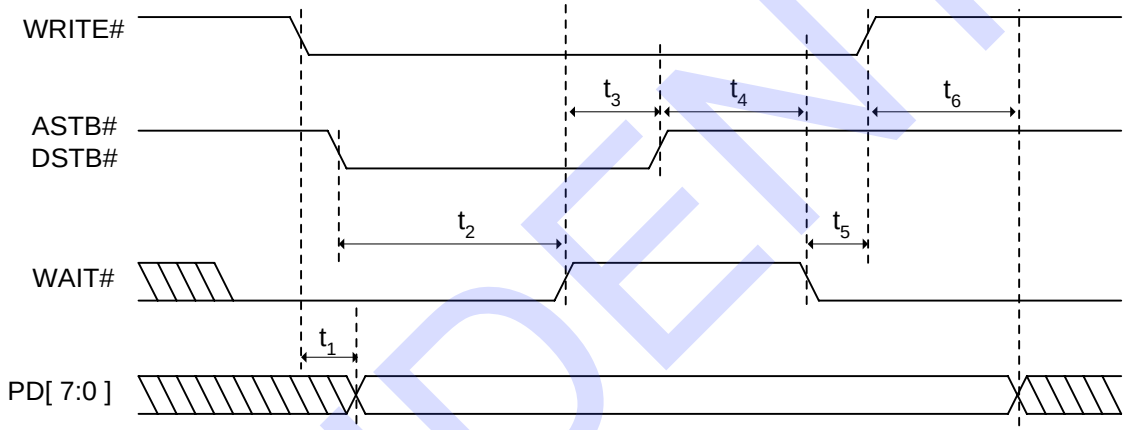
Figure 11-5. Floppy Disk Drive Timings



11.6 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	µsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec

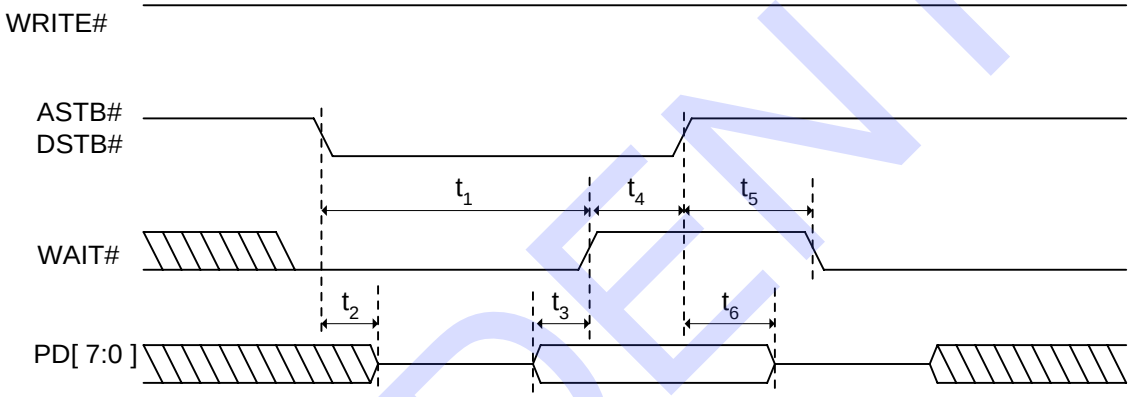
Figure 11-6. EPP Address or Data Write Cycle Timings



11.7 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	µsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

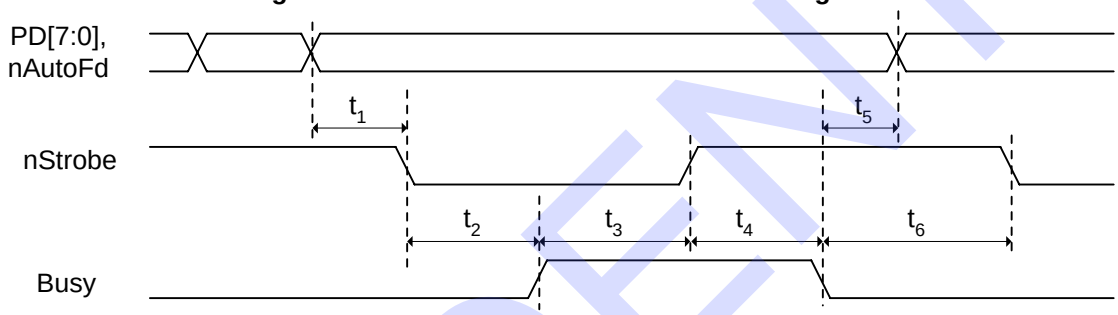
Figure 11-7. EPP Address or Data Read Cycle Timings



11.8 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

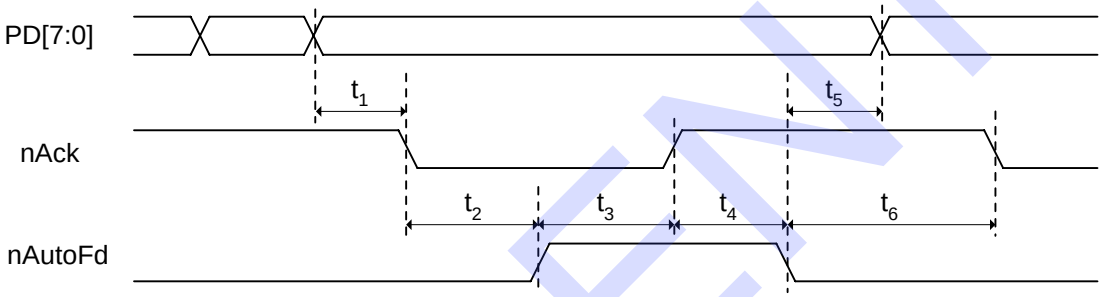
Figure 11-8. ECP Parallel Port Forward Timings



11.9 ECP Parallel Port Backward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

Figure 11-9. ECP Parallel Port Backward Timings



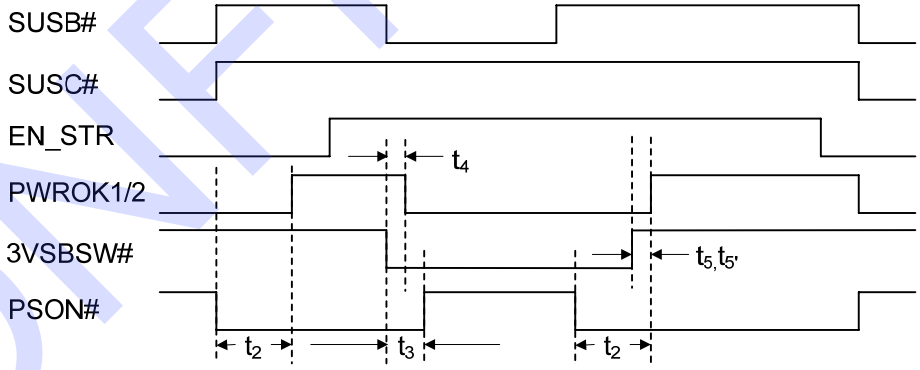
11.10 RSMRST#, PWROK1/2, and ACPI Power Control Signal Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	RSMRST# de-actives delay from VCCH5V=4V	13	16	19	msec
t_2	PWROK1/2 active delay from VCC5V=4V	350	400	450	msec
t_3	Overlap of PSON# and 3VSBSW#	8.5	10	11.5	msec
t_4	3VSBAW# rising to PWROK1/2 delay time (2A bit 0 =0)		1		usec
t_4	3VSBAW# rising to PWROK1/2 delay time (2A bit 0 =1)	120	140	160	msec
t_5	3VSBAW# falling to PWROK1/2 delay time		1	2	msec

Figure 11-11. RSMRST# Timings

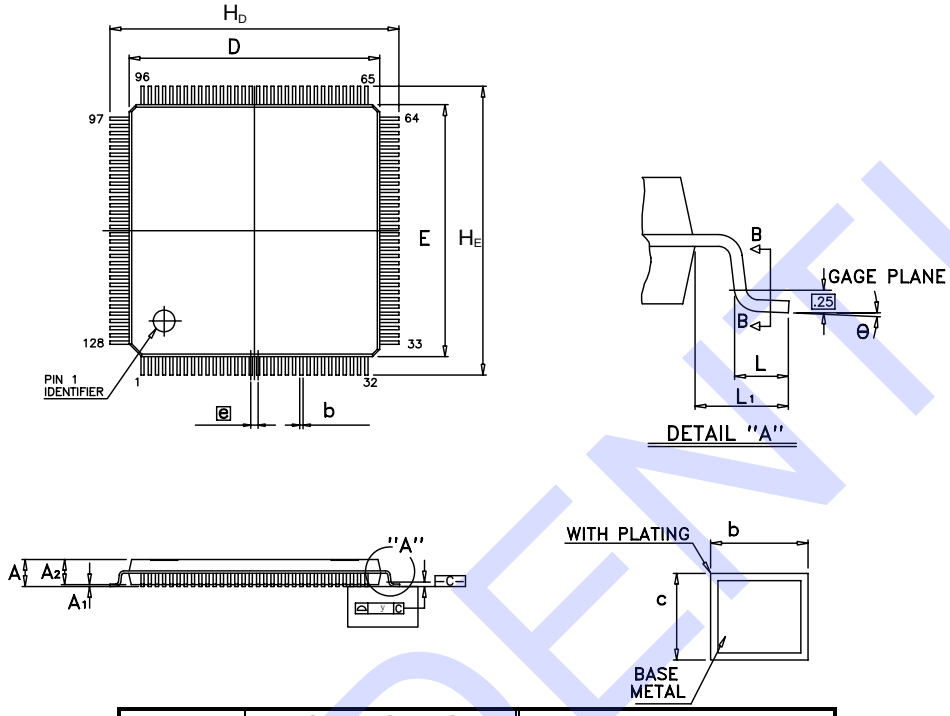
Figure 11-12. PWROK1/2 Timings

Figure 11-13. ACPI Power Signal Timings



12. Package Information

LQFP 128L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A_1	0.002	-	-	0.05	-	-
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1.Dimensions D and E do not include mold protrusion.

2.Dimensions b does not include dambar protrusion.
Total in excess of the b dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.

3.Controlling dimension : Millimeter

4.Reference document : JEDEC MS-026

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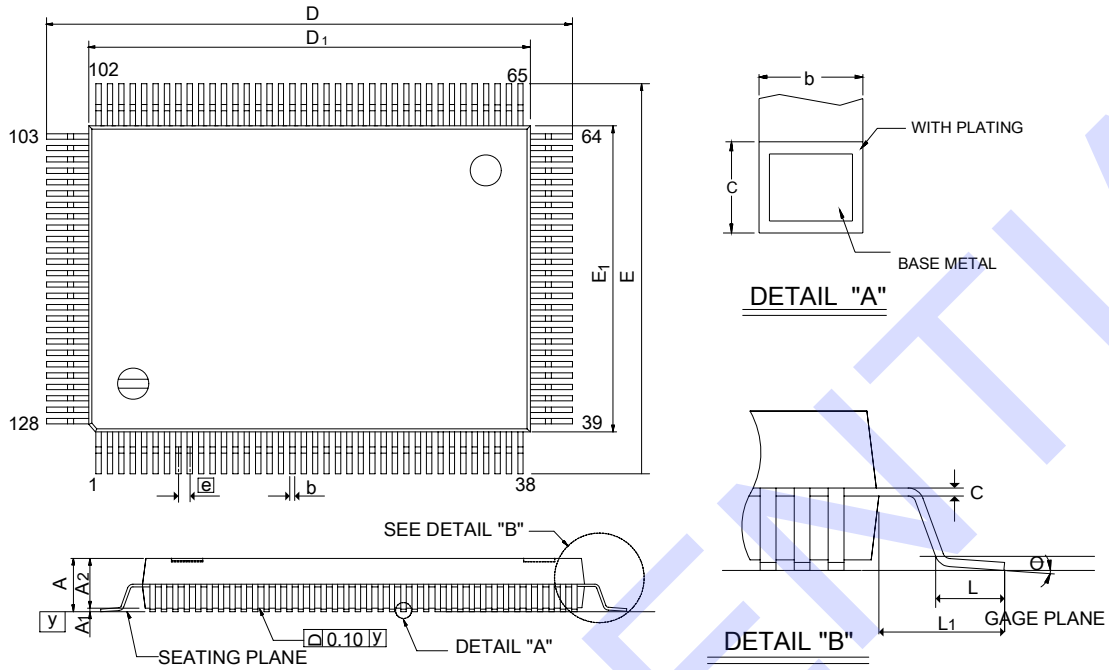
QFP 128L Outline Dimensions **unit: inches/mm**



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.25	-	-
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter

DI-QFP128(14*20)v2

13. Ordering Information

Part No.	Package
IT8783E	LQFP 128L
IT8783F	QFP 128L

ITE also provides RoHS compliant component. Please mark "-L" at the end of the Part No. when the parts ordered are RoHS compliant."

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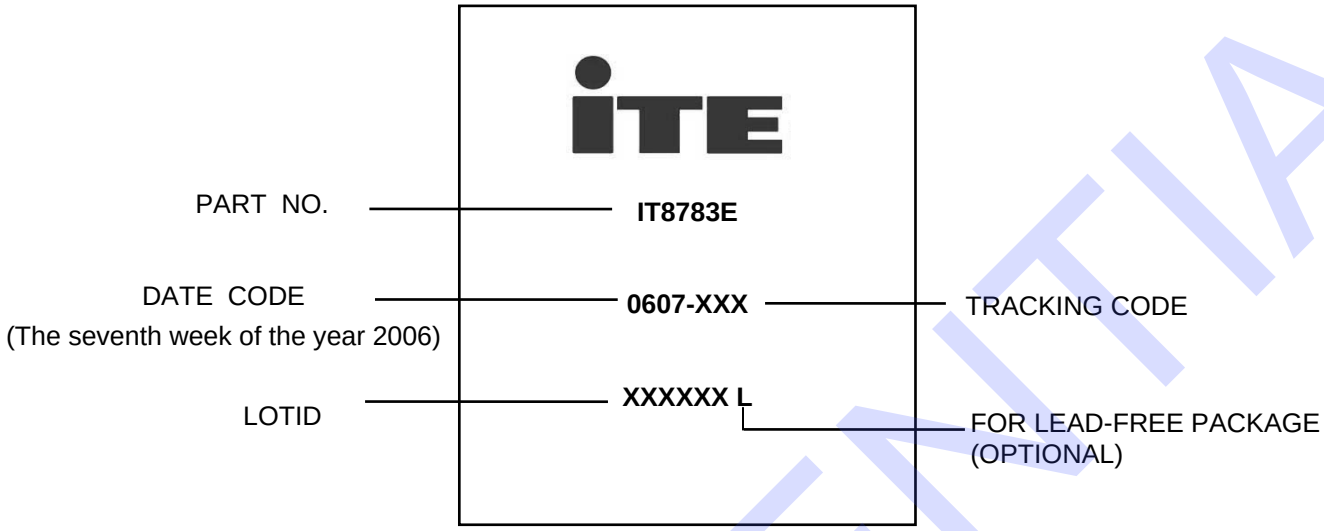
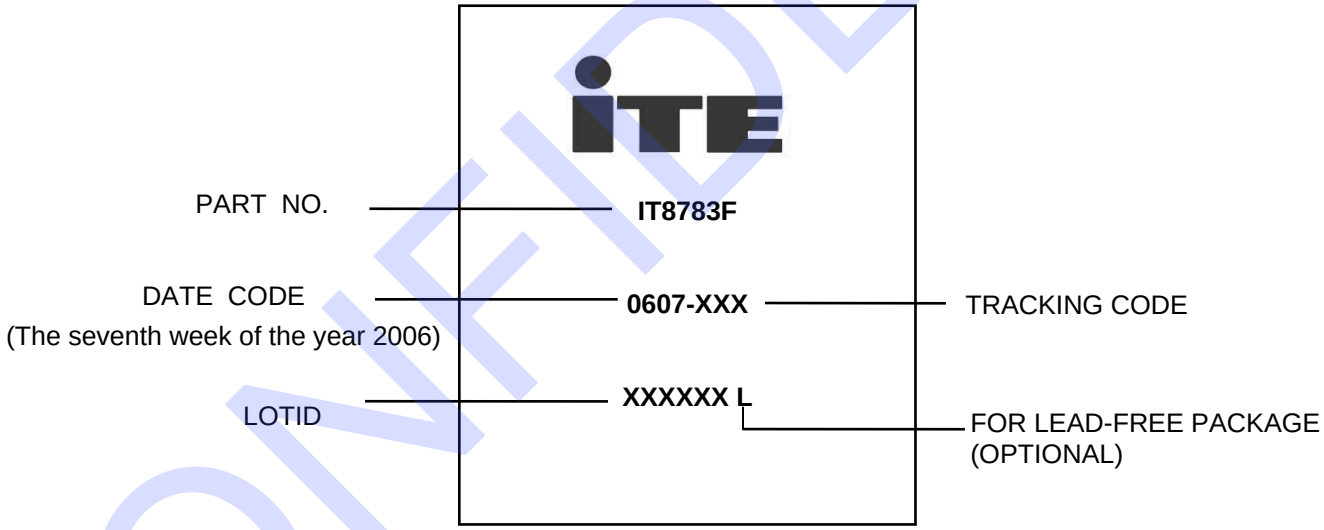
14. Top Marking Information





ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China. Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subjected to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings), misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implantation to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in writing and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided here under and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods here under. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.