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IT8892E/IT8893E

PCI Express to PCI Bridge

Preliminary Specification V0.7

(For F Version)

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
-	Feature update • PCI Express → Maximum payload size up to 256 bytes • PCI → Suport of up to six queues for memory read cycles → Suported number of outstanding memory read cycles changed from eight to 24	-
-	Default of the following registers updated: • Revision ID Register (REVID) • Class Code Register (CC) • Secondary Discard Timer (SDT) • Data Credit (DC) • Header Credit (HC) • Initial Non-Posted Flow Control Credit (INPFCC) • Data Credit (DC) • Header Credit (HC) • Memory Read Lock Enable (MRLE) • PCI Output PAD Skew Control • PCI Input PAD Skew Control • Max_Read_Request Size (MRRS)	-
-	Note below added to PCI Express related registers: These bits will be hidden with legacy mode.	-
-	Registers below added: • Transaction Layer Control Register1 / Transaction Layer Control Register2 • Dummy Register (0000FFFFh)	-
6.2.28	Capabilities Pointer Register (CAPP) • Default and description updated	33
6.2.36	Transaction Layer Control Register (TLCR) • Description of bit 31-15 updated	37
6.2.39	PCI Control Register (PCICR) • Function of bit 12 changed into "PCI Clock Slew Control"	39

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FIGURES

TABLES

1. Features

- **PCI Express**
  - Compliant with PCI Express Base Specification Revision 1.1
  - Compliant with PCI Express to PCI/PCI-X Bridge Specification Revision 1.0
  - Full 2.5GHz per direction
  - Data Link Layer Cyclic Redundancy Check (CRC) generator and checker
  - Automatic Retry of bad packets
  - Legacy interrupt signaling
  - Maximum payload size up to 256 bytes

- **PCI**
  - Compliant with PCI Local Bus Specification Revision 3.0
  - Supports PCI 32-bit, 33/66 MHz, 3.3V, 5V tolerant
  - Supports 4(IT8892E) / 2(IT8893E) external REQ/GNT pairs for internal arbiter
  - Supports up to six queues for memory read cycles
  - Supports up to 24 outstanding memory read cycles

- **Power Management**
  - Supports PCI Express Active State Power Management (ASPM) L0s, L1
  - Supports link power management state L0s, L1, L23 Ready, L2, L3 link state
  - Supports for PM 1.1 compatible D0, D1, D2, D3hot and D3cold device power states
  - Supports PME# event propagation
  - Supports side-band WAKE# signaling

- **SPI Interface**
  - SPI master only
  - Operating at up to 25MHz
  - Supports up to 16MB EEPROM utilizing 1, 2, or 3 byte addressing

- **I/O Port 80**
  - Supports I/O port 80 debugging on PCI side
  - Dual 7-segment display

- **Legacy Mode**
  - Supports PCI-to-PCI bridge with subtractive decode for legacy devices

- **Built-in Regulator**
  - Two on-chip 3.3V to 1.8V regulators
  - Supports power-on-reset

- **General Purpose I/O**
  - Supports 5 GPIOs

- **Package**
  - LQFP 128

- **RoHS Compliant (100% Green Available)**

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2. General Description

IT8892E/IT8893E is a single-function PCI Express to PCI bridge, which is compliant with the PCI Express Base Specification Revision 1.1, PCI Local Bus Specification Revision 3.0 and PCI Express to PCI/PCI-X Bridge Specification Revision 1.0. The PCI Express interface supports a x1 lane configuration, and enables the bridge to provide high-performance operation of the data transfer rate up to 250MB/s. The PCI bus interface supports 32-bit and can operate at up to 66 MHz.

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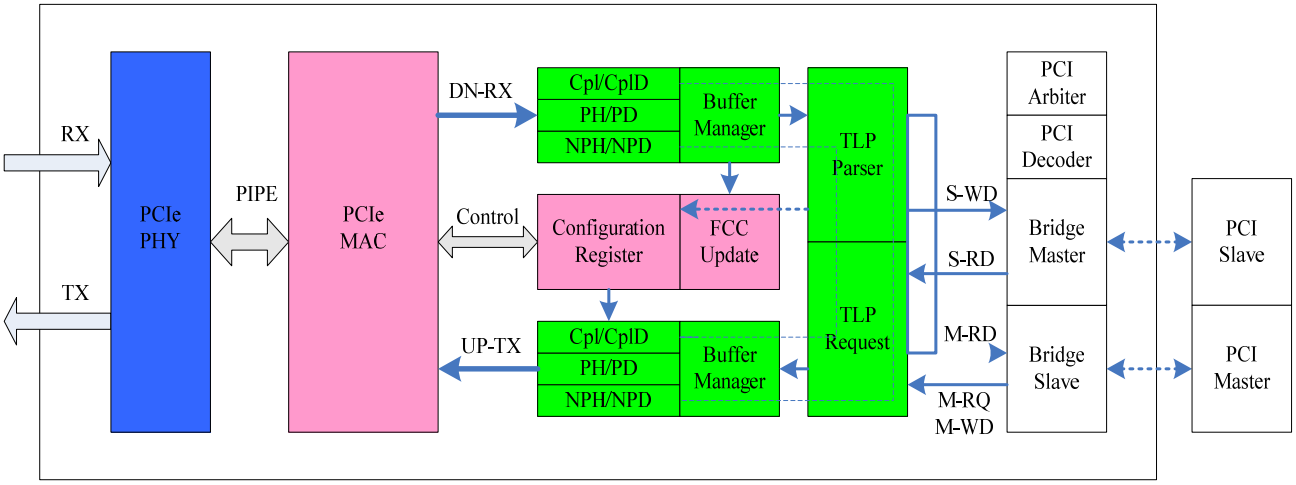
3. Block Diagram



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4. Pin Configuration

4.1 IT8892E Pin Configuration

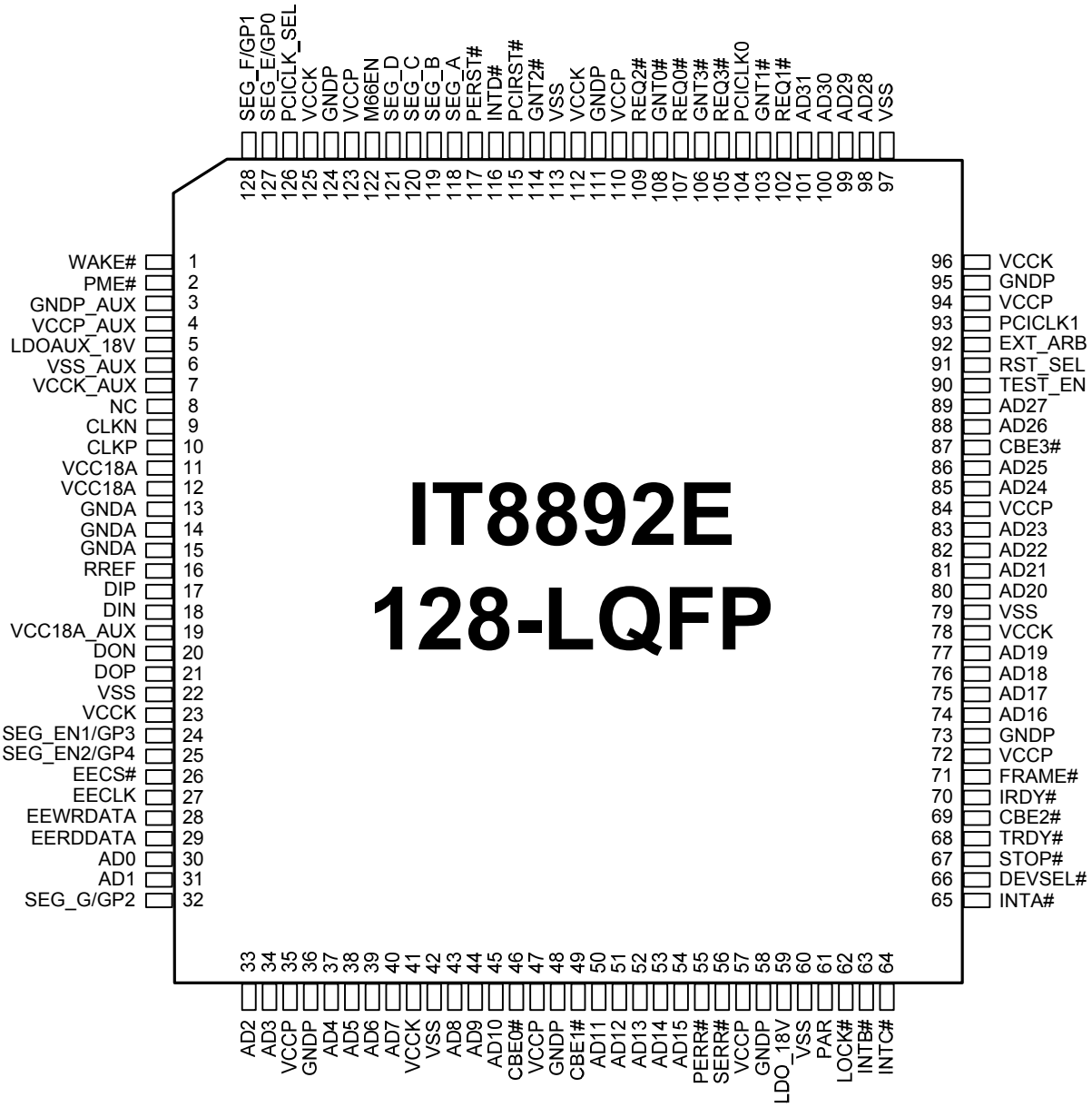

Table 4-1. IT8892E Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	WAKE#	33	AD2	65	INTA#	97	VSS
2	PME#	34	AD3	66	DEVSEL#	98	AD28
3	GNDP_AUX	35	VCCP	67	STOP#	99	AD29
4	VCCP_AUX	36	GNDP	68	TRDY#	100	AD30
5	LDOAUX_18V	37	AD4	69	CBE2#	101	AD31
6	VSS_AUX	38	AD5	70	IRDY#	102	REQ1#
7	VCCK_AUX	39	AD6	71	FRAME#	103	GNT1#
8	NC	40	AD7	72	VCCP	104	PCICLK0
9	CLKN	41	VCCK	73	GNDP	105	REQ3#
10	CLKP	42	VSS	74	AD16	106	GNT#
11	VCC18A	43	AD8	75	AD17	107	REQ0#
12	VCC18A	44	AD9	76	AD18	108	GNT0#
13	GNDA	45	AD10	77	AD19	109	REQ2#
14	GNDA	46	CBE0#	78	VCCK	110	VCCP
15	GNDA	47	VCCP	79	VSS	111	GNDP
16	RREF	48	GNDP	80	AD20	112	VCCK
17	DIP	49	CBE1#	81	AD21	113	VSS
18	DIN	50	AD11	82	AD22	114	GNT2#
19	VCC18A_AUX	51	AD12	83	AD23	115	PCIRST#
20	DON	52	AD13	84	VCCP	116	INTD#
21	DOP	53	AD14	85	AD24	117	PERST#
22	VSS	54	AD15	86	AD25	118	SEG_A
23	VCCK	55	PERR#	87	CBE3#	119	SEG_B
24	SEG_EN1/GP3	56	SERR#	88	AD26	120	SEG_C
25	SEG_EN2/GP4	57	VCCP	89	AD27	121	SEG_D
26	EECS#	58	GNDP	90	TEST_EN	122	M66EN
27	EECLK	59	LDO_18V	91	RST_SEL	123	VCCP
28	EEWRDATA	60	VSS	92	EXT_ARB	124	GNDP
29	EERDDATA	61	PAR	93	PCICLK1	125	VCCK
30	AD0	62	LOCK#	94	VCCP	126	PCICLK_SEL
31	AD1	63	INTB#	95	GNDP	127	SEG_E/GP0
32	SEG_G/GP2	64	INTC#	96	VCCK	128	SEG_F/GP1

Table 4-2. IT8892E Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD0	30	CBE0#	46	INTA#	65	SEG_G/GP2	32
AD1	31	CBE1#	49	INTB#	63	SERR#	56
AD10	45	CBE2#	69	INTC#	64	STOP#	67
AD11	50	CBE3#	87	INTD#	116	TEST_EN	90
AD12	51	CLKN	9	IRDY#	70	TRDY#	68
AD13	52	CLKP	10	LDO_18V	59	VCC18A	11
AD14	53	DEVSEL#	66	LDOAUX_18V	5	VCC18A	12
AD15	54	DIN	18	LOCK#	62	VCC18A_AUX	19
AD16	74	DIP	17	M66EN	122	VCCK	23
AD17	75	DON	20	NC	8	VCCK	41
AD18	76	DOP	21	PAR	61	VCCK	78
AD19	77	EECLK	27	PCICLK_SEL	126	VCCK	96
AD2	33	EECS#	26	PCICLK0	104	VCCK	112
AD20	80	EERDDATA	29	PCICLK1	93	VCCK	125
AD21	81	EEWRDATA	28	PCIRST#	115	VCCK_AUX	7
AD22	82	EXT_ARB	92	PERR#	55	VCCP	35
AD23	83	FRAME#	71	PERST#	117	VCCP	47
AD24	85	GNDA	13	PME#	2	VCCP	57
AD25	86	GNDA	14	REQ0#	107	VCCP	72
AD26	88	GNDA	15	REQ1#	102	VCCP	84
AD27	89	GNDP	36	REQ2#	109	VCCP	94
AD28	98	GNDP	48	REQ3#	105	VCCP	110
AD29	99	GNDP	58	RREF	16	VCCP	123
AD3	34	GNDP	73	RST_SEL	91	VCCP_AUX	4
AD30	100	GNDP	95	SEG_A	118	VSS	22
AD31	101	GNDP	111	SEG_B	119	VSS	42
AD4	37	GNDP	124	SEG_C	120	VSS	60
AD5	38	GNDP_AUX	3	SEG_D	121	VSS	79
AD6	39	GNT0#	108	SEG_E/GP0	127	VSS	97
AD7	40	GNT1#	103	SEG_EN1/GP3	24	VSS	113
AD8	43	GNT2#	114	SEG_EN2/GP4	25	VSS_AUX	6
AD9	44	GNT3#	106	SEG_F/GP1	128	WAKE#	1

4.2 IT8893E Pin Configuration

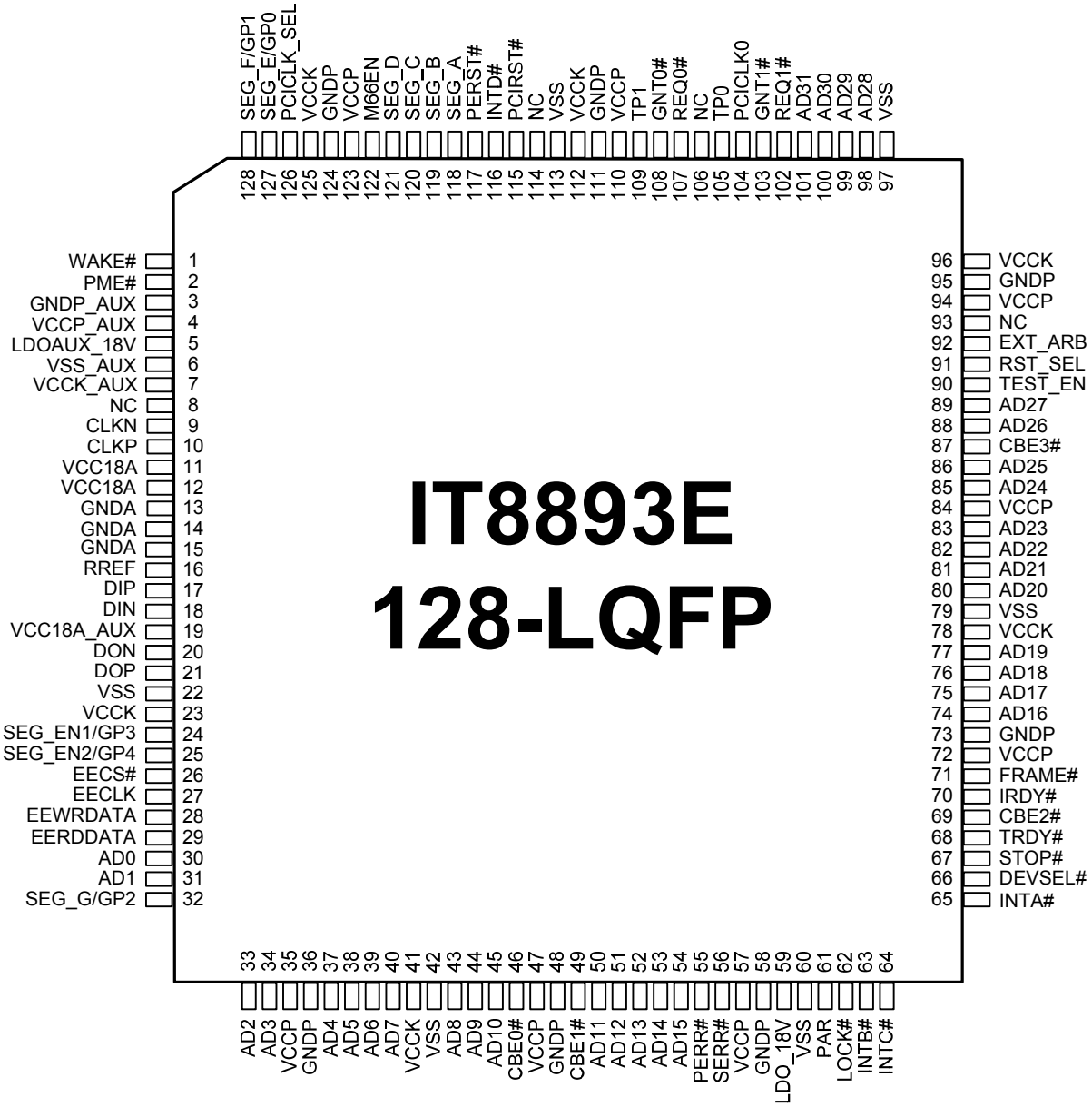

Table 4-3. IT8893E Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	WAKE#	33	AD2	65	INTA#	97	VSS
2	PME#	34	AD3	66	DEVSEL#	98	AD28
3	GNDP_AUX	35	VCCP	67	STOP#	99	AD29
4	VCCP_AUX	36	GNDP	68	TRDY#	100	AD30
5	LDOAUX_18V	37	AD4	69	CBE2#	101	AD31
6	VSS_AUX	38	AD5	70	IRDY#	102	REQ1#
7	VCCK_AUX	39	AD6	71	FRAME#	103	GNT1#
8	NC	40	AD7	72	VCCP	104	PCICLK0
9	CLKN	41	VCCK	73	GNDP	105	TP0
10	CLKP	42	VSS	74	AD16	106	NC
11	VCC18A	43	AD8	75	AD17	107	REQ0#
12	VCC18A	44	AD9	76	AD18	108	GNT0#
13	GNDA	45	AD10	77	AD19	109	TP1
14	GNDA	46	CBE0#	78	VCCK	110	VCCP
15	GNDA	47	VCCP	79	VSS	111	GNDP
16	RREF	48	GNDP	80	AD20	112	VCCK
17	DIP	49	CBE1#	81	AD21	113	VSS
18	DIN	50	AD11	82	AD22	114	NC
19	VCC18A_AUX	51	AD12	83	AD23	115	PCIRST#
20	DON	52	AD13	84	VCCP	116	INTD#
21	DOP	53	AD14	85	AD24	117	PERST#
22	VSS	54	AD15	86	AD25	118	SEG_A
23	VCCK	55	PERR#	87	CBE3#	119	SEG_B
24	SEG_EN1/GP3	56	SERR#	88	AD26	120	SEG_C
25	SEG_EN2/GP4	57	VCCP	89	AD27	121	SEG_D
26	EECS#	58	GNDP	90	TEST_EN	122	M66EN
27	EECLK	59	LDO_18V	91	RST_SEL	123	VCCP
28	EEWRDATA	60	VSS	92	EXT_ARB	124	GNDP
29	EERDDATA	61	PAR	93	NC	125	VCCK
30	AD0	62	LOCK#	94	VCCP	126	PCICLK_SEL
31	AD1	63	INTB#	95	GNDP	127	SEG_E/GP0
32	SEG_G/GP2	64	INTC#	96	VCCK	128	SEG_F/GP1

Table 4-4. IT8893E Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD0	30	CBE0#	46	INTC#	64	STOP#	67
AD1	31	CBE1#	49	INTD#	116	TEST_EN	90
AD10	45	CBE2#	69	IRDY#	70	TP0	105
AD11	50	CBE3#	87	LDO_18V	59	TP1	109
AD12	51	CLKN	9	LDOAUX_18V	5	TRDY#	68
AD13	52	CLKP	10	LOCK#	62	VCC18A	11
AD14	53	DEVSEL#	66	M66EN	122	VCC18A	12
AD15	54	DIN	18	NC	8	VCC18A_AUX	19
AD16	74	DIP	17	NC	93	VCCK	23
AD17	75	DON	20	NC	106	VCCK	41
AD18	76	DOP	21	NC	114	VCCK	78
AD19	77	EECLK	27	PAR	61	VCCK	96
AD2	33	EECS#	26	PCICLK_SEL	126	VCCK	112
AD20	80	EERDDATA	29	PCICLK0	104	VCCK	125
AD21	81	EEWRDATA	28	PCIRST#	115	VCCK_AUX	7
AD22	82	EXT_ARB	92	PERR#	55	VCCP	35
AD23	83	FRAME#	71	PERST#	117	VCCP	47
AD24	85	GNDA	13	PME#	2	VCCP	57
AD25	86	GNDA	14	REQ0#	107	VCCP	72
AD26	88	GNDA	15	REQ1#	102	VCCP	84
AD27	89	GNDP	36	RREF	16	VCCP	94
AD28	98	GNDP	48	RST_SEL	91	VCCP	110
AD29	99	GNDP	58	SEG_A	118	VCCP	123
AD3	34	GNDP	73	SEG_B	119	VCCP_AUX	4
AD30	100	GNDP	95	SEG_C	120	VSS	22
AD31	101	GNDP	111	SEG_D	121	VSS	42
AD4	37	GNDP	124	SEG_E/GP0	127	VSS	60
AD5	38	GNDP_AUX	3	SEG_EN1/GP3	24	VSS	79
AD6	39	GNT0#	108	SEG_EN2/GP4	25	VSS	97
AD7	40	GNT1#	103	SEG_F/GP1	128	VSS	113
AD8	43	INTA#	65	SEG_G/GP2	32	VSS_AUX	6
AD9	44	INTB#	63	SERR#	56	WAKE#	1

5. Pin Description

5.1 IT8892E Pin Description

Table 5-1. IT8892E Pin Description of PCI Bus Interface

Pin(s) No.	Symbol	Attribute	Description
101, 100, 99, 98, 89, 88, 86, 85, 83, 82, 81, 80, 77, 76, 75, 74, 54, 53, 52, 51, 50, 45, 44, 43, 40, 39, 38, 37, 34, 33, 31, 30	**AD[31:0]**	PI/O	***PCI Address/Data Bus(32 pins)*** During the address phase, AD[31:0] contain the physical address of the PCI transaction. During the data phase, AD[31:0] contain the data.
87, 69, 49, 46	**CBE[3:0]#**	PI/O	***Command/Byte Enable (4 pins)*** During the address phase, CBE[3:0]# contain the bus command. During the data phase, CBE[3:0]# contain the byte enable. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]).
66	**DEVSEL#**	PI/O	***Device Select*** As an output, DEVSEL# indicates that the target (PCI slave) decodes its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus is selected.
71	**FRAME#**	PI/O	***FRAME*** Indicates the start of a PCI transaction.
106, 114, 103, 108	**GNT[3:0]#**	PI/O	***Bus Grant (4 pins)*** Indicates that the central arbiter granted the bus to an agent. When the internal PCI arbiter is enabled, GNT[3:0]# are outputs used to grant the bus to external devices. When the external PCI arbiter is enabled, GNT0# is an input used to grant the bus, and GNT[3:1]# are placed into a high-impedance state.
65, 63, 64, 116	**INTA#** **INTB#** **INTC#** **INTD#**	IK	***Interrupt (4 pins)*** Asserted to request an interrupt. After assertion, it is necessary to remain asserted until the device driver clears it. INTx# is level-sensitive and asynchronous to the CLK. All INTx# signals are mapped into Assert_INTx and Deassert_INTx messages on the PCI Express interface.
70	**IRDY#**	PI/O	***Initiator Ready*** Indicates that the initiator (PCI master) is ready to transfer data.
62	**LOCK#**	PI/O	***Lock Atomic Operation*** Indicates an atomic operation to a bridge that might require multiple transactions to complete.
122	**M66EN**	IK	***66 MHz Enable*** Indicates whether the PCI Bus is operating at 33 or 66 MHz.
61	**PAR**	PI/O	***Parity*** PAR is valid one clock after the address phase. For data phases, PAR is valid one clock after IRDY# is asserted on write cycles, and one clock after TRDY# is asserted on read cycles. PAR has the same timing as AD[31:0], except it is delayed by one clock cycle.
115	**PCIRST#**	PO	***PCI Reset*** This pin is to make a PCI device enter an initial state. PCIRST# is driven when a PCI Express reset is detected, or when the secondary bus reset bit of bridge control register is set.
55	**PERR#**	PI/O	***Parity Error*** Indicates that a Data Parity error occurrs. Driven active by the receiving agent two clocks following the data containing the bad parity.

Pin(s) No.	Symbol	Attribute	Description
105, 109, 102, 107	REQ[3:0]#	PI/O	***Bus Request (4 pins)*** Indicates that an agent requires the use of the bus. When the internal PCI arbiter is enabled, REQ[3:0]# are inputs used to service external bus requests. When the external PCI arbiter is enabled, REQ0# is an output used to request bus control, and REQ[3:1]# are unused inputs.
56	SERR#	PI/O	***System Error*** Indicates that an address parity error, data parity error on the special cycle command, or other catastrophic errors occur.
67	STOP#	PI/O	***STOP*** Indicates that the target (bus slave) is requesting that the master stops the current transaction.
68	TRDY#	PI/O	***Target Read*** Indicates that the target (bus slave) is ready to transfer data.
2	PME#	IK	***Power Management Event*** Input used to monitor the request to change the system's power state.

Table 5-2. IT8892E Pin Description of PCI Express Interface

Pin(s) No.	Symbol	Attribute	Description
18	DIN	AI	***Receive Minus*** PCI Express differential receive signal
17	DIP	AI	***Receive Plus*** PCI Express differential receive signal
117	PERST#	IK	***PCI Express Reset*** Reset IT8892E when asserted.
20	DON	AO	***Transmit Minus*** PCI Express differential transmit signal.
21	DOP	AO	***Transmit Plus*** PCI Express differential transmit signal.
9	CLKN	AI	***PCI Express Clock Input Minus*** PCI Express differential 100MHz reference clock.
10	CLKP	AI	***PCI Express Clock Input Plus*** PCI Express differential 100MHz reference clock.
1	WAKE#	OD	***Wake Signal*** Asserted when PME# is asserted and the link remains in the L2 state.

Table 5-3. IT8892E Pin Description of Miscellaneous Signal

Pin(s) No.	Symbol	Attribute	Description
27	EECLK	O8	***Serial EEPROM Clock*** Clock for EEPROM.
26	EECS#	O8	***Serial EEPROM Chip Select*** Chip select for EEPROM.
29	EERDDATA	IU	***Serial EEPROM Read Data*** Read data from EEPROM.
28	EEWRDATA	O8	***Serial EEPROM Write Data*** Write data to EEPROM.
92	EXTARB	IK	***External Arbiter Enable*** When low, the internal PCI arbiter is enabled. When high, IT8892E requests the PCI bus from an external PCI arbiter.
16	RREF	AO	***12-kΩ Resistance for Reference Current***
90	TEST_EN	IK	***Test Mode Enable***

Pin(s) No.	Symbol	Attribute	Description
104	PCICLK0	PI/O	***PCI Clock Output 0*** PCICLK0 outputs the clock for external PCI devices while PCICLK_SEL is pulled down whereas inputs the clock for internal PCI logic while PCICLK_SEL is pulled up, which means the bridge does not provide the clock to external devices. PCICLK0 outputs 62.5MHz with 50% duty cycle while M66EN is high whereas 33.3MHz with 50% duty cycle while M66EN is low.
93	PCICLK1	PI/O	***PCI Clock Output 1*** PCICLK1 outputs the clock for external PCI devices as PCICLK0, but it does not provide the function as an input clock pin.
91	RST_SEL	IK	***Reset Source Select Pin*** This pin has no functionality. Pull down this pin.
126	PCICLK_SEL	IK	***PCI Clock Source Select Pin*** This pin is used to select the internal clock or external clock buffer as the PCI clock source.
8	NC	-	***No Connect***

Table 5-4. IT8892E Pin Description of 7-Segment Display Signal

Pin(s) No.	Symbol	Attribute	Description
118	SEG_A	PO	***7-Segment LED A***
119	SEG_B	PO	***7-Segment LED B***
120	SEG_C	PO	***7-Segment LED C***
121	SEG_D	PO	***7-Segment LED D***
127	SEG_E/GP0	PIO	***7-Segment LED E / GPIO0***
128	SEG_F/GP1	PIO	***7-Segment LED F / GPIO1***
32	SEG_G/GP2	PIO	***7-Segment LED G / GPIO2***
24	SEG_EN1/ GP3	PIO	***7-Segment LED Common Pin for High Digit / GPIO3***
25	SEG_EN2/ GP4	PIO	***7-Segment LED Common Pin for Low Digit / GPIO4***

Table 5-5. IT8892E Pin Description of Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
35, 47, 57, 72, 84, 94, 110, 123	VCCP	I	***3.3V PAD Power***
36, 48, 58, 73, 95, 111, 124	GNDP	I	***Ground of PAD***
23, 41, 78, 96, 112, 125	VCCK	I	***1.8V Core Power***
22, 42, 60, 79, 97, 113,	VSS	I	***Ground of Core***
11, 12	VCC18A	I	***1.8V Analog Transceiver Power of PHY***
13, 14, 15	GNDA	I	***Analog Transceiver Ground of PHY***
19	VCC18A_AUX	I	***1.8V Analog AUX Power for AUX Power***
7	VCCK_AUX	I	***1.8V AUX Power for Core***
5	LDOAUX_18V	O	***1.8V LDO Output with Max 100mA***
59	LDO_18V	O	***1.8V LDO Output with Max 200mA***
6	VSS_AUX	I	***Ground for Core of AUX Power***
4	VCCP_AUX	I	***3.3V AUX Power for PAD***
3	GNDP_AUX	I	***Ground for PAD of AUX Power***

5.2 IT8893E Pin Description

Table 5-6. IT8893E Pin Description of PCI Bus Interface

Pin(s) No.	Symbol	Attribute	Description
101, 100, 99, 98, 89, 88, 86, 85, 83, 82, 81, 80, 77, 76, 75, 74, 54, 53, 52, 51, 50, 45, 44, 43, 40, 39, 38, 37, 34, 33, 31, 30	**AD[31:0]**	PI/O	***PCI Address/Data Bus(32 pins)*** During the address phase, AD[31:0] contain the physical address of the PCI transaction. During the data phase, AD[31:0] contain the data.
87, 69, 49, 46	**CBE[3:0]#**	PI/O	***Command/Byte Enable (4 pins)*** During the address phase, CBE[3:0]# contain the bus command. During the data phase, CBE[3:0]# contain the byte enable. CBE0# corresponds to byte 0 (AD[7:0]), and CBE3# corresponds to byte 3 (AD[31:24]).
66	**DEVSEL#**	PI/O	***Device Select*** As an output, DEVSEL# indicates that the target (PCI slave) decodes its address during the current bus transaction. As an input, DEVSEL# indicates whether a device on the bus is selected.
71	**FRAME#**	PI/O	***FRAME*** Indicates that the start of a PCI transaction.
103, 108	**GNT[1:0]#**	PI/O	***Bus Grant (2 pins)*** Indicates that the central arbiter granted the bus to an agent. When the internal PCI arbiter is enabled, GNT[1:0]# are outputs used to grant the bus to external devices. When the external PCI arbiter is enabled, GNT0# is an input used to grant the bus, and GNT[1]# is placed into a high-impedance state.
65, 63, 64, 116	**INTA#** **INTB#** **INTC#** **INTD#**	IK	***Interrupt (4 pins)*** Asserted to request an interrupt. After assertion, it is necessary to remain asserted until the device driver clears it. INTx# is level-sensitive and asynchronous to the CLK. All INTx# signals are mapped into Assert_INTx and Deassert_INTx messages on the PCI Express interface.
70	**IRDY#**	PI/O	***Initiator Ready*** Indicates that the initiator (PCI master) is ready to transfer data.
62	**LOCK#**	PI/O	***Lock Atomic Operation*** Indicates an atomic operation to a bridge that might require multiple transactions to complete.
122	**M66EN**	IK	***66 MHz Enable*** Indicates whether the PCI Bus is operating at 33 or 66 MHz.
61	**PAR**	PI/O	***Parity*** PAR is valid one clock after the address phase. For data phases, PAR is valid one clock after IRDY# is asserted on write cycles, and one clock after TRDY# is asserted on read cycles. PAR has the same timing as AD[31:0], except it is delayed by one clock cycle.
115	**PCIRST#**	PO	***PCI Reset*** This pin is to make a PCI device enter an initial state. PCIRST# is driven when a PCI Express reset is detected, or when the secondary bus reset bit of bridge control register is set.
55	**PERR#**	PI/O	***Parity Error*** Indicates that a Data Parity error occurs. Driven active by the receiving agent two clocks following the data containing the bad parity.

Pin(s) No.	Symbol	Attribute	Description
102, 107	REQ[1:0]#	PI/O	***Bus Request (2 pins)*** Indicates that an agent requires the use of the bus. When the internal PCI arbiter is enabled, REQ[1:0]# are inputs used to service external bus requests. When the external PCI arbiter is enabled, REQ0# is an output used to request bus control, and REQ[1]# is unused inputs.
56	SERR#	PI/O	***System Error*** Indicates that an address parity error, data parity error on the special cycle command, or other catastrophic error occurs.
67	STOP#	PI/O	***STOP*** Indicates that the target (bus slave) is requesting that the master stops the current transaction.
68	TRDY#	PI/O	***Target Ready*** Indicates that the target (bus slave) is ready to transfer data.
2	PME#	IK	***Power Management Event*** Input used to monitor the request to change the system's power state.

Table 5-7. IT8893E Pin Description of PCI Express Interface

Pin(s) No.	Symbol	Attribute	Description
18	DIN	AI	***Receive Minus*** PCI Express differential receive signal
17	DIP	AI	***Receive Plus*** PCI Express differential receive signal
117	PERST#	IK	***PCI Express Reset*** Reset IT8893E when asserted.
20	DON	AO	***Transmit Minus*** PCI Express differential transmit signal.
21	DOP	AO	***Transmit Plus*** PCI Express differential transmit signal.
9	CLKN	AI	***PCI Express Clock Input Minus*** PCI Express differential 100MHz reference clock.
10	CLKP	AI	***PCI Express Clock Input Plus*** PCI Express differential 100MHz reference clock.
1	WAKE#	OD	***Wake Signal*** Asserted when PME# is asserted and the link remains in the L2 state.

Table 5-8. IT8893E Pin Description of Miscellaneous Signal

Pin(s) No.	Symbol	Attribute	Description
27	EECLK	O8	***Serial EEPROM Clock*** Clock for EEPROM.
26	EECS#	O8	***Serial EEPROM Chip Select*** Chip select for EEPROM.
29	EERDDATA	IU	***Serial EEPROM Read Data*** Read data from EEPROM.
28	EEWRDATA	O8	***Serial EEPROM Write Data*** Write data to EEPROM.
92	EXTARB	IK	***External Arbiter Enable*** When low, the internal PCI arbiter is enabled. When high, IT8893E requests the PCI bus from an external PCI arbiter.
16	RREF	AO	***12-kΩ Resistance for Reference Current***
90	TEST_EN	IK	***Test Mode Enable***

Pin(s) No.	Symbol	Attribute	Description
104	PCICLK0	PI/O	***PCI Clock Output 0*** PCICLK0 outputs the clock for external PCI devices while PCICLK_SEL is pulled down whereas inputs the clock for the internal PCI logic while PCICLK_SEL is pulled up, which means the bridge does not provide the clock to external devices. PCICLK0 outputs 62.5MHz with 50% duty cycle while M66EN is high, and outputs 33.3MHz with 50% duty cycle while M66EN is low.
91	RST_SEL	IK	***Reset Source Select Pin*** This pin has no functionality. Pull down this pin.
126	PCICLK_SEL	IK	***PCI Clock Source Select Pin*** This pin is used to select the internal clock or external clock buffer as the PCI clock source.
109, 105	TP[1:0]	PI	***Test Pin*** ***Pull-up these pins at normal function mode.***
8, 93, 106, 114	NC	-	***No Connect***

Table 5-9. IT8892E Pin Description of 7-Segment Display Signal

Pin(s) No.	Symbol	Attribute	Description
118	SEG_A	PO	***7-Segment LED A***
119	SEG_B	PO	***7-Segment LED B***
120	SEG_C	PO	***7-Segment LED C***
121	SEG_D	PO	***7-Segment LED D***
127	SEG_E/GP0	PIO	***7-Segment LED E / GPIO0***
128	SEG_F/GP1	PIO	***7-Segment LED F / GPIO1***
32	SEG_G/GP2	PIO	***7-Segment LED G / GPIO2***
24	SEG_EN1/ GP3	PIO	***7-Segment LED Common Pin for High Digit / GPIO3***
25	SEG_EN2/ GP4	PIO	***7-Segment LED Common Pin for Low Digit / GPIO4***

Table 5-10. IT8893E Pin Description of Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
35, 47, 57, 72, 84, 94, 110, 123	VCCP	I	***3.3V PAD Power***
36, 48, 58, 73, 95, 111, 124	GNDP	I	***Ground of PAD***
23, 41, 78, 96, 112, 125	VCCK	I	***1.8V Core Power***
22, 42, 60, 79, 97, 113,	VSS	I	***Ground of Core***
11, 12	VCC18A	I	***1.8V Analog Transceiver Power of PHY***
13, 14, 15	GNDA	I	***Analog Transceiver Ground of PHY***
19	VCC18A_AUX	I	***1.8V Analog AUX Power***
7	VCCK_AUX	I	***1.8V AUX Power for Core***
5	LDOAUX_18V	O	***1.8V LDO Output with Max 100mA for AUX Power***
59	LDO_18V	O	***1.8V LDO Output with Max 200mA***
6	VSS_AUX	I	***Ground for Core of AUX Power***
4	VCCP_AUX	I	***3.3V AUX Power for PAD***
3	GNDP_AUX	I	***Ground for PAD of AUX Power***

Note: I/O cell types are described below:

I: Input PAD.
IU: Input PAD with Internal Pull-Up.
IK: Schmitt Trigger Input PAD.
AI: Analog Input PAD.
AO: Analog Output PAD.
PI/O: PCI Bus Specified Input/Output PAD.
PO: PCI Bus Specified Output PAD.
O: Output PAD.
OD: PCI Bus Specified Open Drain PAD.
O8: 8mA Output PAD.
All input pins are 5V tolerant except power and ground pins, PCI Express pins, EECLK, EECS#, and EEWRDATA.

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6. Functional Description

6.1 Register Description

6.1.1 Register Abbreviation

RO (**READ ONLY):** If a register is **read only**, writing data to this register has no effects.
WO (**WRITE ONLY):** If a register is **write only**, reading data to this register returns all zero.
R/W (**READ/WRITE):** A register with this attribute can be read and written data.
R/WS (READ/WRITE STICKY)**:** A register with this attribute can be read and written data.
R/WC (READ/WRITE CLEAR): A register bit with this attribute can be read and written data. However, writing 1 clears the corresponding bit and writing 0 has no effecst.
R/WCS (READ/WRITE CLEAR STICKY): A register bit with this attribute can be read and written data. However, writing 1 clears the corresponding bit and writing 0 has no effects.

The used radix indicator suffixes in this specification are listed below:
Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

6.1.2 List of PCI Configuration Registers

Table 6-1. List of Type 1 Header

31 24	23 16	15 8	7 0	Index
Device ID (8892h/8893h)		Vendor ID (1283h)		00h-03h
Status (0010h)		Command (0000h)		04h-07h
Base Class Code (06h)	Sub-Class Code (04h)	Programming Interface (01h)	Revision ID (40h)	08h-0Bh
BIST (00h)	Header Type (01h)	Latency Timer (00h)	Cache Line Size (00h)	0Ch-0Fh
Base Address Register 0 (00000000h)				10h-13h
Base Address Register 1 (00000000h)				14h-17h
Secondary Latency Timer (00h)	Subordinate Bus Number (00h)	Secondary Bus Number (00h)	Primary Bus Number (00h)	18h-1Bh
Secondary Status (0220h)		I/O Limit (01h)	I/O Base (01h)	1Ch-1Fh
Memory Limit (0000h)		Memory Base (0000h)		20h-23h
Prefetchable Memory Limit (0001h)		Prefetchable Memory Base (0001h)		24h-27h
Prefetchable Base Upper 32 Bits (00000000h)				28h-2Bh
Prefetchable Limit Upper 32 Bits (00000000h)				2Ch-2Fh
I/O Limit Upper 16 Bits (0000h)		I/O Base Upper 16 Bits (0000h)		30h-33h
Reserved (000000h)			Capabilities Pointer(90h)	34h-37h
Reserved (00000000h)				38h-3Bh

Bridge Control (0200h)		INTERRUPT PIN (01h)	INTERRUPT LINE (00h)	3Ch-3Fh
Initial Posted Flow Control Credit (00001008h)				40h-43h
Initial Non-Posted Flow Control Credit (000E9608h)				44h-47h
Initial Completion Flow Control Credit (00000000h)				48h-4Bh
Link Layer Control Register(000000FFh)				4Ch-4Fh
Transaction Layer Control Register (01B9ABF2h)				50h-53h
Reserved (00000000h)				54h-57h
PHY Control Register (008EC920h)				58h-5Bh
Reserved (00000000h)				5Ch-5Fh
Reserved (000000h)			PCI Port 80 Debug (00h)	60h-63h
Reserved (0000h)		PCI Control Register(1DAAh)		64h-67h
PCI PAD Control Register(00000000h)				68h-6Bh
Serial EEPROM Control Register (00000000h)				6Ch-6Fh
Dummy Register (0000FFFFh)				D0h-D3h
Transaction Layer Control Register1 (3FFE0059h)				E0h-E3h
Transaction Layer Control Register2 (AFFEE25Fh)				E4h-E7h
GPIO Output Enable Register (00h)	GPIO Output Register (00h)	GPIO Input Status (00h)	7-Segment Display Register (00h)	F0-F3h
Reserved (0000h)		GPIO Pull-Up Register (00h)	GPIO Pull-Down Register (1Fh)	F4-F8h

Table 6-2. List of PCI Express Capability

31 24	23 16	15 8	7 0	Index
PCI Express Capabilities (0071h)		Next Cap Pointer (90h)	PCI Express Cap ID (10h)	70h-73h
Device Capabilities (00000200h)				74h-77h
Device Status (0000h)		Device Control (0000h)		78h-7Bh
Link Capabilities (0103FC11h)				7Ch-7Fh
Link Status (0010h)		Link Control (0000h)		80h-83h

Table 6-3. List of Power Management Capability

31 24	23 16	15 8	7 0	Index
PM Capabilities (FE42h)		Next Cap Pointer (A0h)	PM Cap ID (01h)	90h-93h

Power Management Control and Status (00000000h)	94h-97h

Table 6-4. List of Subsystem ID and Subsystem Vendor ID Capability

31 24	23 16	15 8	7 0	Index
Reserved (0000h)		Next Cap Pointer (00h)	SSID Cap ID (0Dh)	A0h-A3h
Subsystem ID and Subsystem Vendor ID (00000000h)				A4h-A7h

Table 6-5. List of Device Serial Number Capability

31 24	23 16	15 8	7 0	Index
Device Serial Number Capability Header (00010003h)				100h-103h
Device Serial Number Register (00000000h)				104h-107h
Device Serial Number Register (00000000h)				108h-10Bh

6.2 Register Definition of PCI Configuration Register

6.2.1 Vendor ID Register (VID)

Address Offset: 00h

Bit	R/W	Default	Description
15-0	RO	1283h	**Vendor ID (VID)** 16-bit Vendor ID assigned to ITE VID = 1283.

6.2.2 Device ID Register (DID)

Address Offset: 02h

Bit	R/W	Default	Description
15-0	RO	8892h 8893h	**Device ID (DID)** Device number of ITE. 8892h for IT8892E. 8893h for IT8893E.

6.2.3 PCI Command Register (PCICMD)

Address Offset: 04h

Bit	R/W	Default	Description
15-11	RO	0h	**Reserved**
10	R/W	0b	**Interrupt Mask (INTMASK)** 0: Enable the bridge to generate Interrupt Messages on behalf of function. 1: Disable the bridge to generate Interrupt Messages on behalf of function.
9	RO	0b	**Fast Back-to-Back Transaction Enable (FBTE)** This function is not appled to PCI Express bridges and must be hardwired to 0.
8	R/W	0b	**SERR Enable (SE_EN)** This bit enables the bridge's reporting non-fatal and fatal errors to the Root Complex. In addition, it enables transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error messages on behalf of SERR# assertions detected on the secondary interface. Note that errors are reported if the function is enabled either through this bit or through the PCI Express specific bits in the Device Control register. 0: Disable 1: Enable
7	RO	0b	**Reserved**
6	R/W	0b	**Parity Error Response (PER)** This bit controls the bridge setting of the Master Data Parity Error bit in the Status register in response to the received poisoned TLP from PCI Express. 0: Disable 1: Enable
5	RO	0b	**VGA Platte Snoop (VGA_PS)** This function is not applied to PCI Express bridges and must be hardwired to 0.

4	RO	0b	**Memory Write and Invalidate (MWI)** The bridge does not optionally promote Memory Write Requests to Memory Write and Invalidate transactions on PCI.
3	RO	0b	**Special Cycle Enable (SCE)** This function is not applied to PCI Express bridges and must be hardwired to 0.
2	R/W	0b	**Bus Master Enable (BM_EN)** This bit controls device's ability to act as a master on the PCI bus. 0: Disable the device from generating PCI accesses. 1: Allow the device to behave as a bus master.
1	R/W	0b	**Memory Space Enable (MS_EN)** This bit controls the device's response to Memory Space accesses. 0: Disable the device response. 1: Allow the device to respond to Memory Space accesses.
0	R/W	0b	**I/O Space Enable (IOS_EN)** This bit controls the device's response to I/O Space accesses. 0: Disable the device response. 1: Allow the device to respond to I/O Space accesses.

6.2.4 Status Register (STS)

Address Offset: 06h

Bit	R/W	Default	Description
15	R/WC	0b	**Detected Parity Error (DPE)** This bit is set by the bridge whenever it receives a poisoned TLP regardless of the state the Parity Error Response bit in the Command register. 0: Data poisoning not detected by the bridge on its primary interface. 1: Data poisoning detected by the bridge on its primary interface.
14	R/WC	0b	**Signaled System Error (SSE)** This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message to the Root Complex and the SERR# Enable bit in the Command register is set. 0: Neither ERR_FATAL nor ERR_NONFATAL transmitted on primary interface. 1: ERR_FATAL or ERR_NONFATAL transmitted on primary interface.
13	R/WC	0b	**Received Master-Abort (RMA)** This bit is set when the bridge receives a Completion with Unsupported Request Completion Status on its primary interface. 0: Unsupported Request Completion Status not received on primary interface. 1: Unsupported Request Completion Status received on primary interface.
12	R/WC	0b	**Received Target-Abort (RTA)** This bit is set when the bridge receives a Completion with Completer Abort Completion Status on its primary interface. 0: Completer Abort Completion Status not received on primary interface. 1: Completer Abort Completion Status received on primary interface.
11	R/WC	0b	**Signaled Target-Abort (STA)** This bit is set when the bridge generates a completion with Completer Abort Completion Status in response to a request received on its primary

			interface. 0: Completer Abort Completion not transmitted on the primary interface. 1: Completer Abort Completion transmitted on the primary interface.
10-9	RO	00b	**DEVSEL# Timing (DVT)** This function is not applied to PCI Express bridges and must be hardwired to 00b.
8	R/WC	0b	**Master Data Parity Error (MDP)** This bit is used to report the detection of uncorrectable data errors by the bridge. It is set if the Parity Error Response bit in the Command register is set and either of the following two conditions occur: ∗ The bridge receives a Completion with data marked poisoned on the primary interface. ∗ The bridge poisons a write Request on the primary interface. 0: No uncorrectable data error detected on the primary interface. 1: Uncorrectable data error detected on the primary interface. Once set, this bit will remain set until it is reset by writing a 1 to its location. If the Parity Error Response bit is set to zero, this bit will not be set when an error is detected.
7	RO	0b	**Fast Back-to-Back Transactions Capable (FBC)** This function is not applied to PCI Express bridges and must be hardwired to 0.
6	RO	0b	**Reserved**
5	RO	0b	**66 MHz Capable (66CAP)** This function is not applied to PCI Express bridges and must be hardwired to 0.
4	RO	1b	**Capabilities List (CAPL)** Indicates the presence of a Capability List item.
3	RO	0b	**Interrupt Status (INTSTS)** Indicates that an INTx interrupt message is pending on behalf of sources internal to the bridge. This bit does not reflect the status of INTx inputs associated with the secondary interface (if present).
2-0	RO	0h	**Reserved**

6.2.5 Revision ID Register (REVID)

Address Offset: 08h

Bit	R/W	Default	Description
7-0	RO	40h	**Revision ID (REVID)**

6.2.6 Class Code Register (CC)

This register contains the base class code, sub class code, and programming interface for the device.

Address Offset: 09h

Bit	R/W	Default	Description
23-16	RO	06h	**Base Class Code (BCC)** The value of "06h" indicates that this is a bridge device.
15-8	RO	04h	**Sub Class Code (SCC)** 8-bit value that indicates this is of type PCI-to-PCI bridge.

7-0	RO	01h	**Programming Interface (PIF)** While legacy mode is enabled, PIF is read as 01h; otherwise, PIF is read as 00h (standard PCI-to-PCI bridge).

6.2.7 Cache Line Size Register (CLS)

This register indicates the cache line size of the system.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Cache Line Size (CLS)** This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.2.8 Master Latency Timer Register (MLT)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	RO	0h	**Time Value (TV)** The primary/master latency timer is not applied to PCI Express bridges. This register must be hardwired to 0.

6.2.9 Header Type Register (HEADTYP)

This register is used to indicate the layout for bytes 10h through 3Fh of the device's configuration space.

Address Offset: 0Eh

Bit	R/W	Default	Description
7	RO	0b	**Multi-Function Device (MFD)** Reserved as '0' to indicate the bridge is a single-function device.
6-0	RO	1h	**Header Type (HTYPE)** Defines the layout of addresses 10h through 3Fh in configuration space. Reads as 01h to indicate that the register layout conforms to the standard PCI Express-to-PCI/PCI-X bridge layout.

6.2.10 BIST Register (BIST)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	RO	0h	**BIST (BIST)** The bridge does not support BIST.

6.2.11 Base Address Register 0 (BAR0)

Address Offset: 10h

Bit	R/W	Default	Description
31-0	RO	0h	**Base Address Register 0 (BAR0)** The bridge does not support BAR.

6.2.12 Base Address Register 1 (BAR1)

Address Offset: 14h

Bit	R/W	Default	Description
31-0	RO	0h	**Base Address Register 1 (BAR1)** The bridge does not support BAR.

6.2.13 Primary Bus Number Register (PBN)

This register is used to record the bus number of the logical PCI bus segment to which the primary interface of the bridge is connected.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R/W	0h	**Primary Bus Number Register (PBN)** This field indicates the bus number of the PCI Express interface. Configuration software programs the value in this register. Any type 1 configuration cycle with a bus number less than this number will not be accepted by the bridge.

6.2.14 Secondary Bus Number Register (SCBN)

This register is used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected.

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R/W	0h	**Secondary Bus Number Register (SCBN)** This field indicates the bus number of PCI to which the secondary interface is connected. Any type 1 configuration cycle matching this bus number will be translated to a type 0 configuration cycle and run on the PCI bus.

6.2.15 Subordinate Bus Number Register (SBBN)

This register is used to record the bus number of the highest numbered PCI bus segment which is downstream of (or subordinate to) the bridge.

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	0h	**Subordinate Bus Number Register (SBBN)** This field indicates the highest PCI bus number below this bridge. Any type 1 configuration cycle on the PCI Express interface whose bus number is greater than the secondary bus number and less than or equal to the subordinate bus number will be run as a type 1 configuration cycle on the PCI bus.

6.2.16 Secondary Latency Timer Register (SLT)

Address Offset: 1Bh

Bit	R/W	Default	Description
7-3	R/W	0h	**Secondary Latency Timer Register (SLT)** This 5-bit value indicates the number of PCI clocks, in 8-clock increments, that the bridge remains as a master of the PCI bus if another master is requesting the suse of the PCI bus.
2-0	RO	0h	**Reserved**

6.2.17 I/O Base Register (IOB)

I/O base and I/O limit registers define the I/O range (aligned to a 4-Kbyte boundary) of the bridge. I/O accesses from the PCI Express interface within the range will be sent to PCI interface if the I/O space enable bit is set while those from the PCI interface out of range will be forwarded to PCI Express interface if the bus master space enable bit is set.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-4	R/W	0h	**I/O Base Address Bits [15:12] (IOBA)** This field defines the bottom address of an address range to determine when to forward I/O transactions from one interface to the other. These bits correspond to address lines 15:12 for 4 KB alignment. Bits 11:0 are assumed to be 000h.
3-0	RO	1h	**I/O Base Addressing Capability (IOBC)** These bits indicate whether to support 32-bit or 16-bit I/O address. 0000b: 16-bit I/O address. 0001b: 32-bit I/O address.

6.2.18 I/O Limit Register (IOL)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-4	R/W	0h	**I/O Limit Address Bits [15:12] (IOLA)** This field defines the top address of an address range to determine when to forward I/O transactions from PCI Express to PCI. These bits correspond to address lines 15:12 for 4 KB alignment. Bits [11:0] are assumed to be FFFh.
3-0	RO	1h	**I/O Limit Addressing Capability (IOLC)** These bits indicate whether to support 32-bit or 16-bit I/O address. 0000b: 16-bit I/O address. 0001b: 32-bit I/O address.

6.2.19 Secondary Status Register (SECSTS)

Address Offset: 1Eh

Bit	R/W	Default	Description
15	R/WC	0b	**Detected Parity Error (S_DPE)** This bit reports the detection of an uncorrectable address, attribute or

			data error by the bridge. This bit gets set regardless of whether the Parity Error Response Enable bit (bit 0 of offset 3E–3Fh) of the Bridge Control Register is set or not. 0: Uncorrectable address, attribute or data error not detected on the PCI interface. 1: Uncorrectable address, attribute or data error detected on the PCI interface.
14	R/WC	0b	**Received System Error (S_RSE)** This bit reports the detection of a SERR# assertion on the PCI interface. 0: SERR# assertion on the PCI interface has not been detected. 1: SERR# assertion on the PCI interface has been detected.
13	R/WC	0b	**Received Master-Abort (S_RMA)** This bit reports the detection of a Master-Abort termination by the bridge when it is the master of a transaction on its secondary interface. 0: Master-Abort not detected on secondary interface. 1: Master-Abort detected on secondary interface.
12	R/WC	0b	**Received Target-Abort (S_RTA)** This bit reports the detection of a Target-Abort termination by the bridge when it is the master of a transaction on its secondary interface. 0: Target-Abort not detected on secondary interface. 1: Target-Abort detected on secondary interface.
11	R/WC	0b	**Signaled Target-Abort (S_STA)** This bit reports the signaling of a Target-Abort termination by the bridge when it responds as the target of a transaction on its secondary interface. 0: Target-Abort not signaled on secondary interface. 1: Target-Abort signaled on secondary interface.
10-9	RO	01b	**DEVSEL# Timing (S_DVT)** This field indicates that the bridge responds in medium decode time to all cycles targeting the PCI Express interface.
8	R/WC	0b	**Secondary Master Data Parity Error (S_MDP)** This bit is used to report the detection of an uncorrectable data error by the bridge. It is set if the bridge is the bus master of the transaction on the secondary interface, the Parity Error Response Enable bit in the Bridge Control register is set, and either of the following two conditions occur: * The bridge asserts PERR# on a read transaction. * The bridge detects PERR# asserted on a write transaction. Once set, this bit will remain set until it is reset by writing a 1 to its location. If the Parity Error Response Enable bit is set to zero, this bit will not be set when an error is detected. 0: No uncorrectable data error detected on the secondary interface. 1: Uncorrectable data error detected on the secondary interface.
7	RO	0b	**Fast Back-to-Back Transactions Capable (S_FBC)** This bit indicates that the secondary interface is not able to receive fast back-to-back cycles.
6	RO	0b	**Reserved**
5	RO	1b	**66 MHz Capable (S_66CAP)** This bit indicates that the secondary interface of the bridge is 66 MHz-capable.
4-0	RO	0h	**Reserved**

6.2.20 Memory Base Register (MB)

Memory base and limit registers define the range (aligned to a 1-Mbyte boundary) of the non-prefetchable memory area of the bridge. Memory accesses from the PCI Express interface within the range will be sent to PCI nterface if the memory space enable bit is set while those from PCI nterface out of range will be forwarded to the PCI Express interface if the bus master enable bit is set.

Address Offset: 20h

Bit	R/W	Default	Description
15-4	R/W	0h	**Memory Base (MB)** These bits are compared with bits [31:20] of the incoming address to determine the range of the lower 1 MByte aligned value (inclusive). The incoming address must be greater than or equal to this value.
3-0	RO	0h	**Reserved**

6.2.21 Memory Limit Register (ML)

Address Offset: 22h

Bit	R/W	Default	Description
15-4	R/W	0h	**Memory Limit (ML)** These bits are compared with bits [31:20] of the incoming address to determine the range of the upper 1MByte aligned value (exclusive). The incoming address must be less than this value.
3-0	RO	0h	**Reserved**

6.2.22 Prefetchable Memory Base Register (PMB)

Address Offset: 24h

Bit	R/W	Default	Description
15-4	R/W	0h	**Prefetchable Memory Base Register (PMB)** These bits are compared with bits [31:20] of the incoming address to determine the range of the lower 1 MByte aligned value (inclusive). The incoming address must be greater than or equal to this value.
3-0	RO	1h	**64-bit Indicator (IS64B)** These bits indicate whether the 64-bit addressing is supported for the base or not. 0000b: 32-bit addressing for this space. 0001b: 64-bit addressing for this space.

6.2.23 Prefetchable Memory Limit Register (PML)

Address Offset: 26h

Bit	R/W	Default	Description
15-4	R/W	0	**Prefetchable Memory Limit Register (PML)** These bits are compared with bits [31:20] of the incoming address to determine the range of the upper 1MByte aligned value (exclusive). The incoming address must be less than this value.
3-0	RO	1h	**64-bit Indicator (IS64B)**

			These bits indicate whether the 64-bit addressing is supported for the limit or not. 0000b: 32-bit addressing for this space. 0001b: 64-bit addressing for this space.

6.2.24 Prefetchable Base Upper 32 Bits Register (PMB_UPPER)

This defines the upper 32 bits of the prefetchable address base register.

Address Offset: 28h

Bit	R/W	Default	Description
31-0	R/W	0h	**Prefetchable Memory Base Upper Portion (PMBU)** When the 64-bit indicator of prefetchable memory base indicates 32-bit addressing, this register is read only and returns 0h. When the 64-bit indicator of prefetchable memory base indicates 64-bit addressing, this register determines the upper 32-bit address of prefetchable memory transaction from the primary bus to secondary bus.

6.2.25 Prefetchable Limit Upper 32 Bits Register (PML_UPPER)

This defines the upper 32 bits of the prefetchable address limit register.

Address Offset: 2Ch

Bit	R/W	Default	Description
31-0	R/W	0h	**Prefetchable Memory Limit Upper Portion (PMLU)** When the 64-bit indicator of prefetchable memory limit indicates 32-bit addressing, this register is read only and returns 0h. When the 64-bit indicator of prefetchable memory limit indicates 64-bit addressing, this register determines the upper 32-bit address of prefetchable memory transaction from the primary bus to secondary bus.

6.2.26 I/O Limit Upper 16 Bits Register (IOLU16)

Address Offset: 30h

Bit	R/W	Default	Description
15-0	R/W	0h	**I/O Base High 16 Bits (IOBH)** When the capability of I/O base address indicates 16-bit addressing, this register is read only and returns 0h. When the capability of I/O base address indicates 32-bit addressing, this register determines the upper 16-bit address of I/O transaction from the primary bus to secondary bus.

6.2.27 I/O Base Upper 16 Bits Register (IOBU16)

Address Offset: 32h

Bit	R/W	Default	Description
15-0	R/W	0h	**I/O Limit High 16 Bits (IOLH)** When the capability of I/O limit address indicates 16-bit addressing, this register is read only and returns 0h. When the capability of I/O limit address indicates 32-bit addressing, this

			register determines the upper 16-bit address of I/O transaction from the primary bus to secondary bus.

6.2.28 Capabilities Pointer Register (CAPP)

This register is used to point to a linked list of additional capabilities implemented by the bridge.

Address Offset: 34h

Bit	R/W	Default	Description
7-0	RO	90h	**Capabilities Pointer (PTR)** These bits indicate that the pointer for the first entry in the capabilities list is at 90h in the configuration space, which is Power Management Capability. When the legacy mode is disabled, the value of these bits will be 70h.

6.2.29 Interrupt Line Register (INTRL)

This register communicates interrupt line routing information.

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Line (INTRL)** This register is used to convey the interrupt line routing information between the initialization code and the device driver. This is not used by the bridge.

6.2.30 Interrupt Pin Register (INTRP)

This register is used to indicate which interrupt virtual wire, if any, the bridge uses on behalf of internal sources.

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	RO	1h	**Interrupt Pin (INTRP)** The bridge uses INTA# virtual wire to signal an interrupt.

6.2.31 Bridge Control Register (BRIDGE_CNT)

This register provides extensions to the Command register that is specific to a bridge. The Bridge Control register provides the secondary interface with controls, many of which are the same as those provided by the Command register for the primary interface. Some bits affect operation of both interfaces of the bridge.

Address Offset: 3Eh

Bit	R/W	Default	Description
15-12	RO	0h	**Reserved**
11	R/W	0b	**Discard Timer SERR Enable (DTS_EN)** This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the Secondary Discard Timer expires and the delayed transaction is discarded from a queue in the bridge. The severity is selectable only if Advanced Error Reporting is supported.

			0: Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the Secondary Discard Timer. Note that an error message can still be sent if Advanced Error Reporting is supported and the delayed transaction Discard Timer Expired Mask bit is cleared. 1: Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the Secondary Discard Timer expires and the delayed transaction is discarded from a queue in the bridge.
10	R/WC	0b	**Discard Timer Status (DTS)** This bit is set to a 1 when the Secondary Discard Timer expires and delayed completion is discarded from a queue in the bridge. 0: No discard timer error. 1: Discard timer error.
9	R/W	1b	**Secondary Discard Timer (SDT)** The counter starts once the Completion (PCI Express Completion associated with the delayed transaction Request) has reached the head of the downstream queue of the bridge (i.e., All ordering requirements have been met and the bridge is ready to complete the delayed transaction with the originating master on the secondary bus). If the originating master does not repeat the transaction before the counter expires, the bridge will remove the delayed transaction from its queue and set the Discard Timer Status bit. 0: The Secondary Discard Timer counts 2^{15} PCI clock cycles. 1: The Secondary Discard Timer counts 2^{10} PCI clock cycles.
8	R/W	0b	**Primary Discard Timer (PDT)** This function is not relevant to the PCI Express interface. When Primary Discard Timer Enable is set, this bit is RW for software compatibility only. Otherwise this bit is read only.
7	RO	0b	**Fast Back-to-Back Enable (FB_EN)** The bridge cannot generate fast back-to-back cycles on the PCI bus from PCI Express interface initiated transactions.
6	R/W	0b	**Secondary Bus Reset (SBR)** This bit provides the function to force the assertion of RST# on the secondary interface. 0: Do not force the assertion of the secondary interface RST#. 1: Force the assertion of the secondary interface RST#.
5	R/W	0b	**Master-Abort Mode (MAM)** This bit controls the behavior of a bridge when it receives a Master-Abort termination (e.g., an Unsupported Request on PCI Express) on either interface. 0: Do not report Master-Aborts. When a UR response is received from PCI Express for non-posted transactions and the secondary side is operating in the conventional PCI mode, return FFFF FFFFh on reads and complete I/O writes normally. When a Master-Abort is received on the secondary interface for posted transactions initiated from the primary interface, no action is taken (i.e., All data is discarded.). 1: Report UR Completions from PCI Express by signaling Target-Abort on the secondary interface when the secondary interface is operating in the conventional PCI mode. For posted transactions initiated from the primary interface and Master-Aborted on the secondary interface, the bridge must return an ERR_NONFATAL (by default) or ERR_FATAL transaction (Provided the SERR# Enable bit is set in the Command

			register). The severity is selectable only if Advanced Error Reporting is supported.
4	R/W	0b	**VGA 16-bit Decode (V16D)** This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. It is meaningful only when the VGA Enable bit in this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. This read/write bit enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary whenever the VGA Enable bit is set to 1. 0: Execute 10-bit address decoding on VGA I/O accesses. 1: Execute 16-bit address decoding on VGA I/O accesses.
3	R/W	0b	**VGA Enable (VGA_EN)** This function is to modify the response of the bridge to VGA-compatible addresses. If this bit is set, the bridge will forward the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): * Memory accesses in the range from 000A 0000h to 000B FFFFh * I/O addresses in the first 64 KB of the I/O address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is in the range from 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases - Address[15:10] may possess any values and is not used in the decoding) If the VGA Enable bit is set, forwarding of VGA addresses is independent of the value of the ISA Enable bit (located in the Bridge Control register), the I/O address range and memory address range defined by the I/O Base and Limit registers, the Memory Base and Limit registers, and the Prefetchable Memory Base and Limit registers of the bridge. The forwarding of VGA addresses is qualified by the I/O Enable and Memory Enable bits in the Command register. 0: Do not forward VGA compatible memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address range. 1: Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O Enable and Memory Enable bits are set) independent of the I/O and memory address range and independent of the ISA Enable bit.
2	R/W	0b	**ISA Enable (I_EN)** This function is to modify the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge will block any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions will be forwarded if they address the last 768 bytes in each 1-KB block. See Section 11.2 of PCI Express Bridge Spec. for further details. 0: Forward all downstream I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1: Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of PCI I/O

			address space (top 768 bytes of each 1-KB block).
1	R/W	0b	**SERR Enable (S_EN)** This function is to control the forwarding of SERR# assertions from the secondary interface to the primary interface. The bridge will transmit an ERR_FATAL or ERR_NONFATAL cycle (See Chapter 10 of PCI Express Bridge Spec. for the mapping of errors to severity level) on the primary interface when all of the followings are true: * SERR# is asserted on the secondary interface. * This bit is set or Advanced Error Reporting is supported and the SERR# Assertion Detected Mask bit is cleared in the Secondary Uncorrectable Error Mask register. * The SERR# Enable bit is set in the Command register or the PCI Express-specific bits are set (Refer to Chapter 10 of PCI Express Bridge Spec. for details) in the Device Control register of the PCI Express Capability Structure. 0: Disable the forwarding of SERR# from the secondary interface to ERR_FATAL and ERR_NONFATAL (SERR# might still be forwarded if the SERR Advanced Error mask bit is cleared). Refer to Section 5.2.3.2 of PCI Express Bridge Spec. for details. 1: Enable the forwarding of secondary SERR# to ERR_FATAL or ERR_NONFATAL.
0	R/W	0b	**Parity Error Response Enable (PER_EN)** This function is to control the bridge's response to the uncorrectable address, attribute, and data errors on the secondary interface. 0: Ignore uncorrectable address, attribute, and data errors on the secondary interface. 1: Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface.

6.2.32 Initial Posted Flow Control Credit (IPTFCC)

Address Offset: 40h

Bit	R/W	Default	Description
31-20	RO	0h	**Reserved**
19	RO	0h	**Discontinued CBE# ECO Disable**
18-8	RO	10h	**Data Credit (DC)**
7-0	RO	08h	**Header Credit (HC)**

6.2.33 Initial Non-Posted Flow Control Credit (INPFCC)

Address Offset: 44h

Bit	R/W	Default	Description
31-20	RO	0h	**Reserved**
19	RO	1b	**MERGE Enhance Enable**
18	RO	1b	**RX_BACKOFF Enhance Enable**
17	RO	1b	**INFINITE_FCC Enhance Enable**
16	RO	0b	**CPL_RD_END Enhance Enable**
15	RO	1b	**TLP_CNT Enhance Enable**
14	RO	0b	**M66EN Status**

13	RO	0b	**Arbiter Parking ECO Disable**
12	RO	1b	**Reduce PD Enable**
11-8	RO	6h	**Data Credit (DC)**
7-0	RO	08h	**Header Credit (HC)**

6.2.34 Initial Completion Flow Control Credit (ICPLFCC)

Address Offset: 48h

Bit	R/W	Default	Description
31-20	RO	0h	**Reserved**
19-8	RO	00h	**Data Credit (DC)**
7-0	RO	00h	**Header Credit (HC)**

6.2.35 Link Layer Control Register (LLCR)

Address Offset: 4Ch

Bit	R/W	Default	Description
31-13	RO	0h	**Reserved**
12	R/W	0b	**Reduced TX FTS Enable (RD_TXFTS_EN)** 1: Enable reduction. 0: Disable reduction.
11-8	R/W	0h	**Reduced Number of TX FTS (RD_NTXFTS)** These bits indicate the reduced number of transmitted FTS. The original number of FTS needs to be transmitted is latched by N_FTS of TS1 and TS2 from the upstream device. While RD_TXFTS_EN is set, the total number of FTS to be transmitted will be the latched N_FTS minuses RD_NTXFTS.
7-0	R/W	FFh	**Number of FTS (NFTS)** These bits are used to decide N_FTS field in training sequence.

6.2.36 Transaction Layer Control Register (TLCR)

Address Offset: 50h

Bit	R/W	Default	Description
31-29	R/W	0h	**Max Read Size for PCI Memory Read Command**
28-26	R/W	0h	**Max Read Size for PCI Memory Read Line Command**
25-23	R/W	3h	**Max Read Size for PCI Memory Read Multiple Command**
22-20	R/W	3h	**Max Read Size for Second Memory Read, (Read Line or Read Multiple), Command**
19	R/W	1b	**Memory Read Pre-fetch Enable** When this bit is set, Transaction Layer will pre-fetch data of the next address segment. 0: Disable 1: Enable
18-15	R/W	3h	**Pre-fetch Maximum Count**
14	R/W	0b	**80 Port Forwarding** 0: Do not forward I/O write cycle for 80 port. 1: Forward I/O write cycle for 80 port.

13	R/W	1b	**Legacy Mode Enable** When this bit is set, the legacy support is enabled. 0: Disable 1: Enable
12	R/W	0b	**ITE Debug Mode** 0: Disable 1: Enable
11	R/W	1b	**Discard Timer Enable** 0: Disable 1: Enable
10	R/W	0b	**Malformed TLP Error Enable** When this bit is set, Transaction Layer can send the fatal-error message if malformed TLP is received. 0: Disable 1: Enable
9	R/W	1b	**Last Read Align Enable** When this bit is set, Transaction Layer requests memory read cycle and aligns the ending address at multiple of 0x10. 0: Disable 1: Enable
8	R/W	1b	**Infinite Completion Credit Enable** This bit is used to enable infinite completion credit for PCI Express link. 0: Disable 1: Enable
7	R/W	1b	**Memory Read Lock Enable (MRLE)** When this bit is set, Transaction Layer supports MRdLk command. When this bit is cleared, Transaction Layer replies an Unsupported Request for MRdLK command. 0: Disable 1: Enable
6	R/W	1b	**Completion Cache Enable (CCE)** When this bit is set, Transaction Layer will keep the residual completion data for a non-complete PCI transaction. 0: Disable 1: Enable
5-0	R/W	32h	**Max Completion Time Out Value (MAXCT)** This filed means the value count, in ms unit, for a completion time out.

6.2.37 PHY Control Register (PHYCR)

Address Offset: 58h

Bit	R/W	Default	Description
31-16	RO	008Eh	**SET_P[33~18]**
15-0	RO	C920h	**SET_P[17, 15~1]**

6.2.38 PCI Port 80 Debug Register (P80DR)

Address Offset: 60h

Bit	R/W	Default	Description

7-0	WO	0h	**PCI Port 80 Debug** This field contains the data value of I/O port 80 on the PCI side. When this register is written and 80 port forwarding bit is enabled, the bridge will generate I/O write cycle with a 0x0080 address.

6.2.39 PCI Control Register (PCICR)

Address Offset: 64h

Bit	R/W	Default	Description
31-26	RW	0h	**Enable Hide PCI Device Function** These bits are used to hide the PCI devices under this bridge. Each bit corresponds to its respective PCI device such as bit 26 mapping to device 0, bit 27 mapping to device 1, and so forth. 0: Disable 1: Enable
25-13	RO	0h	**Reserved**
12	RW	1h	**PCI Clock Slew Control** This bit is used to enable the fast slew for 33MHz. 0: Disable 1: Enable
11	RW	1b	**PCI Pull-Up Enable** This bit is used to enable the pull-up resistor on PCI control signals, including FRAME#, TRDY#, IRDY#,DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, REQ0~3#, PME#. 0: Disable 1: Enable
10	RO	1b	**Primary Discard Timer R/W Enable** This bit is used to enable the Primary Discard Timer R/W for software compatibility. It is programmed by EEPROM only. 0: Disable 1: Enable
9	RO	0b	**Reserved**
8	R/W	1b	**Enable PCI Arbiter Time Out (EPCIATO)** This bit is used to control the PCI arbiter to check a master gains the bus, but it does not use PCI bus in a small time interval. 0: Disable arbiter time out mechanism. 1: Enable arbiter time out mechanism.
7-0	R/W	AAh	**PCI Arbiter Priority (PCIAP)** This is a PCI Arbiter priority setting between bride Mater and REQ0~3. There are eight stages for the PCI Arbiter priority setting and each bit presents one stage respectively. 0: Priority of bridge master is lower than REQ0~3# at this stage. 1: Priority of bridge master is higher than REQ0~3# at this stage.

6.2.40 PCI PAD Skew Control Register (PPSCR)

Address Offset: 68h

Bit	R/W	Default	Description
31-16	RO	0h	**Reserved**

15-12	R/W	4h	**PCI Output PAD Skew Control**
11-8	R/W	4h	**PCI Input PAD Skew Control**
7-0	RO	0h	**Reserved**

6.2.41 Serial EEPROM Control Register (SEEPROMCR)

Address Offset: 6Ch

Bit	R/W	Default	Description
31	R/W	0b	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers are loaded from the serial EEPROM. Reading this bit returns 0 while initialization is in progress and 1 when initialization is completed.
30-27	RO	0h	**Reserved**
26-25	R/W	0h	**Serial EEPROM Clock Frequency** 00b: 3.125MHz. 01b: 6.25MHz 10b: 12.5MHz 11b: 25MHz
24-23	R/W	0h	**Serial EEPROM Address Width** These bits report the installed serial EEPROM's addressing width. When the addressing width cannot be determined, 00b is returned. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. 00b: Undetermined 01b: 1 byte 10b: 2 bytes 11b: 3 bytes
22	RO	0b	**Serial EEPROM Chip Select Active** This bit is set when the EECS# to the serial EEPROM is active. The Chip Select can be active across multiple byte operations.
21	RO	0b	**Serial EEPROM Present** This bit is set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the bridge.
20	RO	0b	**Serial EEPROM Valid** 1: Serial EEPROM with 5Ah in the first byte is detected.
19	RO	0b	**Serial EEPROM Busy** 1: Serial EEPROM Controller is busy performing a Byte Read or Write operation.
18	R/W	0b	**Serial EEPROM Chip Select Enable** 0: Disable 1: Enable
17	R/W	0b	**Serial EEPROM Byte Read Start** 1: A byte is read from the serial EEPROM, and accessed using the Serial EEPROM Read Data field. This bit will be automatically cleared when the Read operation is completed.
16	R/W	0b	**Serial EEPROM Byte Write Start** 1: Value in the Serial EEPROM Write Data field is written to the serial EEPROM. This bit will be automatically cleared when the Write operation is completed.

15-8	RO	0h	**Serial EEPROM Read Data** This function is to determine the byte read from the serial EEPROM when the Serial EEPROM Byte Read Start bit is set.
7-0	R/W	0h	**Serial EEPROM Write Data (SEEPROMWD)** This function is to determine the byte written to the serial EEPROM when the Serial EEPROM Byte Write Start bit is set, representing an opcode, address, or data being written to the serial EEPROM.

6.2.42 PCI Express Capability Identifier Register (EXP_CAPID)

These bits will be hidden with legacy mode.

Address Offset: 70h

Bit	R/W	Default	Description
7-0	RO	10h	**PCI Express Capability Identifier (PCIECAPI)** This function indicates the PCI Express Capability structure. This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure.

6.2.43 PCI Express Next Pointer Register (EXP_NXTP)

These bits will be hidden with legacy mode.

Address Offset: 71h

Bit	R/W	Default	Description
7-0	RO	90h	**Next Capabilities Pointer (NCPTR)** This function points to the next capabilities list pointer, which is the Power Management Capability.

6.2.44 PCI Express Capability Register (EXP_CAP)

These bits will be hidden with legacy mode.

Address Offset: 72h

Bit	R/W	Default	Description
15-8	RO	0h	**Reserved**
7-4	RO	7h	**Device/Port Type(DEVPORT)** This function indicates the type of PCI Express logical device. This device is a PCI Express-to-PCI/PCI-X Bridge (7h).
3-0	RO	1h	**Capability Version (CAPVER)** This function indicates PCI-SIG defined PCI Express capability structure version number.

6.2.45 PCI Express Device Capabilities Register (EXP_DEVCAP)

This register contains information about the PCI Express link capabilities. These bits will be hidden with legacy mode.

Address Offset: 74h

Bit	R/W	Default	Description

31-28	RO	0h	**Reserved**
27-26	RO	0h	**Captured Slot Power Limit Scale** This function specifies the scale used for the Slot Power Limit Value. The value is set by the Set Slot Power Limit message. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x
25-18	RO	0h	**Captured Slot Power Limit Value** This function specifies the upper limit on power supplied by slot in combination with the Slot Power Limit Scale value. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. The value is set by the Set Slot Power Limit message.
17-15	RO	0h	**Reserved**
14	RO	0b	**Power Indicator Present (PIP)** This bridge does not support PIP.
13	RO	0b	**Attention Indicator Present (AIP)** This bridge does not support AIP.
12	RO	0b	**Attention Button Present (ABP)** This bridge does not support ABP.
11-9	RO	1h	**Endpoint L1 Acceptable Latency (L1AL)** The acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state is 1 μs to less than 2 μs.
8-6	RO	0h	**Endpoint L0s Acceptable Latency (L0AL)** The acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state is less than 64 ns.
5	RO	0b	**Extended Tag Field Supported (ETFS)** This field indicates the maximum supported size of the Tag Field. The defined encodings are as the followings: 0: 5-bit Tag field supported 1: 8-bit Tag field supported This bridge supports 5-bit Tag field.
4-3	RO	0h	**Phantom Functions Supported (PFS)** No function number bits used for Phantom Functions.
2-0	RO	0h	**Supported Maximum Payload Size (SMPS)** This field indicates the maximum payload size that the bridge can support for TLPs. The defined encodings are as the followings: 000b: 128 bytes max payload size 001b: 256 bytes max payload size

6.2.46 PCI Express Device Control Register (EXP_DEVCNTL)

This register contains command bits that control the bridge behavior on the PCI Express bus. These bits will be hidden with legacy mode.

Address Offset: 78h

Bit	R/W	Default	Description

15	R/W	0b	**Bridge Configuration Retry Enable (BCR_EN)** When this field is set, the bridge is enabled to return a configuration retry response on the PCI Express bus for a configuration transaction to PCI.
14-12	R/W	0h	**Max_Read_Request Size (MRRS)** This field sets the maximum Read Request size for the device as a requester. The device must not generate the read request with the size exceeding the set value. 000b: 128 bytes max read request size
11	RO	0b	**Enable No Snoop (ENS)** This bridge never sets the No Snoop attribute in transactions it initiates.
10	RO	0b	**Auxiliary (AUX) Power PM Enable (AUXPWRPM_EN)** This bridge does not support this function.
9	RO	0b	**Phantom Function Enable (PF_EN)** This bridge does not support phantom function.
8	RO	0b	**Extended Tag Field Enable (ETF_EN)** This bridge supports the 5-bit tag only.
7-5	R/W	0h	**Maximum Payload Size (MPS)** This field sets the maximum TLP payload size for the device. The permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. 000b: 128 bytes
4	RO	0b	**Enable Relaxed Ordering (ERO)** This bridge does not support relaxed ordering.
3	R/W	0b	**Unsupported Request Reporting Enable (URR_EN)** 0: Disable 1: Enable
2	R/W	0b	**Fatal Error Reporting Enable (FER_EN)** 0: Disable 1: Enable
1	R/W	0b	**Non-Fatal Error Reporting Enable (NFER_EN)** 0: Disable 1: Enable
0	R/W	0b	**Correctable Error Reporting Enable (CER_EN)** 0: Disable 1: Enable

6.2.47 PCI Express Device Status Register (EXP_DSTS)

This register contains information on the PCI Express device status. These bits will be hidden with legacy mode.

Address Offset: 7Ah

Bit	R/W	Default	Description
15-6	RO	0h	**Reserved**
5	RO	0b	**Transaction Pending (TP)** When this bit is set, the bridge has issued Non-Posted Requests which have not been completed yet and the bridge will report this bit to be cleared only when all completions for any outstanding Non-Posted Requests have been received.
4	RO	0b	**AUX Power Detected (APD)** When this bit is set, the AUX power is detected by this bridge.

3	R/WC	0b	**Unsupported Request Detected (URD)** The bridge sets this bit when any unsupported requests from PCI Express are received, including those not claimed by the functions within the bridge but NOT including those forwarded to the PCI interface with completions returned with an unsupported request status.
2	R/WC	0b	**Fatal Error Detected (FERRD)** When this bit is set, a fatal error has been detected regardless of whether an error message was generated or not.
1	R/WC	0b	**Non-Fatal Error Detected (NFERRD)** When this bit is set, a nonfatal error has been detected regardless of whether the mask bit is set in advanced error capability or not.
0	R/WC	0b	**Correctable Error Detected (CERRD)** When this bit is set, a correctable error has been detected regardless of whether an error message is generated or not.

6.2.48 PCI Express Link Capabilities Register (EXP_LCAP)

This register identifies PCI Express Link specific capabilities. These bits will be hidden with legacy mode.

Address Offset: 7Ch

Bit	R/W	Default	Description
31-24	RO	1h	**Port Number (PN)** This field indicates the PCI Express Port number for the given PCI Express Link.
23-18	RO	0h	**Reserved**
17-15	RO	7h	**L1 Exit Latency (L1EL)** This field indicates the L1 exit latency is more than 64 μs for the given PCI Express Link.
14-12	RO	7h	**L0s Exit Latency (L0EL)** This field indicates the L0s exit latency is more than 4 μs for the given PCI Express Link.
11-10	RO	3h	**Active State Link PM Support (ASLPMS)** The bridge supports L0s and L1 Active State.
9-4	RO	1h	**Maximum Link Width (MLW)** This field indicates the maximum width of the given PCI Express Link.
3-0	RO	1h	**Maximum Link Speed (MLS)** This field indicates the maximum link speed of the given PCI Express Link. The defined encoding is as the following: 0001b 2.5 Gb/s Link

6.2.49 PCI Express Link Control Register (EXP_LCNTL)

This register controls PCI Express Link specific parameters. These bits will be hidden with legacy mode.

Address Offset: 80h

Bit	R/W	Default	Description
15-8	RO	0h	**Reserved**
7	R/W	0b	**Extended Synch (EXTS)** When this bit is set, it will force extended transmission of 4096 fast training sequence (FTS) ordered sets in FTS and an extra 1024 training

			sequence one (TS1) at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication. The default value for this bit is 0.
6	R/W	0b	**Common Clock Configuration (CCC)** When this bit is set, it will indicate this component and that at its opposite end of this link are operating with a distributed common reference clock while the value “0b” will indicate they are operating with asynchronous reference clock.
5-2	RO	0h	**Reserved**
1-0	R/W	0h	**Active State Link PM Control (ASLPMC)** This field controls the level of ASPM supported on the given PCI Express Link. The defined encodings are as the folowings: 00b: Disable 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled

6.2.50 PCI Express Link Status Register (EXP_LSTS)

This register controls PCI Express Link specific parameters. These bits will be hidden with legacy mode.

Address Offset: 82h

Bit	R/W	Default	Description
15-10	RO	0h	**Reserved**
9-4	RO	1h	**Negotiated Link Width (NLW)** This field indicates the negotiated width of the given PCI Express Link.
3-0	RO	0h	**Link Speed (LS)** This field indicates the negotiated Link speed of the given PCI Express Link. 0001b 2.5Gbps PCI Express Link

6.2.51 Power Management Capability ID Register (PM_CAPID)

Address Offset: 90h

Bit	R/W	Default	Description
7-0	RO	01h	**Capability ID (CAPID)** Capability ID indicates PCI compatible Power Management.

6.2.52 Power Management Next Pointer Register (PM_NXTPTR)

Address Offset: 91h

Bit	R/W	Default	Description
7-0	RO	A0h	**Next Capability Pointer (NCPTR)** This field points to the next capability list pointer, which is the Subsystem ID and Subsystem Vendor ID Capability.

6.2.53 Power Management Capabilities Register (PM_CAP)

Address Offset: 92h

Bit	R/W	Default	Description
15-11	RO	1Fh	**PME_Support (PMES)** PME# can be asserted from D0, D1, D2, $D3_{hot}$, $D3_{cold}$.
10	RO	1b	**D2 Support (D2S)** The bridge supports the D2 device state.
9	RO	1b	**D1 Support (D1S)** The bridge supports the D1 device state.
8-6	RO	1h	**AUX Current (AUXC)** The bridge supports the AUX power, and the maximum current required is 55mA.
5	RO	0b	**Device Specific Initialization (DSI)** The bridge does not require device specific initialization when transitioned to D0 from D3hot state, so this bit is zero.
4	RO	0b	**Reserved**
3	RO	0b	**PME Clock (PMECLK)** This function is not applicable to PCI Express and hence hardwired to 0.
2-0	RO	2h	**Version (VERS)** The bridge PM Implementation is compliant with the PCI Power Management Interface Specification Revision 1.1.

6.2.54 Power Management Control and Status Register (PM_CNTLSTS)

Address Offset: 94h

Bit	R/W	Default	Description
31-24	RO	0h	**Data (DAT)** The bridge does not support this data register.
23-16	RO	0h	**Reserved**
15	R/WCS	0b	**PME Status (PMEST)** This bit is set normally when the function will assert the PME# signal independent of the state of the PME_En bit.
14-13	RO	0h	**Data Scale (DATS)** This 2-bit read-only field indicates the scaling factor to be used when the value of the Data register is interpreted.
12-9	RO	0h	**Data Select (DATSEL)** This 4-bit field is used to select which data is to be reported through the Data register and Data Scale field.
8	R/WS	0b	**PME Enable (PME_EN)** 0: PME# assertion is disabled. 1: PME# assertion is enabled.
7-2	RO	0h	**Reserved**
1-0	R/W	0h	**Power State (PWR_ST)** This 2-bit field is used to not only determine the current power state of a function but also reset it to a new power state. The field values supported by the bridge are given below: 00b – D0 01b – D1 10b – D2 11b – D3hot If software attempts to write an unsupported reserved state to this field,

			the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

6.2.55 SSID Capability ID Register (SSID_CAPID)

Address Offset: A0h

Bit	R/W	Default	Description
7-0	RO	0Dh	**Capability ID (CAPID)** This function is to indicate Subsystem ID and Subsystem Vendor ID Capability.

6.2.56 SSID Next Pointer Register (SSID_NXTPTR)

Address Offset: A1h

Bit	R/W	Default	Description
7-0	RO	00h	**Next Capability Pointer (NCPTR)** Null pointer means the end of a linked list.

6.2.57 SSID Register (SSID)

Address Offset: A4h

Bit	R/W	Default	Description
31-16	RO	0h	**Subsystem ID (SSID)**
15-0	RO	0h	**Subsystem Vendor ID (SSVID)**

6.2.58 Dummy Register (DMR)

Address Offset: D0h

Bit	R/W	Default	Description
31-16	R/W	0000h	**Dummy Register [31:16] for ITE Use Only**
15-0	R/W	FFFFh	**Dummy Register [15:0] for ITE Use Only**

6.2.59 Transaction Layer Control Register1 (TLCR1)

Address Offset: E0h

Bit	R/W	Default	Description
31-29	R/W	1h	**Read Request Number for PCI Memory Read Command** These bits decide the first read request number of a TLP from PCI memory-read command and the length of each read request is aligned to 16 DW. 001b: 1 read request 010b: 2 read requests 011b: 3 read requests 100b: 4 read requests 101b: 5 read requests 110b: 6 read requests 111b: 7 read requests

			000b: 8 read requests
28-26	R/W	7h	**Read Request Number for PCI Memory Read Multiple Command** These bits decide the first read multiple request number of a TLP from PCI memory-read command and the length of each read request is aligned to 16 DW. 001b: 1 read request 010b: 2 read requests 011b: 3 read requests 100b: 4 read requests 101b: 5 read requests 110b: 6 read requests 111b: 7 read requests 000b: 8 read requests
25-23	R/W	7h	**Read Request Number for PCI Memory Read Line Command** These bits decide the first read line request number of a TLP from PCI memory-read command and the length of each read request is aligned to 16 DW. 001b: 1 read request 010b: 2 read requests 011b: 3 read requests 100b: 4 read requests 101b: 5 read requests 110b: 6 read requests 111b: 7 read requests 000b: 8 read requests
22-20	R/W	7h	**Read Request number for PCI Memory Read prefetch** These bits decide the prefetch read request number of a TLP from PCI memory-read command and the length of each read request is aligned to 16 DW. 001b: 1 read request 010b: 2 read requests 011b: 3 read requests 100b: 4 read requests 101b: 5 read requests 110b: 6 read requests 111b: 7 read requests 000b: 8 read requests
19	R/W	1h	**Downstream Post Request Merge Enable**
18	R/W	1h	**Downstream Completion Request Merge Enable**
17	R/W	1h	**Arbiter Priority AutoSset Based on Downstream Completion Ready**
16	R/W	0h	**Slave Latency Timer Enable**
15:12	R/W	0h	**PCI Master Number Count**
11-9	R/W	0h	**Slave Latency Timer Count**
8	R/W	0h	**Split Enable**
7	R/W	0h	**Split as 32 or 16**
6-5	R/W	2h	**MAX PCI Burst Length for Upstream MEMW**
4	R/W	1b	**Memory Read Command Prefetch Enable**
3	R/W	1b	**UPSTREAM Memory Request Length = 32 Enable**
2	R/W	0b	**Debug Mode**
1	R/W	0b	**Clk-50m Enable**

0	R/W	1b	**UPSTREAM Memory Request Length = 32 Controled by m66en**

6.2.60 Transaction Layer Control Register2 (TLCR2)

Address Offset: E4h

Bit	R/W	Default	Description
31-30	R/W	2h	**For ITE Use Only**
29	R/W	1h	**q_wrms** This is a function to control if the cached queue will be set as being removed when the upstream write command with the same master record in queue is issued. 0: Disable 1: Enable
28	R/W	0h	**q_rrms** This is a function to control if the cached queue will be set as being removed when the upstream discontinued read command with the same master record in queue is issued. 0: Disable 1: Enable
27	R/W	1h	**q_drms** This is a function to control if the cached queue will be set as being removed when the downstrean command is issued. 0: Disable 1: Enable
26-23	R/W	Fh	**Cpl_merge_cnt** The maximum merge count of the downstream is completed when there is another completion ready to return. These bits are meaningfull when bit 18 of E0h is set.
22-17	R/W	3Fh	**Grant Cache Enable Control** The cache function is enabled for each request master.
16	RO	0h	**For ITE Use Only**
15-12	R/W	Eh	**Prefetch Start Pointer** When this register meets the PCI address [5:2], the prefetch for the upstream read command will start**.**
11-7	R/W	4h	**Grms Count** This is a function to control if the cached queue will be set as being removed when the number of next few read commands with the same master record in queue is the same as this register..
6	R/W	1b	**Pd Next Match able to Pass through CPL and NPD**
5-1	R/W	Fh	**Cache Transfer Count**
0	R/W	1b	**Npd next Match able to Pass through CPL**

6.2.61 7-Segment Display Register (7SDR)

Address Offset: F0h

Bit	R/W	Default	Description
7-3	RO	0h	**Reserved**
2	R/W	0b	**7-Segment Display Function Enable** When 7-segment display function is disabled, SEG_E, SEG_F, SEG_G, SEG_EN1, and SEG_EN2 are used as GPIO pins.

			0: Disable 1: Enable
1	R/W	0b	**Enable Polarity for 7-Segment Display** 0: Drive SEG_EN1 or SEG_EN2 low while its corresponding 7-segment digit is turned on. 1: Drive SEG_EN1 or SEG_EN2 high while its corresponding 7-segment digit is turned on.
0	R/W	0b	**Data Polarity for 7-Segment Display** 0: Drive SEG_A, SEG_B, SEG_C, SEG_D, SEG_E, SEG_F, or SEG_G low while its corresponding LED is on. 1: Drive SEG_A, SEG_B, SEG_C, SEG_D, SEG_E, SEG_F, or SEG_G high while its corresponding LED is on.

6.2.62 GPIO Input Status (GPIOIS)

Address Offset: F1h

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4	RO	0b	**GPIO4 Input Status**
3	RO	0b	**GPIO3 Input Status**
2	RO	0b	**GPIO2 Input Status**
1	RO	0b	**GPIO1 Input Status**
0	RO	0b	**GPIO0 Input Status**

6.2.63 GPIO Output Register (GPIOOR)

Address Offset: F2h

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4	R/W	0b	**GPIO4 Output Data**
3	R/W	0b	**GPIO3 Output Data**
2	R/W	0b	**GPIO2 Output Data**
1	R/W	0b	**GPIO1 Output Data**
0	R/W	0b	**GPIO0 Output Data**

6.2.64 GPIO Output Enable Register (GPIOOER)

Address Offset: F3h

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4	R/W	0b	**GPIO4 Output Enable**
3	R/W	0b	**GPIO3 Output Enable**
2	R/W	0b	**GPIO2 Output Enable**
1	R/W	0b	**GPIO1 Output Enable**
0	R/W	0b	**GPIO0 Output Enable**

6.2.65 GPIO Pull-Up Register (GPIOPUR)

Address Offset: F4h

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4	R/W	0b	**GPIO4 Pull-Up** 0: Not Pull-Up 1: Pull-Up
3	R/W	0b	**GPIO3 Pull-Up** 0: Not Pull-Up 1: Pull-Up
2	R/W	0b	**GPIO2 Pull-Up** 0: Not Pull-Up 1: Pull-Up
1	R/W	0b	**GPIO1 Pull-Up** 0: Not Pull-Up 1: Pull-Up
0	R/W	0b	**GPIO0 Pull-Up** 0: Not Pull-Up 1: Pull-Up

6.2.66 GPIO Pull-Down Register (GPIOPDR)

Address Offset: F5h

Bit	R/W	Default	Description
7-5	RO	0h	**Reserved**
4	R/W	1b	**GPIO4 Pull-Down** 0: Not Pull-Down 1: Pull-Down
3	R/W	1b	**GPIO3 Pull-Down** 0: Not Pull-Down 1: Pull-Down
2	R/W	1b	**GPIO2 Pull-Down** 0: Not Pull-Down 1: Pull-Down
1	R/W	1b	**GPIO1 Pull-Down** 0: Not Pull-Down 1: Pull-Down
0	R/W	1b	**GPIO0 Pull-Down** 0: Not Pull-Down 1: Pull-Down

6.2.67 Device Serial Number Enhanced Capability Header (DSN_ECAPHDR)

Address Offset: 100h

Bit	R/W	Default	Description
31-20	RO	0h	**Next Capability Offset (NCO)** Null pointer means the end of a linked list.
19-16	RO	1h	**Capability Version (CAPVER)** This field indicates PCI-SIG defined PCI Express Capability structure version number.

15-0	RO	3h	**Capability ID (CAPID)** Extended Capability ID indicates Device Serial Number Capability.

6.2.68 Serial Number Register (DSN_SNR)

Address Offset: 104h

Bit	R/W	Default	Description
63-0	RO	0h	**PCI Express Device Serial Number** This field contains the IEEE defined 64-bit extended unique identifier, which includes a 24-bit company ID value assigned by IEEE registration authority and 40-bit extension identifier assigned by the manufacturer.

6.3 PCI Clock

IT8892E/IT8893E supports two PCI clock modes, internal clock and external clock. The mode is decided by the PCICLK_SEL pin. If PCICLK_SEL is set to low, the internal PCI clock mode will be selected while set to high, the external PCI clock mode will be selected.

When the internal PCI clock mode is selected, IT8892E/IT8893E has two output clock frequencies, 33.3MHz or 62.5MHz, and it depends on the M66EN pin. PCICLK0 and PCICLK1 output the same frequency with 50% duty cycle. All clock-trace lengths between IT8892E/IT8893E and PCI devices should be matched.

Figure 6-1. Internal Clock Mode with 33.3MHz Output

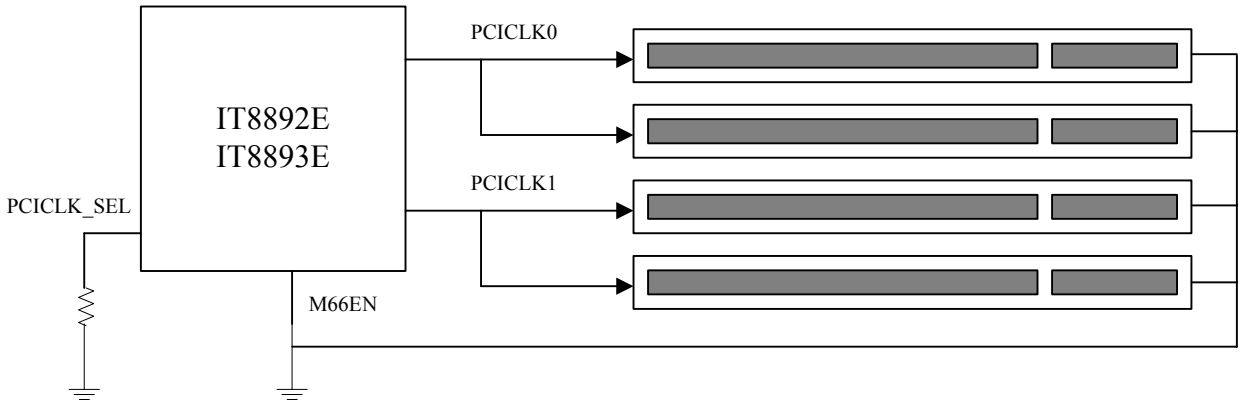
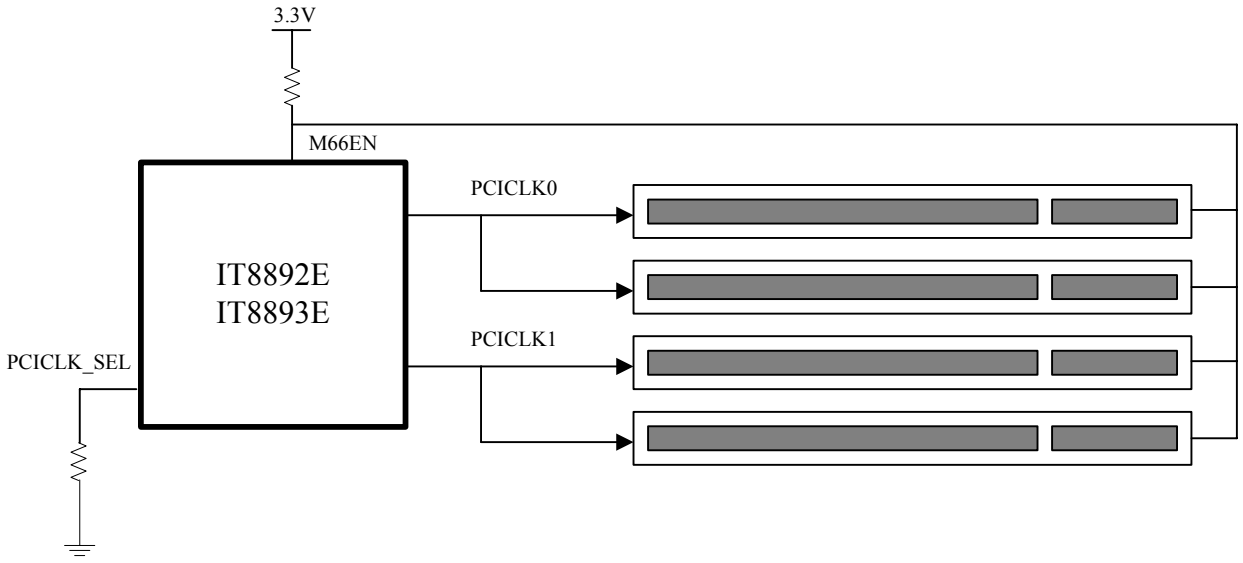
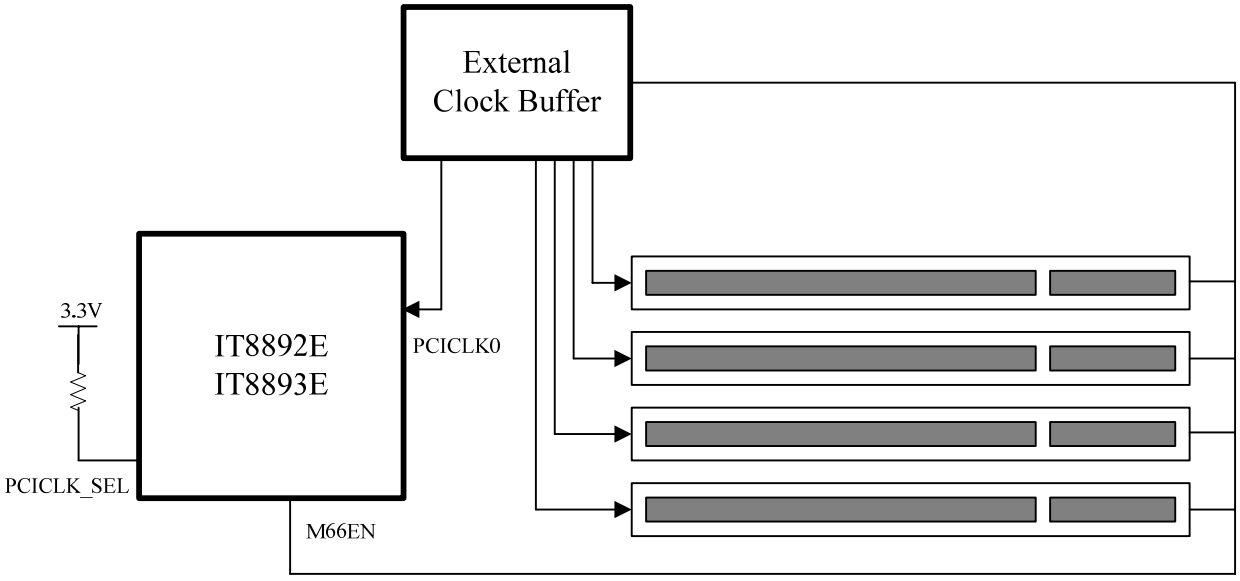


Figure 6-2. Internal Clock Mode with 62.5MHz Output



When the external PCI clock mode is selected, all PCI clock sources are from the external clock buffer. The PCI clock of IT8892E/IT8893E should be input from PCICLK0, and PCICLK1 is unused. All clock-trace lengths from the external clock buffer to IT8892E/T8893E and to PCI devices should be matched.

Figure 6-3. External Clock Mode



6.4 Reset

There are some reset sources for IT8892E/IT8893E. They are categorized as three types, and all of them bring registers, state machines, and buffers to default states. These reset sources will propagate the reset event to the secondary PCI bus, and configuration register will be updated by SPI EEPROM if EEPROM exists and its data content is valid. The PCI bus reset is also controlled by the secondary bus reset bit in the bridge control register, 0x3Eh bit<6>.

Fundamental Reset
The fundamental reset includes the cold reset and warm reset, both of which are from the PERST# pin. A cold reset occurs following the application of power to IT8892E/IT8893E. Sticky registers are only initialized by the cold reset. A warm reset is triggered by hardware without the removal and re-application of power to IT8892E/IT8893E.

Hot Reset
The hot reset is an in-band mechanism for propagating the reset across the link. IT8892E/IT8893E reaches Hot Reset by receiving TS1 ordered sets with the Hot Reset bit asserted.

DL_Down Reset
Data Link Layer reporting DL_Down is in some ways identical to a hot reset. DL_Down status indicates that there is no connection with another component on the Link or that the connection has been lost and is not recoverable by the Physical or Data Link Layer.

Table 6-6. Reset Summary

Reset Type	EEPROM Load	IT8892E/IT8893E Behavior
Cold Reset	Yes	● Registers are initialized. (Including sticky register) ● PCIRST# de-asserted 1ms after PERST# de-asserted.
Warm Reset	Yes	● Registers are initialized. ● All TLPs are dropped. ● PCIRST# de-asserted 1ms after PERST# de-asserted.
Hot Reset	Yes	● Registers are initialized. ● All TLPs are dropped. ● PCIRST# de-asserted 1ms after exiting hot reset state and link is up.
DL_Down Reset	Yes	● Registers are initialized. ● All TLPs are dropped. ● PCIRST# de-asserted 1ms after link is up.
Secondary Bus Reset	No	● PCIRST# asserted while 0x3Eh bit<6> is set. ● PCIRST# de-asserted 1ms after 0x3Eh bit<6> is cleared.

6.5 Power Management

IT8892E/IT8893E supports PCI-PM device power management states: D0, D1, D2, $D3_{cold}$, and $D3_{hot}$. It also supports PCI Express link power management state: L0, L0s, L1, L2/L3 Ready, L2, and L3 states.

- D0 state is divided into two sub-states. When power is applied, its default state is $D0_{uninitialized}$. IT8892E/IT8893E enters $D0_{active}$ whenever any singles or combinations of Memory Space Enable, I/O Space Enable, or Bus Master Enable bits are enabled.
- D1 and D2 states will make the bridge request entering L1 link power management state.
- D3 state will make bridge request entering L1 link power management state, and this is at $D3_{hot}$ state. The power state will be transitioned to $D3_{cold}$ by removing the main power from the host component.

IT8892E/IT8893E supports L0s and L1 active state power management (ASPM). L0 is a normal operational active state. Two standby link states, L0s and L1 are different levels of low power state. L0s state is optimized for short entry and exit latencies. L1 state is optimized at a cost of longer entry and exit latencies.

IT8892E/IT8893E in D0, D1, D2, and $D3_{hot}$ must respond to the receipt of a PME_Turn_Off message by the transmission of a PME_TO_Ack message. After this handshake sequence, IT8892E/IT8893E will request a link to transition to L2/L3 Ready using the PM_Enter_L23 DLLP. Following the L2/L3 Ready entry transition protocol, IT8892E/IT8893E will be ready for loss of main power and reference clock. If AUX power is provided by the platform, the link sleeps in L2. In the absence of AUX power, the link state is L3.

IT8892E/IT8893E has sticky registers, PME Enable (PME_EN) and PME Status (PME_ST) in power management control and status register. These registers will maintain the value through reset if AUX power is available and they are enabled for wakeup events. PCI device can assert PME# to signal change of its power state. IT8892E/IT8893E converts PME# signal information to PM_PME message to the upstream device.

IT8892E/IT8893E supports sideband WAKE# to wake up system.

6.6 PCI Intrrupt

PCI INTx interrupts are “virtualized” in PCI Express using Assert_INTx and Deassert_INTx messages, where x is A, B, C, and D for the respective PCI INTx# interrupt signals. This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INTx and Deassert_INTx messages transmitted on the PCI Express Link capture the asserting/deasserting edge of the respective PCI INTx# signal. IT8892E/IT8893E is a Multi-ported PCI Express bridge which collapses the INTA#-INTD# pins from each of their downstream conventional PCI/PCI-X interfaces into four INTx “virtual wires” on their Upstream Port.

6.7 PCI Arbiter

The IT8892E/IT8893E supports PCI External Arbiter or Internal Arbiter by setting the EXTARB pin high or low. The Internal arbiter of IT8892E/IT8893E accepts up to six requests from external PCI masters. The internal arbiter supports priority setting between the bridge master and external PCI masters PC the by PCI Arbiter Priority bits of the PCI control register. Please note that IT8893E provides two pairs of requests and grants.

Figure 6-4. IT8892E/IT8893E with Internal Arbiter

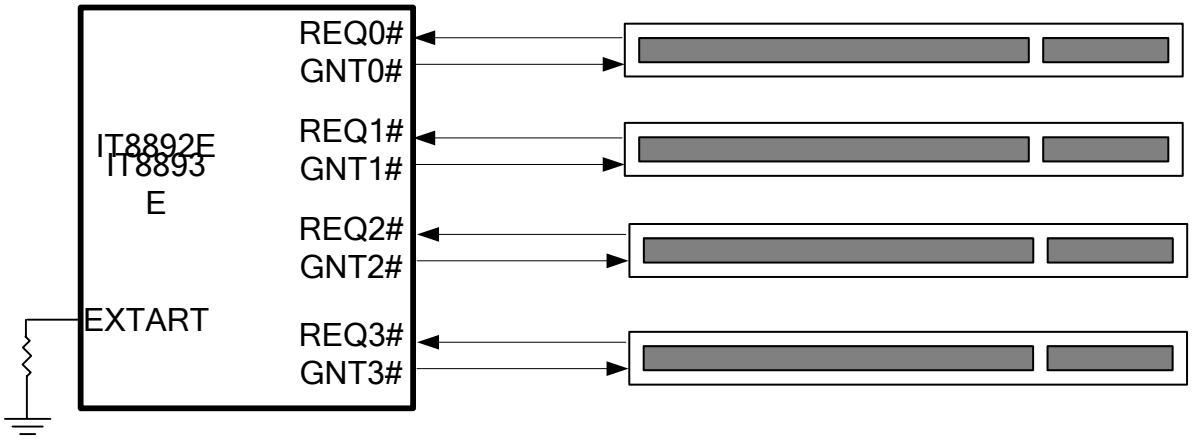
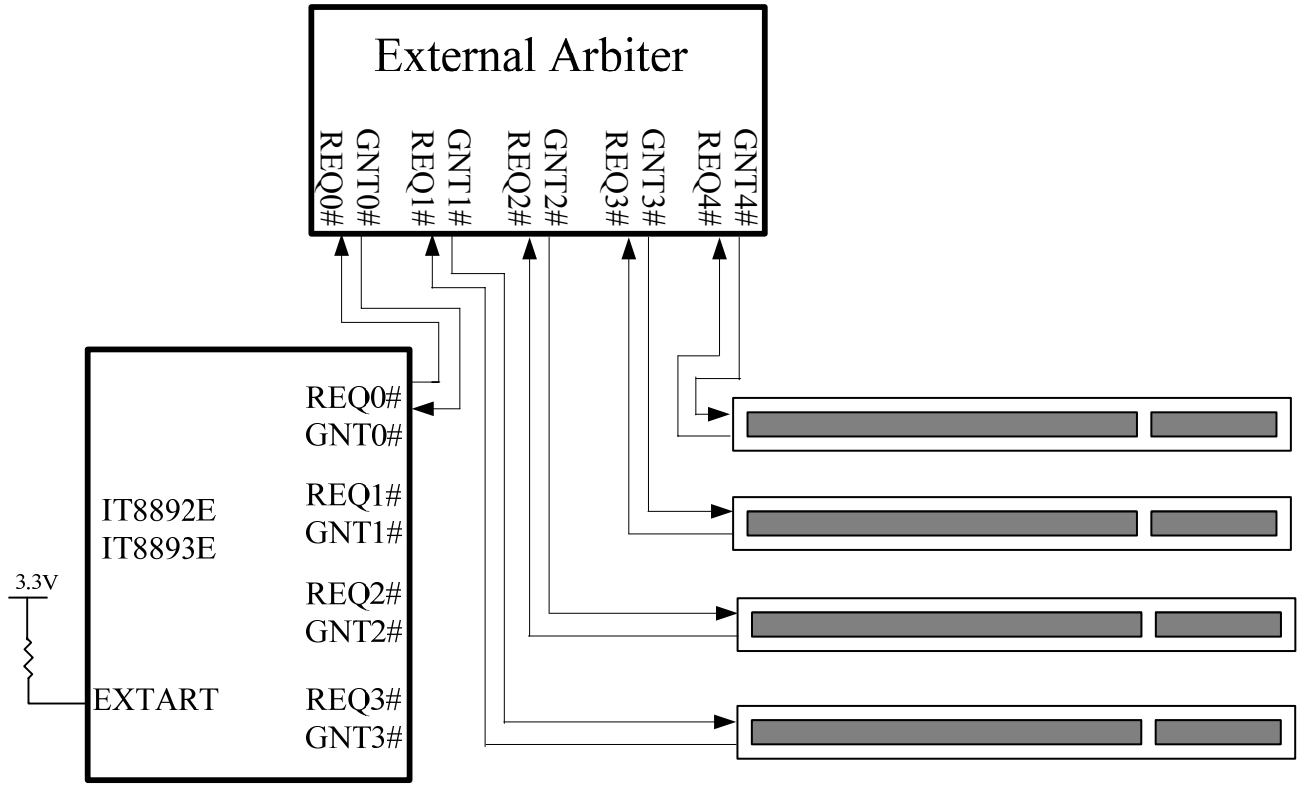


Figure 6-5. IT8892E/IT8893E with External Arbiter



6.8 EEPROM

6.8.1 Overview

The IT8892E/IT8893E offers an optional configuration method via the Serial Peripheral Interface (SPI) bus and operates at up to 25 MHz. Compatible 128-byte serial EEPROMs include the Atmel AT25010A and Catalyst CAT25C01. The IT8892E/IT8893E supports up to 16 MB serial EEPROM with one, two or three byte addressing. The addressing mode is determined by IT8892E/IT8893E automatically.

After the Reset of IT8892E/IT8893E is de-asserted, the EEPROM controller will automatically get the EEPROM status to check if there is serial EEPROM. When an EEPROM is detected, the controller will check the first byte. When a valid signature (5Ah) is read, the controller will keep reading until the EEPROM byte address reaches the byte count times six + 4. The frequency of serial EEPROM is determined by the bit 26-25 of the Serial EEPROM Control Register. The default frequency is 3.125MHz. For faster loading of large serial EEPROM that supports a faster clock, direct the first configuration register load from the serial EEPROM to the serial EEPROM Control register with a faster clock, which is to increase the serial EEPROM clock for the following read operation.

The data format in serial EEPROM is illustrated below:

Table 6-7. EEPROM Data Format

EEPROMByte Address	EEPROM Data	Description
0h	5Ah	Validation Signature
1h	Reserved	Reserved
2h	Byte Count (LSB)	Number of Cfg in EEPROM times six
3h	Byte Count (MSB)	
4h	First ADDR(LSB)	Address of Configuration Register
5h	First ADDR(LSB)	
6h	First DATA(Byte 0)	Data of Configuration Register
7h	First DATA(Byte 1)	
8h	First DATA(Byte 2)	
9h	First DATA(Byte 3)	
Ah	Second ADDR(LSB)	Address of Configuration Rregister
Bh	Second ADDR(LSB)	
Ch	Second DATA(Byte 0)	Data of Configuration Register
Dh	Second DATA(Byte 1)	
Eh	Second DATA(Byte 2)	
Fh	Second DATA(Byte 3)	
…..		

6.8.2 EEPROM Read Status Operation

1. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
2. Send Read Status command code (05h) to 0x6C bit<7:0>.
3. Set Chip Select Enable bit. (0x6Ch bit<18> = 1)
4. Set Write start. (0x6Ch bit<16> = 1)
5. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
6. Set Read start. (0x6Ch bit<17> = 1)
7. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
8. Get read data form 0x6Ch bit<15:8>.
9. Clear Chip Select Enable bit. (0x6Ch bit<18> = 0)

6.8.3 EEPROM Write Enable Operation

1. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0).
2. Send Write Enable command code (06h) to 0x6C bit<7:0>.
3. Set Chip Select Enable bit. (0x6Ch bit<18> = 1)
4. Set Write start. (0x6Ch bit<16> = 1)
5. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0).
6. Clear Chip Select Enable bit. (0x6Ch bit<18> = 0)

6.8.4 EEPROM Write Operation

1. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0).
2. Send Write command code (02h) to 0x6C bit<7:0>.
3. Set Chip Select Enable bit. (0x6Ch bit<18> = 1)
4. Set Write start. (0x6Ch bit<16> = 1)
5. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
6. Send Write address to 0x6C bit<7:0>.
7. Set Write start. (0x6Ch bit<16> = 1)
8. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
9. Send Write data to 0x6C bit<7:0>.
10. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
11. Clear Chip Select Enable bit. (0x6Ch bit<18> = 0)

Note 1: If the EEPROM address width is 2, repeat step 5, 6, 7 onece after step 7.
2: If the EEPROM address width is 3, repeat step 5, 6, 7 twice after step 7.

6.8.5 EEPROM Read Operation

1. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0).
2. Send Read command code (02h) to 0x6C bit<7:0>.
3. Set Chip Select Enable bit. (0x6Ch bit<18> = 1)
4. Set Write start. (0x6Ch bit<16> = 1)
5. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
6. Send Write address to 0x6C bit<7:0>.
7. Set Write start. (0x6Ch bit<16> = 1)
8. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
9. Set Read start. (0x6Ch bit<17> = 1)
10. Check the EEPROM idle. (Wait 0x6Ch bit<19> = 0)
11. Get read data form 0x6Ch bit<15:8>.
12. Clear Chip Select Enable bit. (0x6Ch bit<18> = 0)

Note 1: If the EEPROM address width is 2, repeat step 5, 6, 7 onece after step 7.
2: If the EEPROM address width is 3, repeat step 5, 6, 7 twice after step 7.

6.8.6 Suggested EEPROM Data Content

To inhance the performance and compatibility, here are the suggested EEPROM data content:

Table 6-8. Suggested EEPROM Data Content

EEPROM Byte Address	EEPROM Data	Description
0h	5Ah	Validation Signature
1h	00h	Reserved
2h	06h	Number of Cfg in EEPROM times six
3h	00h	
4h	50h	Adress of Configuration Register
5h	00h	
6h	72h	Data of Configuration Register
7h	8Ah	
8h	B9h	
9h	01h	

6.9 Legacy Mode

IT8892E/IT8893E supports not only the standard PCI-to-PCI bridge, but also the legacy mode for subtractive decode. When the legacy mode is enabled, 0x50h bit<13> is set and IT8892E/IT8893E will forward all Memory Read, Memory Write, I/O Read, and I/O Write cycles received from the upstream device, Root Complex or Switch, to the PCI side even though those cycles are not within the I/O or Memory range defined by the base and limit registers. The programming interface register is also changed to 01h to indicate software that the legacy mode and subtractive decoding is enabled. The PCI Express capablility list registers and device serial number capability registers will be reserved when the bridge is in the legacy mode. Read accesses to these registers will be completed normally on the bus and the data will be returned with 0 while write accesses to them will be completed normally on the bus and the data will be discarded.

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7. DC Characteristics

Absolute Maximum Ratings

Power Supply (VCCP) ..... -0.3V to 3.6V

Input Voltage..... -0.3V to VCC + 0.3V

Output Voltage..... -0.3V to VCC + 0.3V

Storage Temperature .....-40°C to 150°C

Commercial Operating Temperature..... 0°C to 70°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=3.0V~3.6V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	LVTTL	-	-	0.8	V
V_{IL}	Input low voltage (PCI PAD)	PCI	-0.5	-	0.3*VCCP	V
V_{IH}	Input high voltage	LVTTL	2.0	-	-	V
V_{IH}	Input high voltage (PCI PAD)	PCI	0.5*VCCP	-	VCCP+0.5	V
V_{OL}	Output low voltage	I_{OL}=2~16mA	-	-	0.4	V
V_{OL}	Output low voltage (PCI PAD)	I_{out}=1500uA	-	-	0.1*VCCP	V
V_{OH}	Output high voltage	I_{OH}=-2~-16mA	2.4	-	-	V
V_{OH}	Output high voltage (PCI PAD)	I_{out}=-500uA	0.9*VCCP	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	-	V
Vt+	Schmitt trigger positive going threshold voltage	LVTTL	-	1.6	2.0	V
R_{pu}	Input pull-up resistance	PU=high PD=low	40	75	190	KΩ
R_{pd}	Input pull-down resistance	PU=low PD=high	40	75	190	KΩ
I_{IL}	Input leakage current	No pull-up or pull-down	-10	±1	10	uA
I_{OZ}	Tri-state leakage current	No pull-up or pull-down	-10	±1	10	mA
C_{IN}	Input capacity		-	3.2	-	pF
C_{OUT}	Output capacity		-	3.2	-	pF
C_{BID}	Bi-directional buffer capacity		-	3.2	-	pF
V_{LDO}	LDO output voltage of LDO_18V		1.62		2	V
V_{LDO_AUX}	LDO output voltage of LDOAUX_18V		1.62		2	V

Note: The output voltages of built-in LDOs are only guranteed by the usage of this bridge.

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8. AC Characteristics

Figure 8-1. PCI Bus Timing Condition

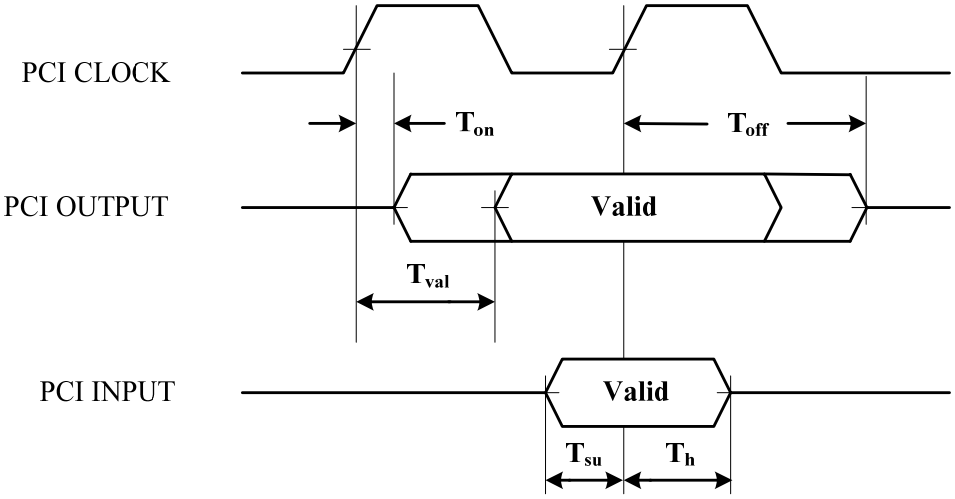

Table 8-1. PCI Bus AC Table

		33MHz			66MHz		
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Max.**	**Unit**
T_{cyc}	PCI Clock Cycle Time	-	30	-	15	-	ns
T_{cyc_out}	PCI Clock Cycle Time of Bridge Output	28.9	-	31.2	15.8	16.2	ns
T_{val}	CLK to Signal Valid Delay - bused signals	2	-	11	2	6	ns
$T_{val(ptp)}$	CLK to Signal Valid Delay - point to point signals[1]	2	-	12	2	6	ns
T_{on}	Float to Active Delay	2	-	-	2		ns
T_{off}	Active to Float Delay	-	-	28		14	ns
T_{h}	Input signal hold time from CLK	0	-	-	0	-	ns
T_{su}	Input Setup Time to CLK - bused signals	7	-	-	3	-	ns
$T_{su(ptp)}$	Input Setup Time to CLK - point to point signals	10,12	-	-	5	-	ns
T_{rst}	Reset Active Time after power stable	1	-	-	1	-	ms

Note: Point to point signals are REQ[3~0]#, and GNT[3~0]# for IT8892E. Point to point signals are REQ[1~0]#, and GNT[1~0]# for IT8893E.

Figure 8-2. Serial EEPROM Timing Condition

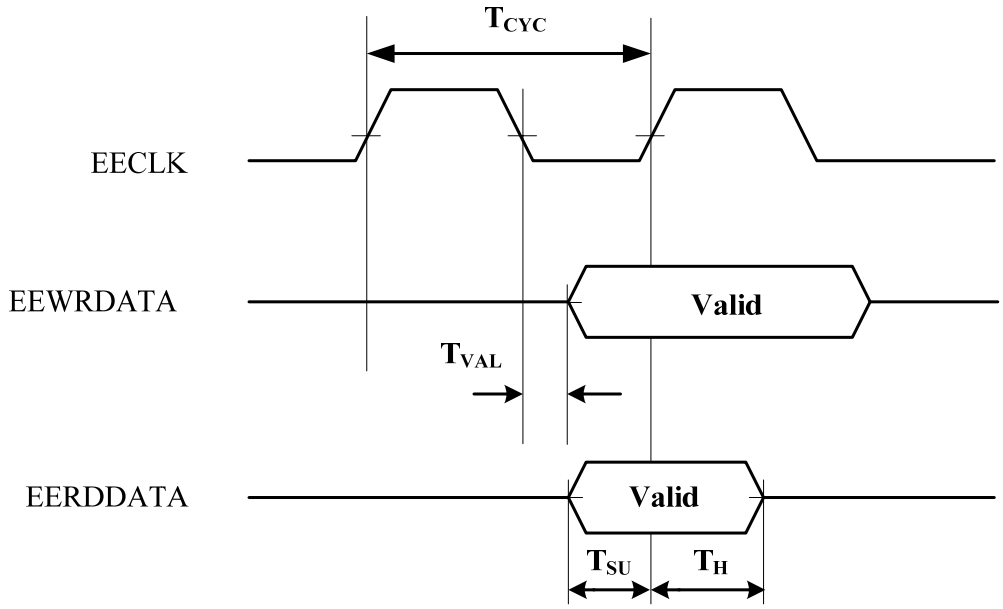

Table 8-2. Serial EEPROM AC Table

Symbol	Parameter	Min.	Max.	Unit
T_{CYC}	EECLK Clock Cycle Time	-	40	ns
T_{VAL}	EECLK to Signal Valid Delay	-	10	ns
T_{SU}	EERDDATA setup time	-	10	ns
T_{H}	EERDDATA hold time	10	-	ns

Note: EECS# must be asserted before accesses to the serial EEPROM and meet the CS# timing of serial EEPROM.

9. PCI Express Interface Characteristics

Table 9-1. PCI Express AC / DC Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input Levels						
$T_{RX-DIFF}$	High-speed differential input signals	$\|V_{RX(DIP)} - V_{RX(DIN)}\|$, measured at the connection of the end of a receiver.	87.5	-	600	mv
T_{RX-EYE}	Receiver eye time opening	Minimum eye time at Rx pins to yield a 10E-12 BER	0.4	-	-	UI
V_{IDLE}	Electrical idle detect threshold	IDLE is detected.	-	-	87.5	mV
		No IDLE is detected.	87.5	-	-	
$V_{RX-CM-AC}$	RX and AC common-mode voltage	Peak voltage	-	-	150	mV
Output Levels						
$V_{TX-DIFF}$	High-speed differential output signal	$\|V_{TX(DOP)} - V_{TX(DON)}\|$, measured at the connection of transmitter's near end.	400	-	600	mV
V_{TX-EYE}	Transmitter eye time opening	Minimum eye time at Rx pins to yield 10E-12 BER	0.75	-	-	UI
$V_{TX-IDLE-AC}$	Electrical idle differential peak output voltage	-	-	-	20	mV
V_{T-D-R}	The amount of voltage change allowed during receiver detection	The total amount of voltage change during TX-Detect-RX	-	-	600	mV
$V_{TC-CM-AC}$	TX AC common-mode voltage	AC RMS value	-	-	20	mV
V_{TC-DEM}	TX de-emphasis level	Transient bits are driven out with degrade amplitude.	-3	-	-4	dB
F_{BEACON}	A signal of wakeup mechanism	-	2	-	150	MHz
Resistance						
R_{RX}	Built-in receiver input impedance	-	40	50	60	Ohm
R_{TX}	Built-in driver output impedance	-	40	50	60	Ohm
Capacitance						
C_{TX}	AC coupling capacitor	-	75	-	200	nF

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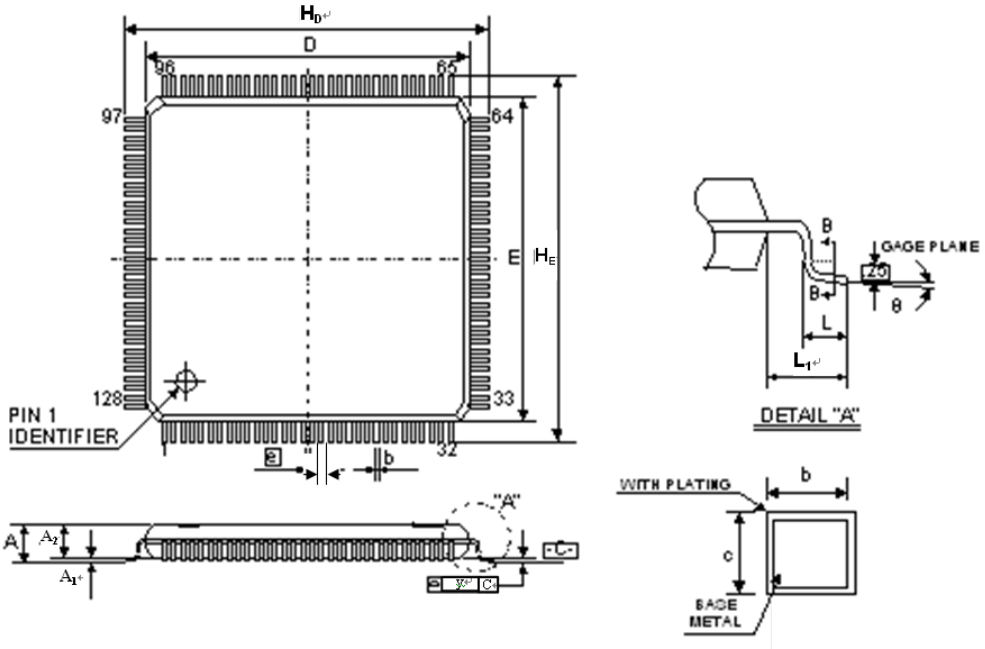
10. Package Information

LQFP 128 Outline Dimensons unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A_1	0.002	-	-	0.05	-	-
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1.Dimensions D and E do not include mold protrusion.

2.Dimensions b does not include dambar protrusion.
Total in excess of the b dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.

3.Controlling dimension : Millimeter

4.Reference document : JEDEC MS-026

DI-LQFP128(14*14)v4

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11. Ordering Information

Part No.	Package
IT8892E/FX	LQFP 128
IT8893E/FX	LQFP 128

All components provided are RoHS-compliant (100% Green Available).

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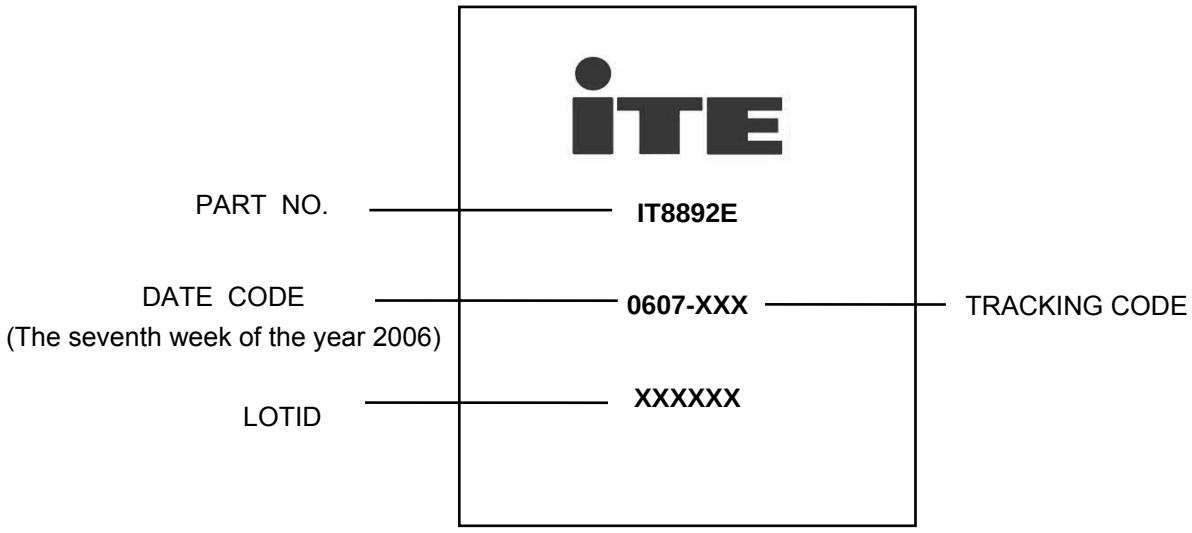
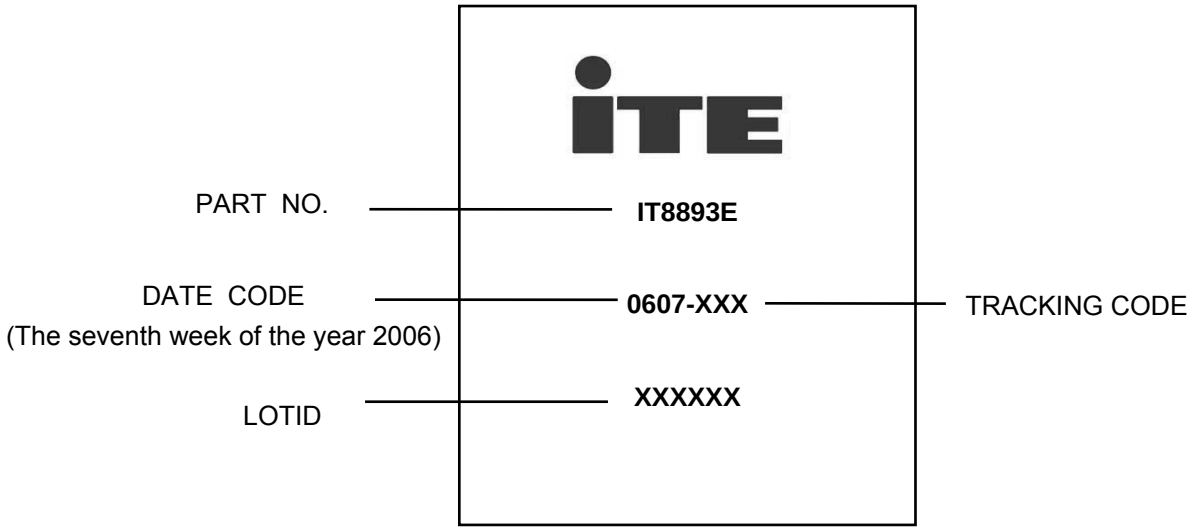
12. Top Marking Information





ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.