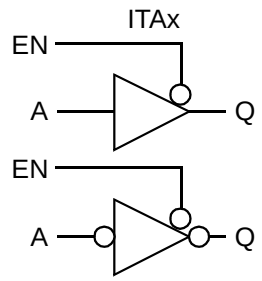
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ITAx is a family of non-inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

HDL Syntax

Verilog ..... ITAx *inst_name* (Q, A, EN);

VHDL..... *inst_name*: ITAx port map (Q, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITA1	ITA2	ITA4	ITA6
A	1.0	1.0	1.0	1.0
EN	1.7	2.3	3.4	4.6
Q	0.6	1.2	2.5	3.7

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITA1	2.0	TBD	3.9
ITA2	3.0	TBD	6.7
ITA4	6.0	TBD	12.4
ITA6	8.0	TBD	18.1

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	14	27	40	54 (max)
ITA1	From: A To: Q	t_{PLH} t_{PHL}	0.28 0.28	0.99 0.90	1.68 1.53	2.37 2.17	3.11 2.86
	From: EN To: Q	t_{ZH} t_{ZL}	0.17 0.18	0.85 0.84	1.52 1.46	2.20 2.09	2.92 2.78
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
ITA2	From: A To: Q	t_{PLH} t_{PHL}	0.28 0.28	0.84 0.82	1.41 1.38	1.95 1.90	2.52 2.44
	From: EN To: Q	t_{ZH} t_{ZL}	0.15 0.17	0.75 0.73	1.22 1.27	1.69 1.79	2.23 2.34
	Number of Equivalent Loads		**1**	**38**	**77**	**116**	**154 (max)**
ITA4	From: A To: Q	t_{PLH} t_{PHL}	0.38 0.35	0.85 0.82	1.34 1.30	1.86 1.77	2.36 2.24
	From: EN To: Q	t_{ZH} t_{ZL}	0.10 0.19	0.62 0.70	1.07 1.18	1.54 1.64	2.01 2.09
	Number of Equivalent Loads		**1**	**55**	**110**	**165**	**220 (max)**
ITA6	From: A To: Q	t_{PLH} t_{PHL}	0.43 0.43	0.91 0.95	1.39 1.39	1.86 1.83	2.34 2.31
	From: EN To: Q	t_{ZH} t_{ZL}	0.10 0.20	0.63 0.75	1.01 1.21	1.43 1.66	1.89 2.13

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ITA1	ITA2	ITA4	ITA6
EN	Q	t_{HZ} t_{LZ}	0.13 0.15	0.13 0.20	0.13 0.27	0.13 0.33