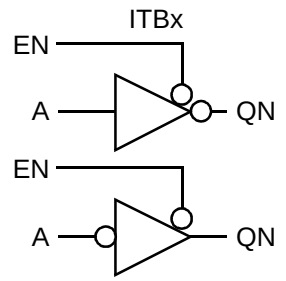
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ITBx is a family of inverting internal tristate buffers with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITBx *inst_name* (QN, A, EN);

VHDL..... *inst_name*: ITBx port map (QN, A, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITB1	ITB2	ITB4	ITB6
A	1.0	2.1	4.3	6.4
EN	1.7	2.3	3.5	4.7
QN	0.6	1.2	2.5	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITB1	2.0	TBD	2.8
ITB2	3.0	TBD	5.0
ITB4	5.0	TBD	7.4
ITB6	7.0	TBD	10.9

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	14	27	40	54 (max)
ITB1	From: A To: QN	t_{PLH} t_{PHL}	0.20 0.18	0.95 0.87	1.64 1.53	2.35 2.18	3.14 2.88
	From: EN To: QN	t_{ZH} t_{ZL}	0.05 0.17	0.86 0.86	1.57 1.52	2.26 2.17	3.00 2.89
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
ITB2	From: A To: QN	t_{PLH} t_{PHL}	0.15 0.15	0.75 0.71	1.33 1.24	1.89 1.73	2.50 2.26
	From: EN To: QN	t_{ZH} t_{ZL}	0.10 0.16	0.69 0.70	1.31 1.24	1.85 1.76	2.39 2.30
	Number of Equivalent Loads		**1**	**38**	**77**	**116**	**154 (max)**
ITB4	From: A To: QN	t_{PLH} t_{PHL}	0.02 0.16	0.68 0.62	1.20 1.06	1.68 1.51	2.12 1.98
	From: EN To: QN	t_{ZH} t_{ZL}	0.11 0.21	0.66 0.68	1.11 1.14	1.58 1.61	2.07 2.10
	Number of Equivalent Loads		**1**	**55**	**110**	**165**	**220 (max)**
ITB6	From: A To: QN	t_{PLH} t_{PHL}	0.09 0.15	0.65 0.65	1.14 1.08	1.65 1.53	2.18 2.00
	From: EN To: QN	t_{ZH} t_{ZL}	0.11 0.18	0.66 0.72	1.08 1.18	1.52 1.62	2.00 2.07

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ITB1	ITB2	ITB4	ITB6
EN	QN	t_{HZ} t_{LZ}	0.14 0.16	0.13 0.19	0.13 0.26	0.13 0.31