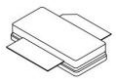
700MHz-1000MHz, 150W, 28V High Power RF LDMOS FETs

Description

The ITBH09150B is a 150-watt, internally matched LDMOS FET, designed for CDMA/WCDMA and multicarrier GSM base station applications with frequencies from 700 to 1000 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

ITBH09150B2



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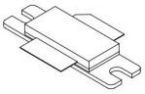


- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, IDQ = 1000 mA, Pulse CW, Pulse Width=100 us, Duty cycle=10% .

Frequency	Gp (dB)	P_{-1dB} (dBm)	η_D@P_{-1} (%)	P_{-3dB} (dBm)	η_D@P_{-3} (%)
960 MHz	20.5	51.9	62.5	53	67.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+75	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	75			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA

Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 0.8 mA)	$V_{GS}(th)$		2.1		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 1000 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.6	3.1	3.6	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) : V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 960 MHz, Pulse CW Signal Measurements.

(Pulse Width=100 μs, Duty cycle=10%)

Power Gain	Gp		20.5		dB
Drain Efficiency@P3dB	η_D		67.9		%
1 dB Compression Point	P_{-1dB}		51.9		dBm
3dB Compression Point	P_{-3dB}		53		dBm
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 1000 mA, f = 960 MHz

VSWR 10:1 at 150W pulse CW Output Power	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram

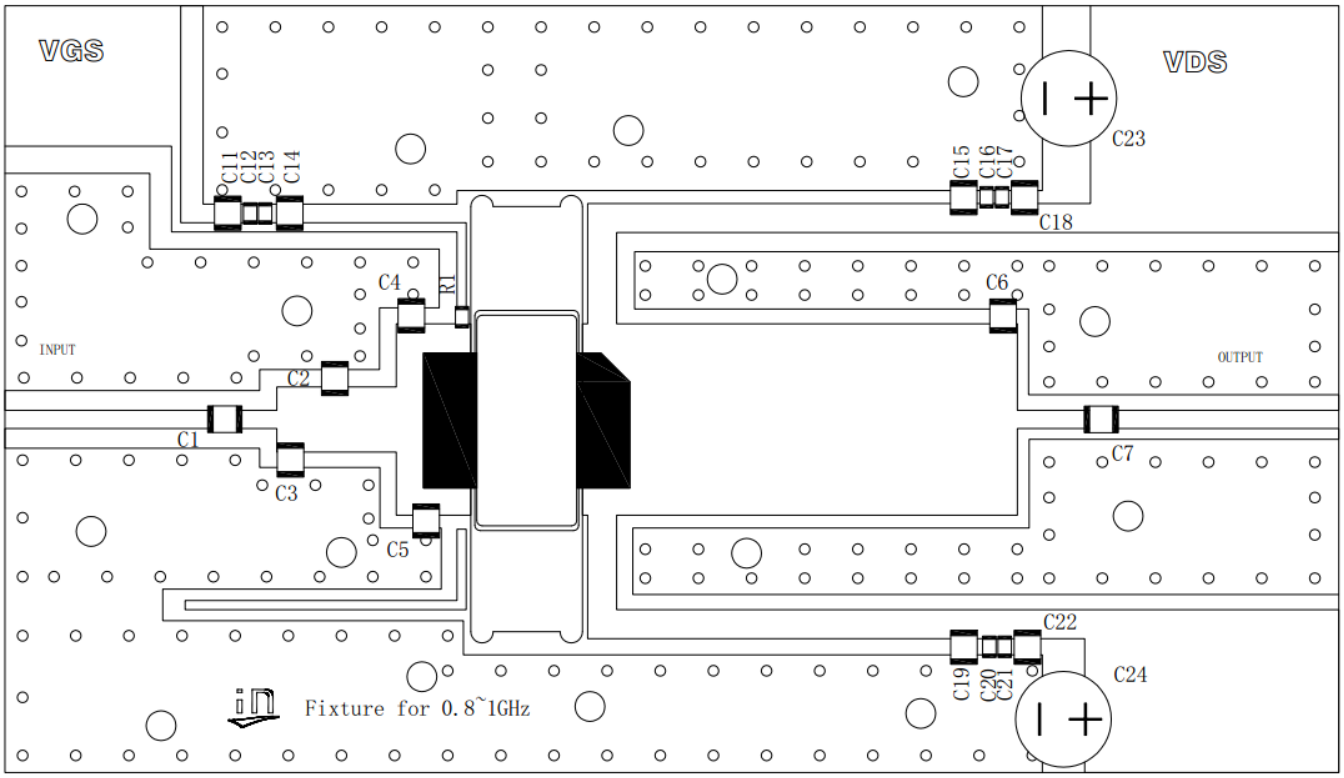


Figure 1. ITBH09150B Test Circuit Component Layout (920MHz~960MHz)

Table 5. ITBH09150B（920Mz~960MHz）Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C1,C7,C14,C15,C19	Ceramic Capacitor,47pF	ATC	800B470
C2	Ceramic Capacitor,6.2pF	ATC	800B 6R2
C3	Ceramic Capacitor,2.7pF	ATC	800B 2R7
C4,C5	Ceramic Capacitor,9.1pF	ATC	800B 9R1
C6	Ceramic Capacitor,1.0pF	ATC	800B 1R0
C13,C16,C20	Capacitor,1000pF	Murata	GRM21BR71H102
C12,C17,C21	Capacitor,0.1uF	Murata	GRM21BR71H104
C11,C18,C22	Capacitor,10uF	Murata	GRM32DF51H106
C23,C24	Electrolytic Capacitor ,470uF,63V	Vishay	MAL203858471E3
R1	Chip Resistor,10Ω	Digi-Key	P10ECT-ND
PCB	0.76mm [0.030"] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

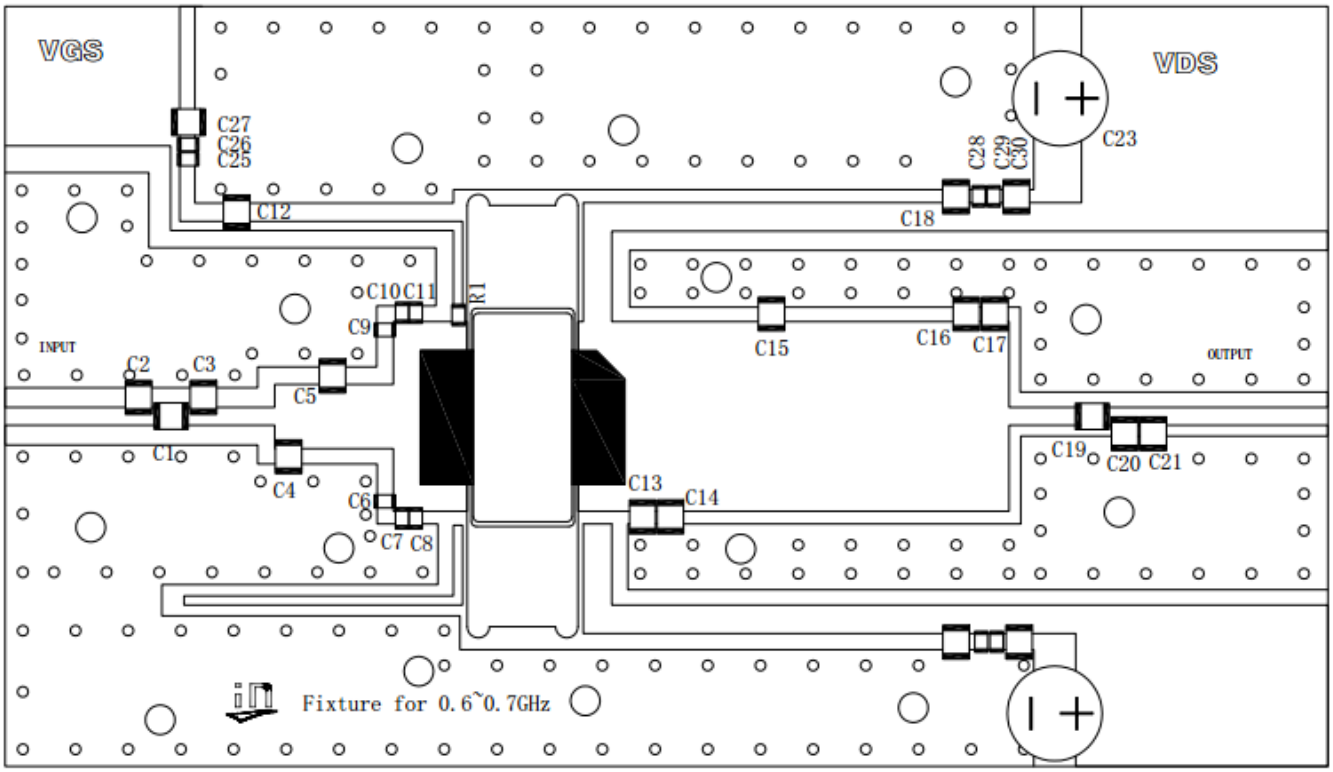


Figure 2. ITBH09150B Test Circuit Component Layout (610MHz~680MHz)

Table 6. ITBH09150B（610Mz~680MHz）Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer	P/N
C1,C12,C18,C19	Ceramic Capacitor,47pF	ATC	
C2	Ceramic Capacitor,1.2pF	ATC	
C3,C14	Ceramic Capacitor,4.7pF	ATC	
C4,C5,C6,C7,C8,C9,C10,C11,C13	Ceramic Capacitor,10pF	ATC	
C15,C16,C17	Ceramic Capacitor,5.6pF	ATC	
C20,C21	Ceramic Capacitor,2.7pF	ATC	
C25,C28	Capacitor,1000pF	Murata	
C26,C29	Capacitor,0.1uF	Murata	
C27,C30	Capacitor,10uF	Murata	
C23	Electrolytic Capacitor ,470uF,63V	Vishay	
R1	Chip Resistor,10Ω	Digi-Key	
PCB	0.76mm [0.030"] thick, εr=3.48, Rogers RO4350, 1 oz. copper		

TYPICAL CHARACTERISTICS

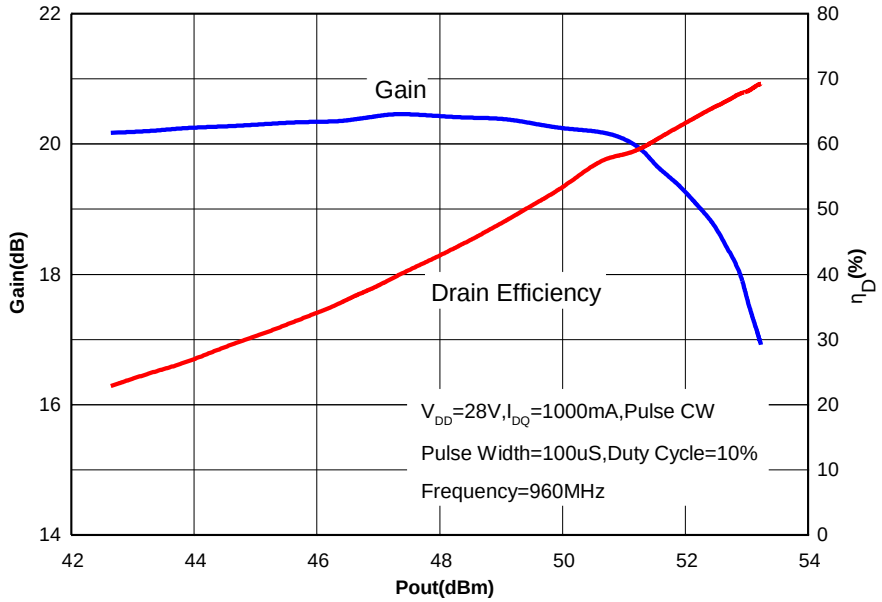


Figure 2. Power gain and drain efficiency as function of average load power (920MHz~960MHz)

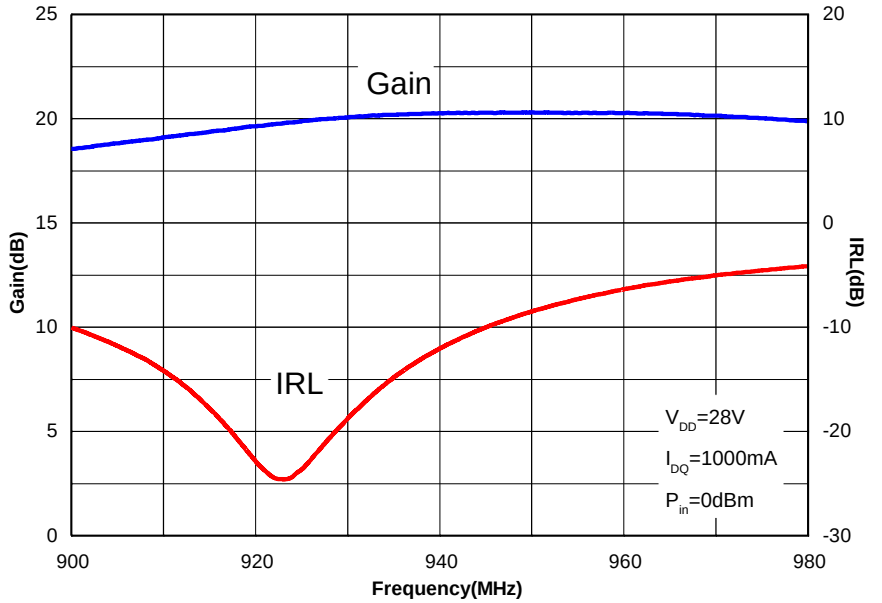
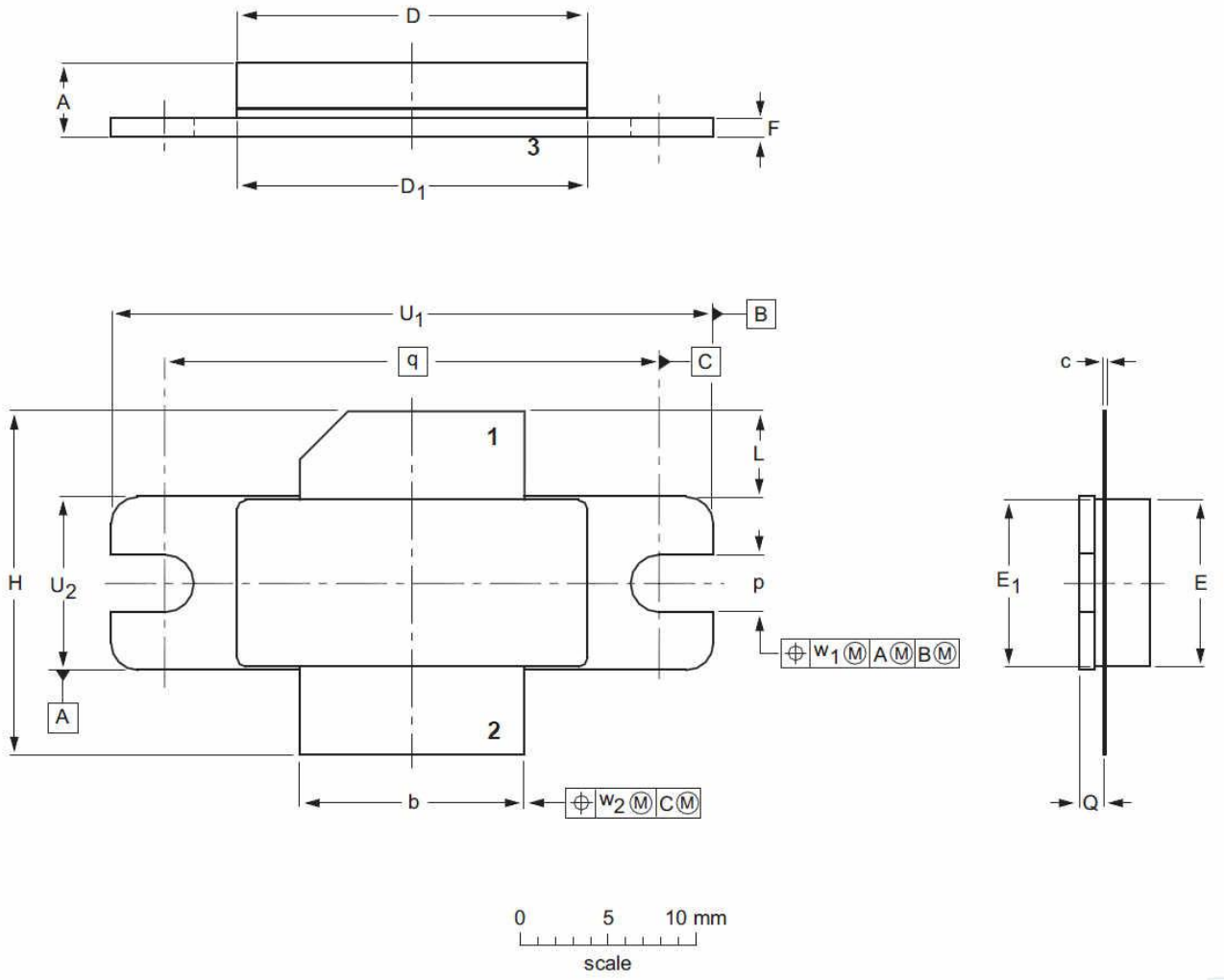


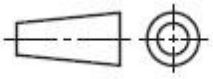
Figure 3. Broadband Frequency Response (920MHz~960MHz)

Package Outline

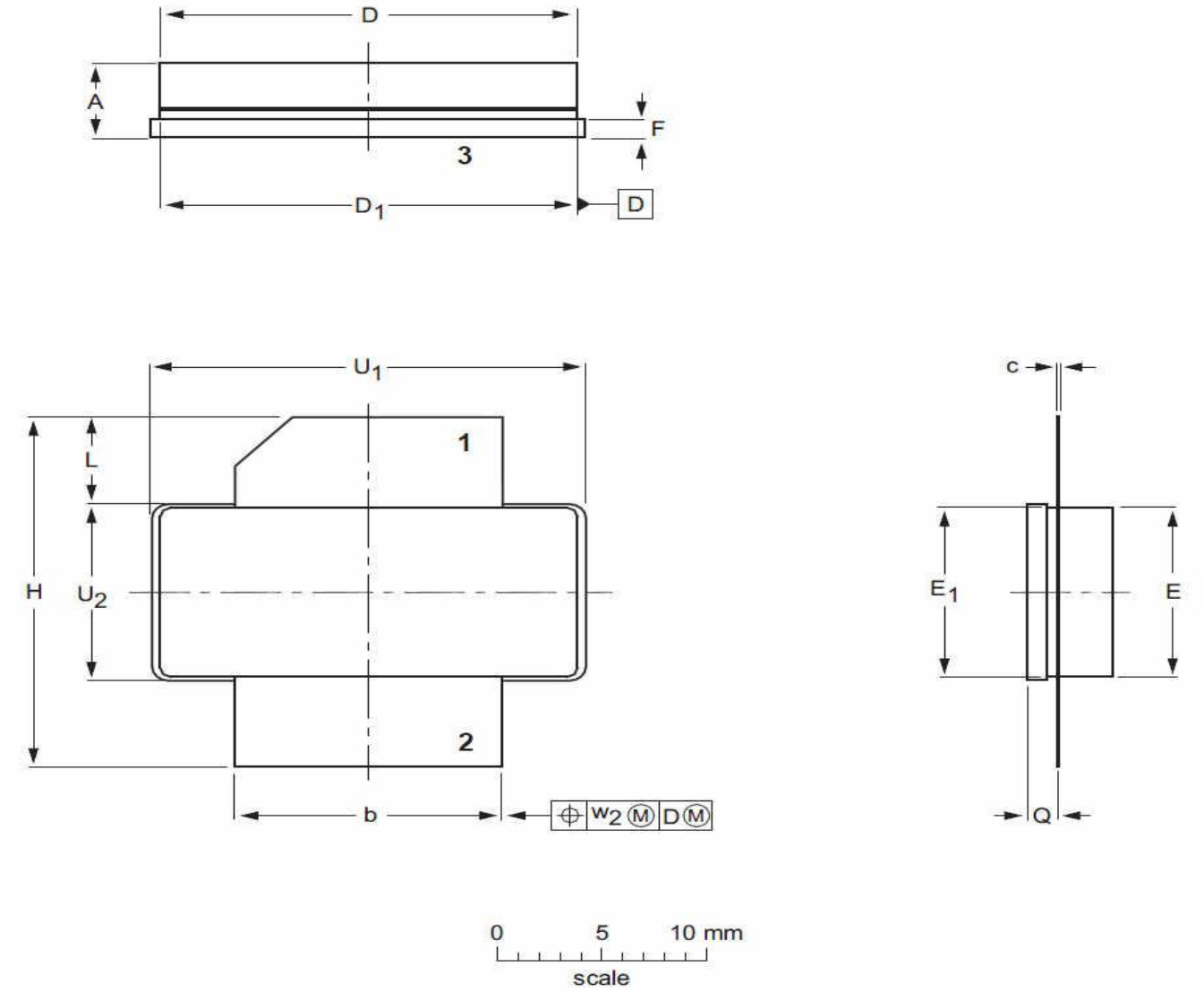
Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2014/06/17	Rev 1.0	Preliminary Datasheet
2016/03/07	Rev 2.0	Product Datasheet

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