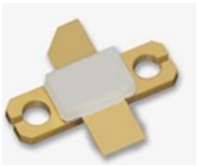
80W, 28V High Power RF LDMOS FETs

Description

The ITCH09080GX is a 80-watt, unmatched LDMOS FETs, designed for Wide-band and Mobile radio applications with frequencies from HF to 1500MHz. It can be used in Class AB/B and Class C for all typical modulation formats.

ITCH09080GX



•Typical Class AB Performance (On Innogration fixture with device soldered):

VDD = 28 Volts,Vgs=3.02V, IDQ = 450 mA, Pulse CW, Pulse Width =20us, Duty Cycle =10%.

Frequency	Gain (dB)	P_{-1dB} (W)	η_D@P_{-1} (%)	P_{-3dB} (W)	η_D@P_{-3} (%)
880MHz	20	80	52	120	61

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negativ for Improved Class C Oper
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.76	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	70	——		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA

Gate Threshold Voltage (V_{DS} = 28V, I_D = 300 μA)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 450 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V

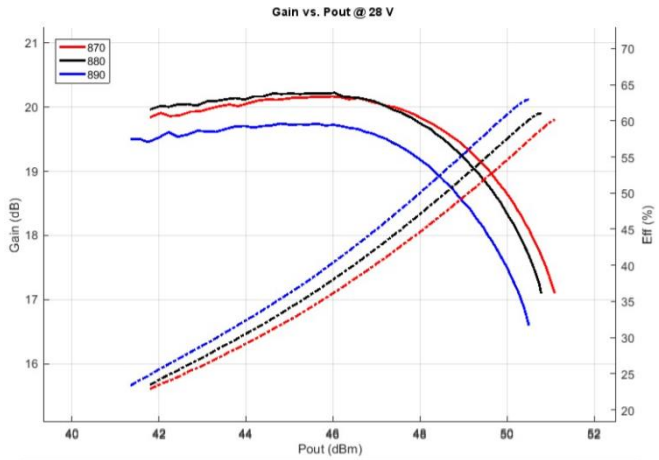
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 450mA, f = 880 MHz, Pulse Width =20us, Duty Cycle =10%..

Power Gain	Gp	——	19	——	dB
Drain Efficiency@P3dB	η_D	——	52	——	%
3 dB Compression Point	P_{-1dB}	——	80	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 450 mA, f = 870 MHz

VSWR 10:1 at 80W pulse CW Output Power	No Device Degradation

Figure 1: Pulsed CW performance (VDS = 28 Volts, Vgs=3.02V, IDQ = 450 mA, Pulse CW, Pulse Width =20us, Duty Cycle =10%.)



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
870	49.39	86.85	51.41	19.15	51.09	128.44	60.17
880	48.98	79.14	52.16	19.22	50.78	119.64	61.07
890	48.80	75.83	54.29	18.68	50.50	112.08	62.93

Figure 2:Network Analyzer Results（S11，S21）(VDS=28V, Idq=800mA)

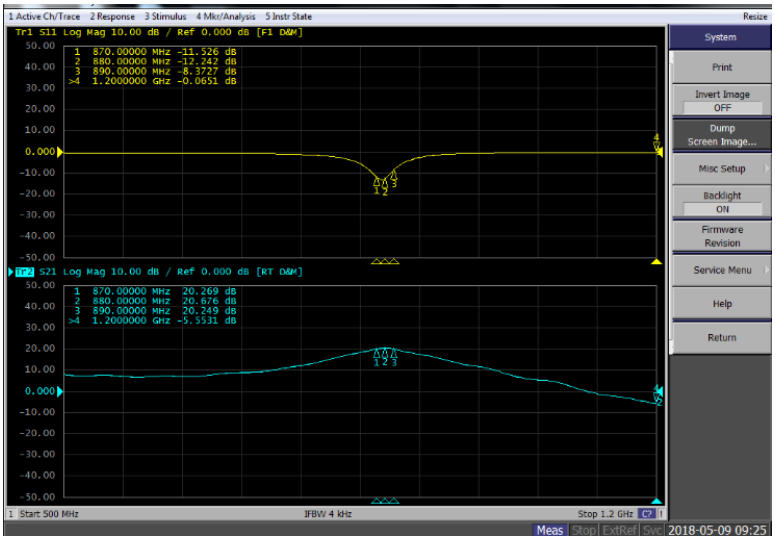
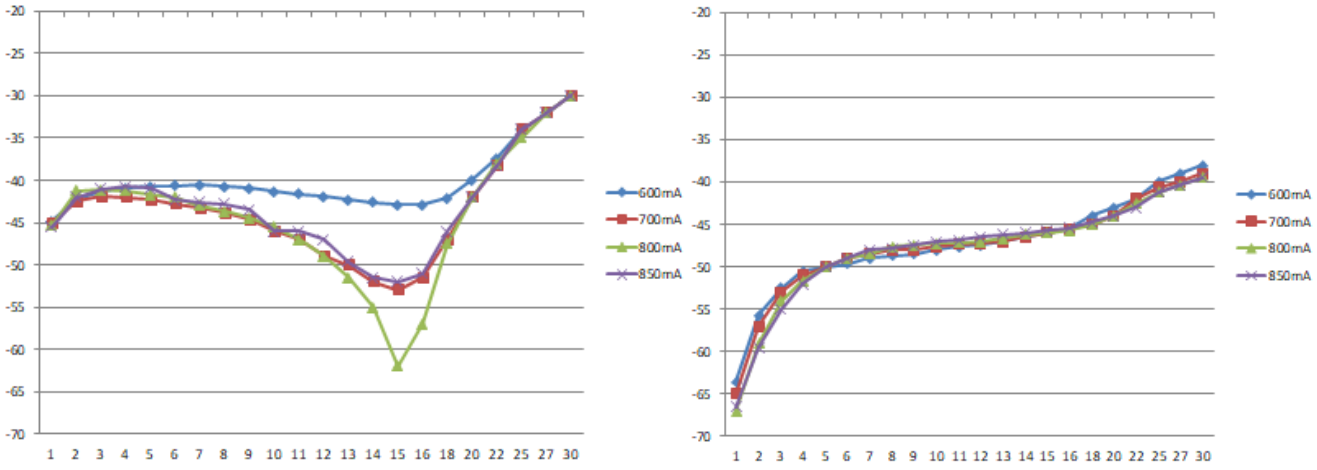


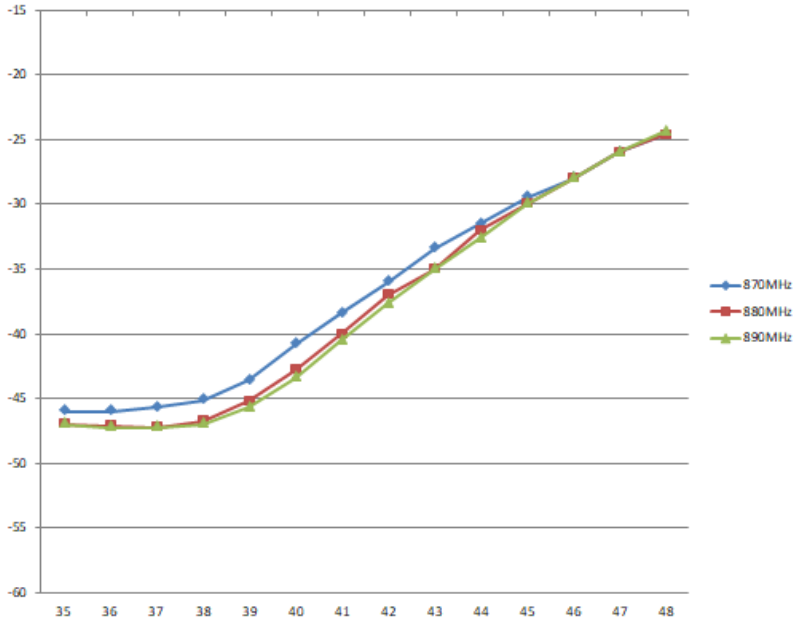
Figure 3: IM3 &IM5 as function of Idq (VDS=28V, f=880MHz，Two-Tone, Carrier Spacing=500kHz)



IM3(dBc) VS 2 tones average power(W）

IM5(dBc） VS 2 tones average power(W）

Figure 4: WCDMA ACPR performance (VDS=28V, Idq=800mA, Single Carrier W-CDMA, PAR=10.8Db@0.01% Probability on CCDF.)



ACPR（dBc） VS Pout（dBm）

Figure 5: Photo of 880MHz application circuit

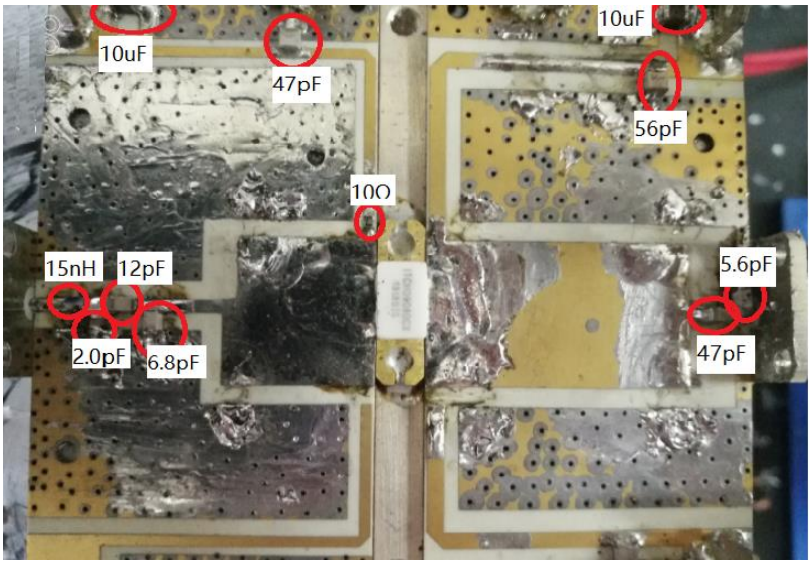
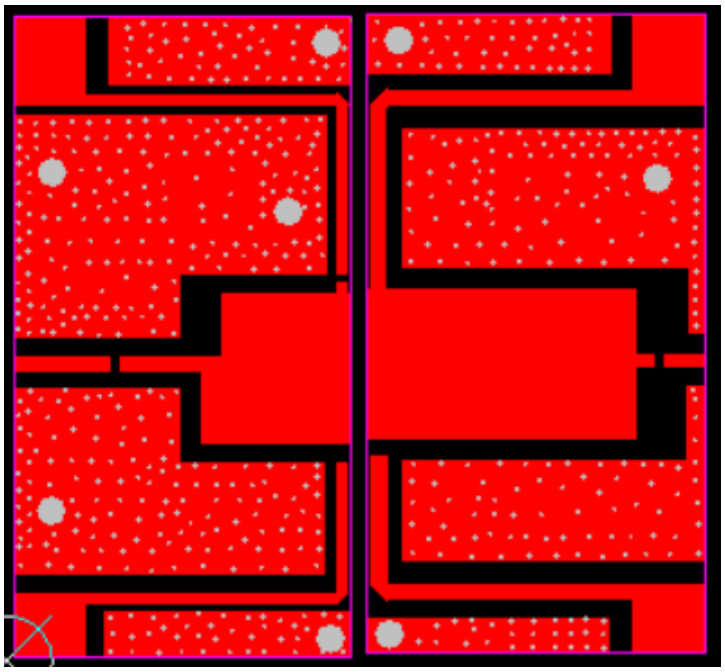
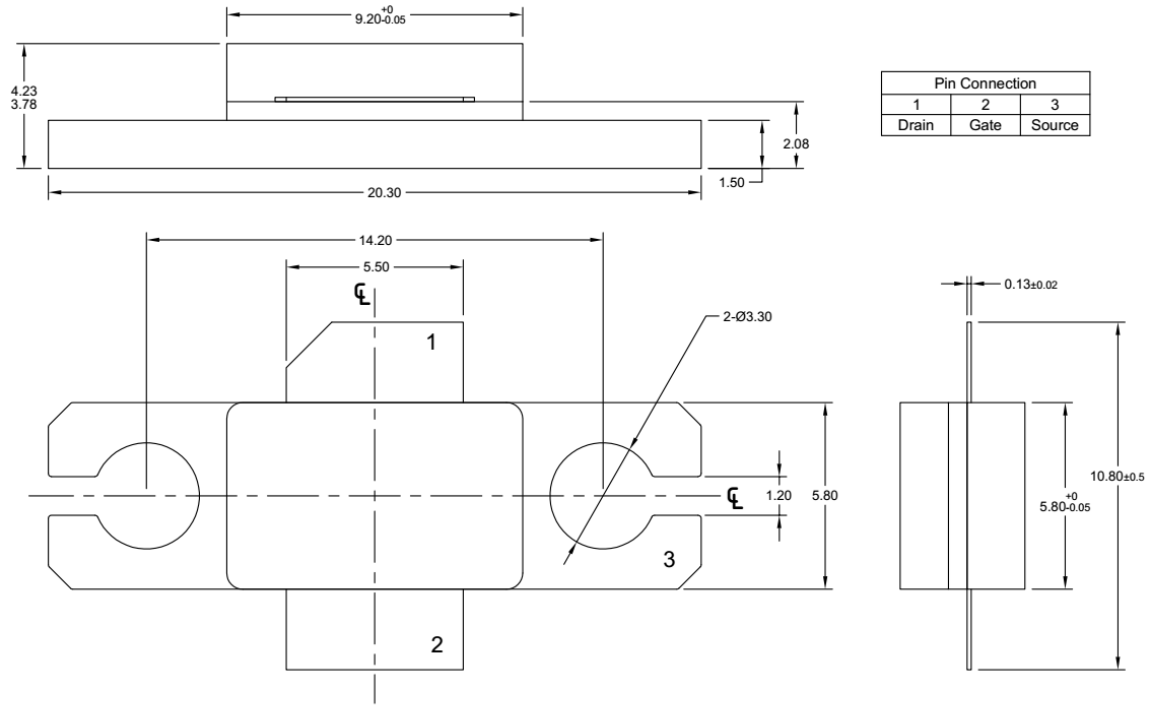


Figure 6 PCB:RO4350 30Mil (Layout gerber file upon request):



Package Outline

Flanged ceramic package; 2 leads



Pin Connection		
1	2	3
Drain	Gate	Source

Unit: mm
Tolerances(unless specified): x.x ±0.1
x.xx ±0.05

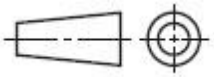
OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/5/10	**Rev 1.0**	**Product Datasheet**

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