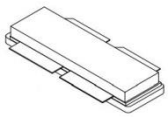
1300-1500MHz, 400W, High Power RF LDMOS FETs

ITCH15401D4



Description

ITCH15401D4 is a 400-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies from 1300-1500MHz

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- Typical Performance (on Innogration 1.3GHz narrow band fixture with device soldered): Vdd=28V, Vgs=2.57V, Idq=400mA,Tc=25 degree C, Test signal: CW,

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	Id(A)	Gp(dB)	Eff
1300	37.7	56.3	430	24.5	18.6	63%

Features

- Low cost, high reliable solution.
- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase= 85°C, Tj= 200°C, DC Power supply	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	——	——	V
Zero Gate Voltage Drain Leakage Current	I_{DSS}	——	——	10	μA

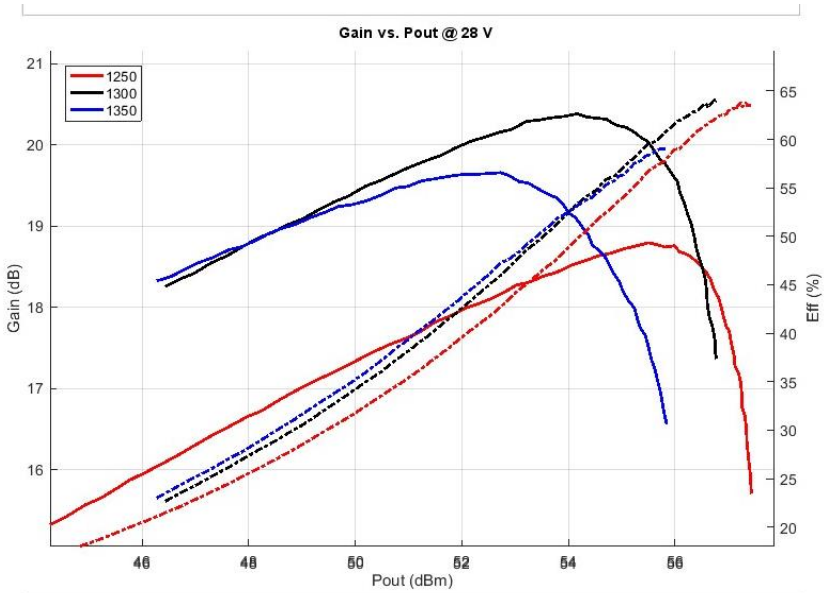
(V_{DS} = 28 V, V_{GS} = 0 V)					
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_{DQ} = 400 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.57		V

Functional Tests (In Innogration 1.3GHz Test Fixture, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 400 mA, f = 1300 MHz, Pulse CW Signal Measurements. Pulse width:100uS,Duty cycle:10%, Pin=5W

Power Gain	Gp	——	18.6	——	dB
Drain Efficiency@Pout	η_D		63	——	%
Output Power	Pout	350	400	——	W
Input Return Loss	IRL	——	-7	——	dB

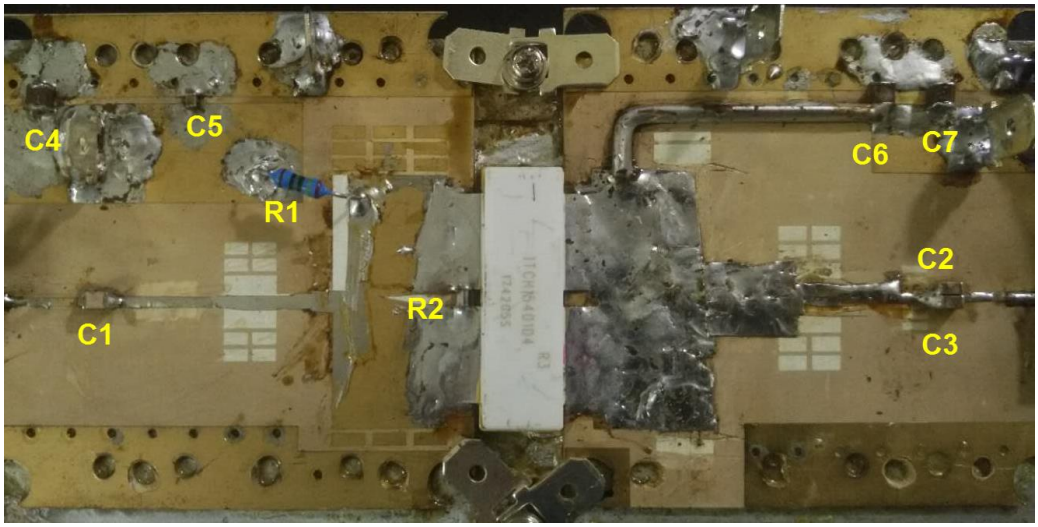
Figure 1: Gain and Efficiency as function of output power

Signal: Pulse width 100us, duty cycle 10% , Vgs= 2.57V,Vdd= 28V,Idq=400mA



Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1250	56.97	497.21	62.65	17.76	57.43	553.60	63.28
1300	56.16	412.93	62.20	19.31	56.78	476.10	63.89
1350	54.68	293.77	55.24	18.63	55.85	384.15	59.15

Figure 2: Test fixture photo, layout and bill of materials

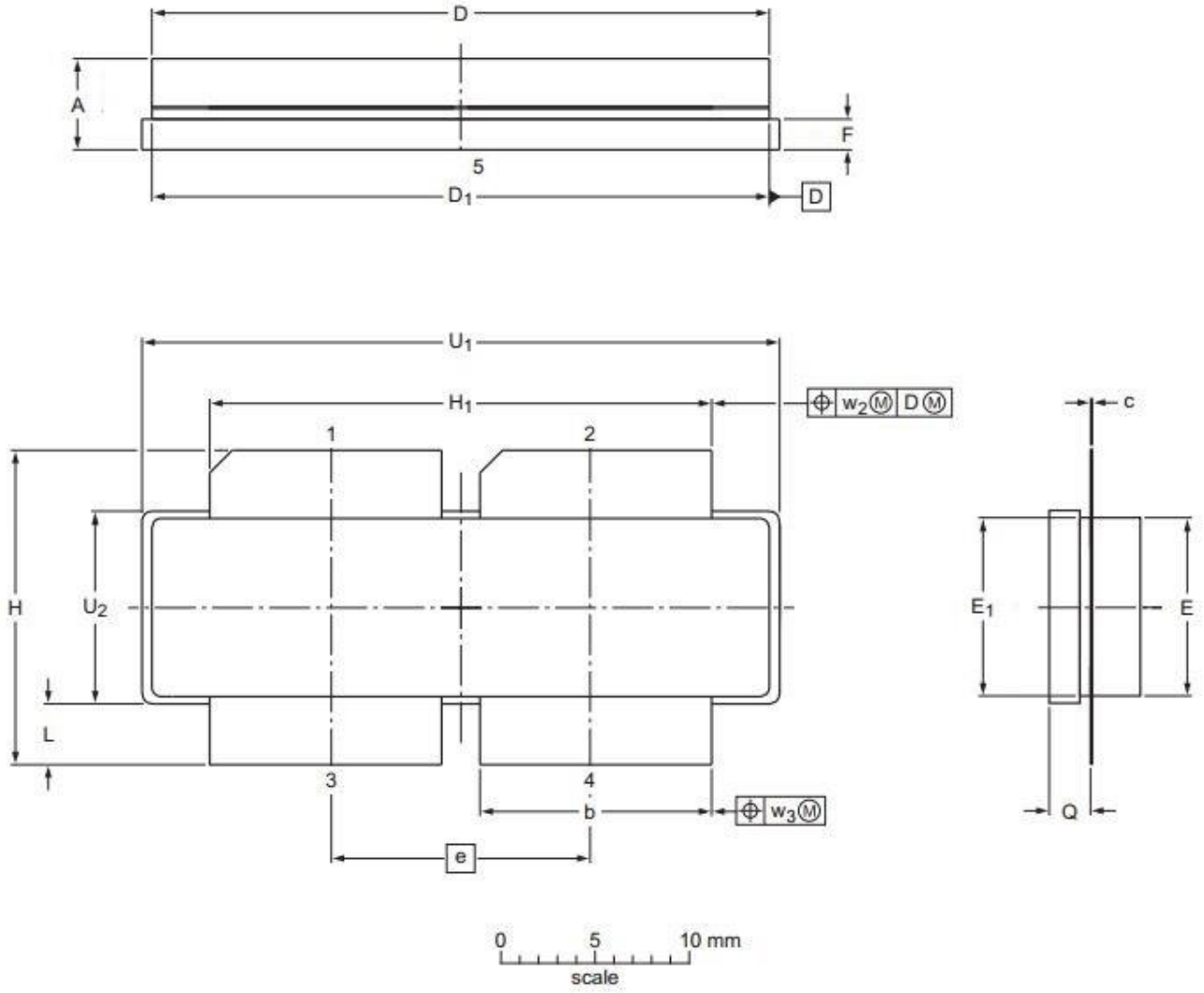


PCB: 30mil RO4360 (Dielectric Constant = 6.15)

C1, C5	ATC600F 33pF
C2, C3, C6	ATC800B 33pF
C4, C7	10uF
R1	47 Ω
R2	10 Ω

Package Outline

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/19	V1	Preliminary Datasheet Creation
2017/10/24	V2	1.3GHz performance modified according to internal drawing Rev 3

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