



1800MHz-2000MHz, 180W, 28V High Power RF LDMOS FETs

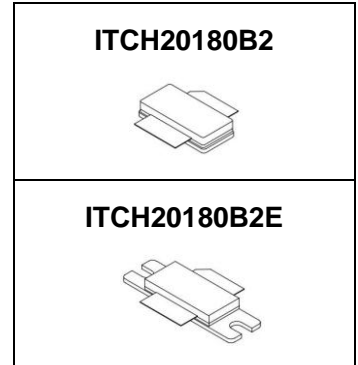
Description

The ITCH20180B2 is a 180-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 1800 to 2000 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

•Typical Performance (On Innogrations fixture with device soldered):

VDD = 28 Volts, IDQ = 780 mA, Pulse CW, Pulse Width=10 us, Duty cycle=12% .

Frequency	Gp (dB)	P _{-1dB} (dBm)	$\eta_D@P_{-1}$ (%)	P _{-3dB} (dBm)	$\eta_D@P_{-3}$ (%)
1805 MHz	18.2	52.0	50.8	53.4	55.9
1842.5 MHz	18.2	52.0	50.4	53.5	57.3
1880 MHz	17.3	51.8	49.2	53.4	56.2



•Typical Performance (On Innogrations fixture with device soldered): VDD = 28 Volts, IDQ = 1.37 A, Test signal: WCDMA, 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Frequency (MHz)	P _{L(AV)} (W)	Gp (dB)	η_D (%)	ACPR _{5M} (dBc)	ACPR _{10M} (dBc)
1805	10	18.6	15	-44.5	-61.6
1842.5	10	18.6	14	-46.3	-62.5
1880	10	17.8	14	-49.0	-63.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	70	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _C = 85°C, T _J =200°C, DC test	R _{θJC}	0.35	°C/W

Table 3. ESD Protection Characteristics



Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V _{GS} =0V; I _D =1mA)	V _{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}			10	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}			1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 600 uA)	V _{GS(th)}		1.8		V
Gate Quiescent Voltage (V _{DD} = 28 V, I _{DQ} = 800 mA, Measured in Functional Test)	V _{GS(Q)}	2.2	2.7	3.2	V

Functional Tests (In Innogrations demo, 50 ohm system) :V_{DD} = 28 Vdc, I_{DQ} = 780 mA, f = 1805 MHz, Pulse CW, Pulse Width=10 us, Duty cycle=12% .

Power Gain	G _p		18.2		dB
1 dB Compression Point	P _{-1dB}		52.0		dBm
3dB Compression Point	P _{-3dB}		53.4		dBm
Drain Efficiency@P3dB	η _D		55.9		%
Input Return Loss	IRL		-7		dB

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 800 mA, f = 1805 MHz

VSWR 10:1 at 180W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

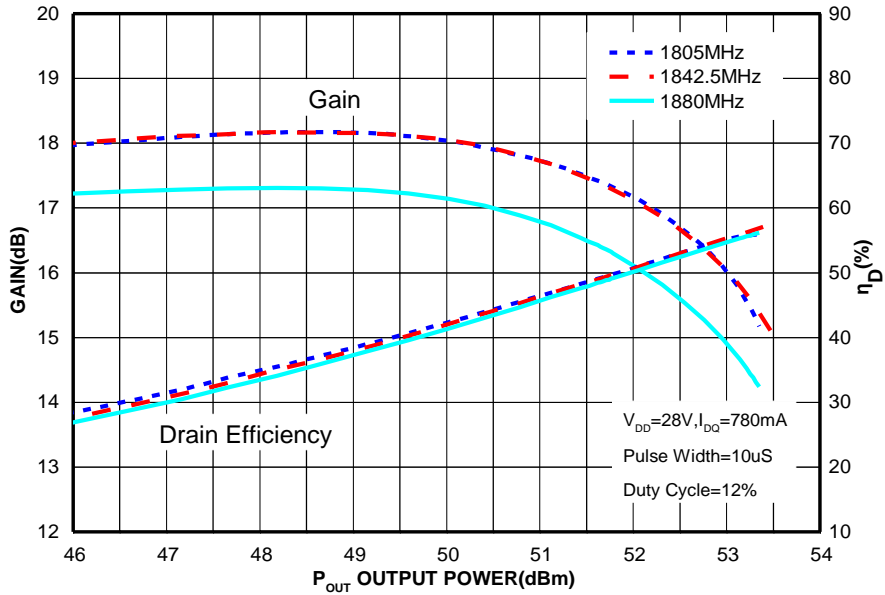


Figure 1. Power gain and drain efficiency as function of Pulse output power

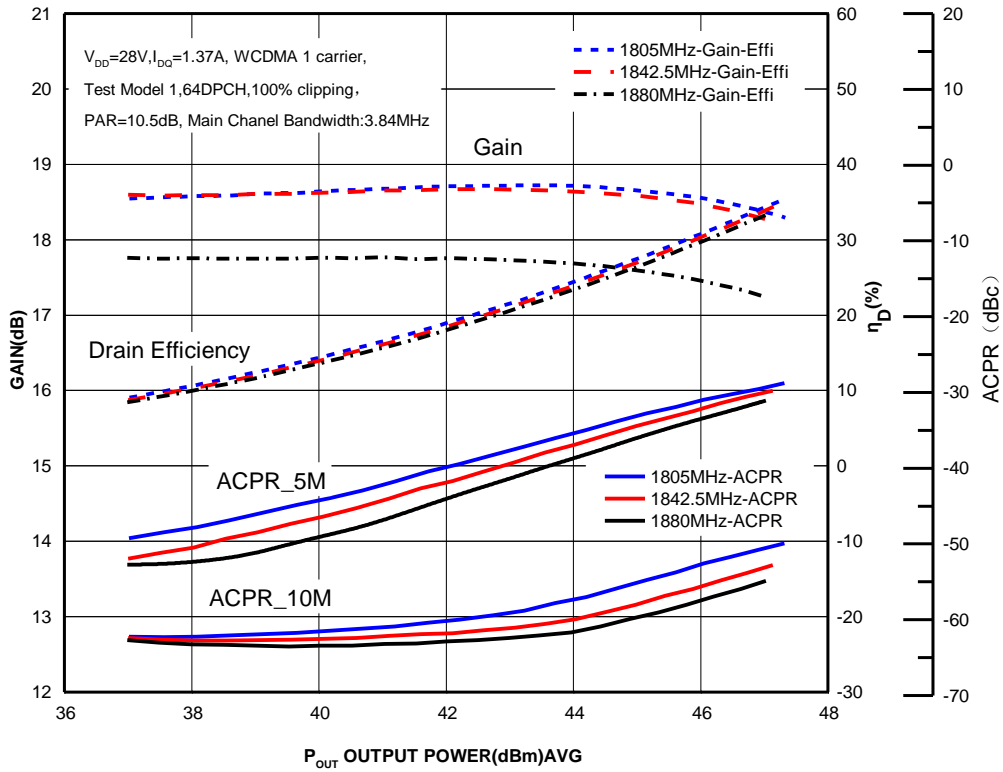
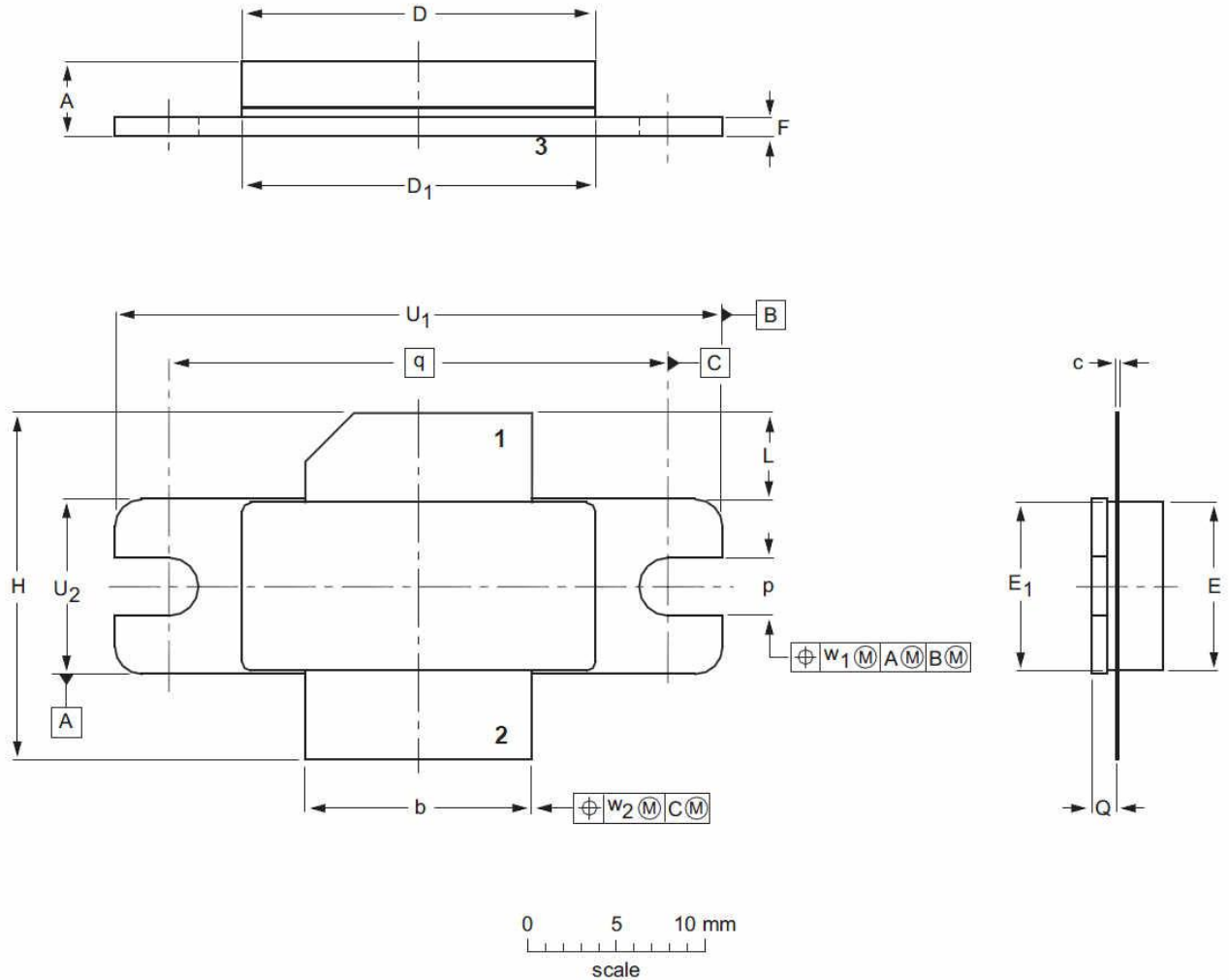


Figure 2. Single-Carrier WCDMA Power gain and drain efficiency and ACPR at 5 MHz and at 10 MHz as function of average output power



Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN、2—GATE、3—SOURCE)

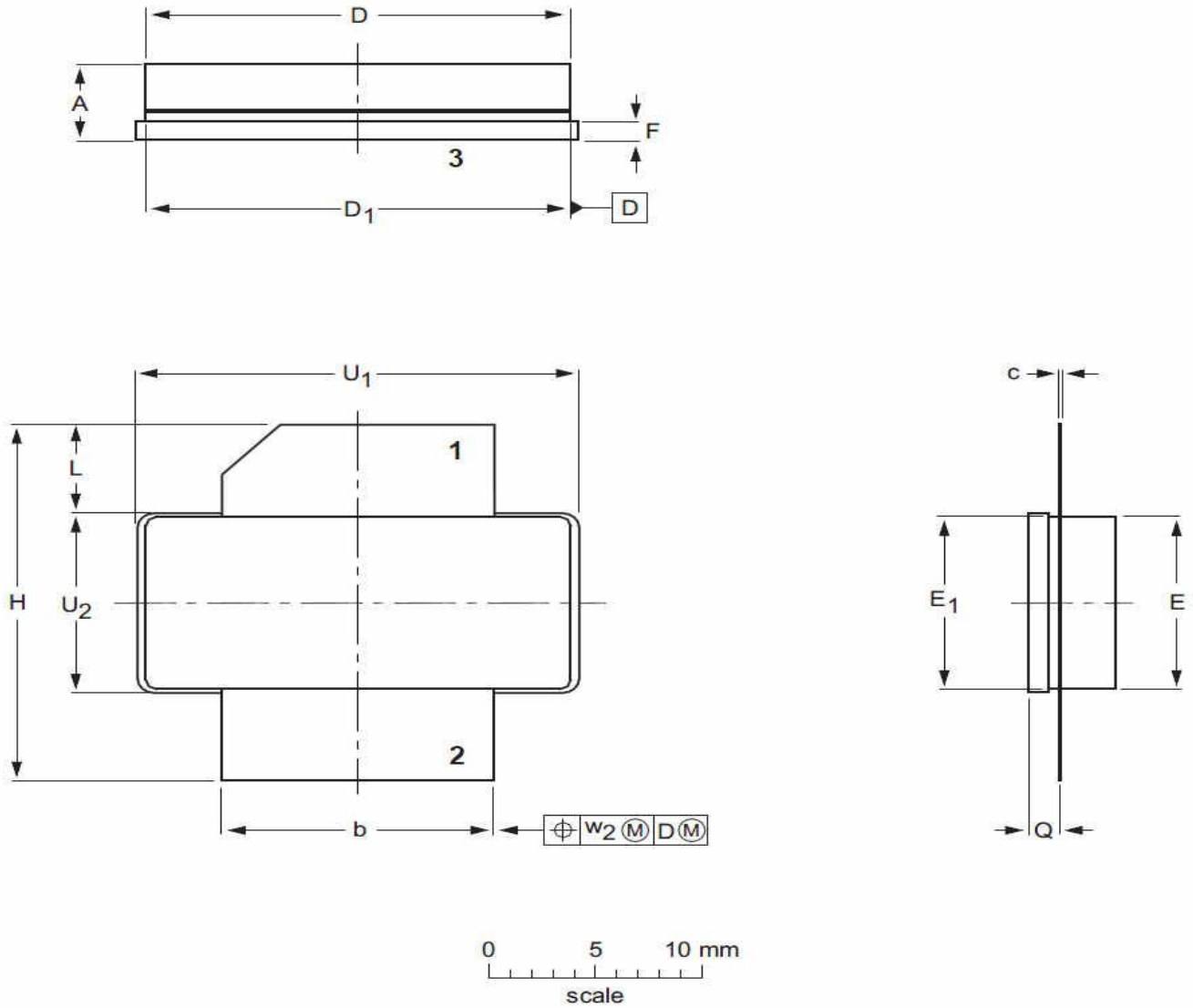


UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013



Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/03/27	Rev 1.0	Preliminary Datasheet

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