



2000MHz-2200MHz, 160W, 28V High Power RF LDMOS FETs

Description

The ITCH22160B4 is a 160-watt, internally matched LDMOS FET, designed for multicarrier WCDMA/PCS/DCS/LTE base station and ISM applications with frequencies from 2000 to 2200 MHz. It Can be used in Class AB/B and Class C for all typical cellular base station modulation formats.

•Typical Performance of Single Section (On Innegration fixture with device soldered):

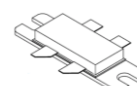
$V_{DD} = 28$ Volts, $I_{DQ} = 600$ mA, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Freq (MHz)	Gmax (dB)	P _{-1dB} (dBm)	P _{-3dB} (dBm)	$\eta_D@P_{-3}$ (%)
2110	17.4	49.1	49.9	54.4
2140	17.6	48.7	49.6	54.6
2170	17.2	48.3	49.3	54.2

ITCH22160B4



ITCH22160B4E



•Typical Performance of Doherty Circuit (On Innegration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQMAIN} = 500$ mA, $V_{GPEAK} = 0.9$ V, Pulse CW, Pulse Width=20 us, Duty cycle=10% .

Freq (MHz)	Gmax (dB)	P _{-1dB} (dBm)	P _{-3dB} (dBm)	$\eta_D@P_{-3}$ (%)
2110	14.9	50.6	52.8	59.2
2140	15.0	51.3	52.9	59.7
2170	14.9	51.8	52.7	59.0

•Typical Single-Carrier W-CDMA Performance of Doherty Circuit (On Test Fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQMAIN} = 600$ mA, $V_{GPEAK} = 0.9$ V, $P_{out} = 45$ dBm Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 10.5 dB @ 0.01% Probability on CCDF.

Freq (MHz)	P _{OUT} (dBm)	Gp (dB)	η_D (%)	ACPR _{5M} (dBc)
2110	45	14.5	45.8	-27.1
2140	45	14.6	45.3	-29.0
2170	45	14.7	43.9	-31.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc



Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^{\circ}\text{C}$, $T_J = 200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per Section)

Drain-Source Breakdown Voltage ($V_{GS} = 0\text{V}$; $I_D = 1\text{mA}$)	V_{DSS}	65	70		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}			10	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}			1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\text{ }\mu\text{A}$)	$V_{GS(th)}$		1.8		V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_{DQ} = 800\text{ mA}$, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	V

Functional Tests of per Section (On Innogrations doherty demo, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQMAIN} = 600\text{ mA}$, $f = 2170\text{ MHz}$, Pulse CW, Pulse Width=20 μs , Duty cycle=10%.

Power Gain (Maximum Gain)	G_p		17.2		dB
1 dB Compression Point	P_{-1dB}		48.3		dBm
3dB Compression Point	P_{-3dB}		49.3		dBm
Drain Efficiency@P3dB	η_D		54.2		%
Input Return Loss	IRL		-7		dB

Load Mismatch of per Section (On Innogrations Test Fixture, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 600\text{ mA}$, $f = 2170\text{ MHz}$

VSWR 10:1 at 80W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

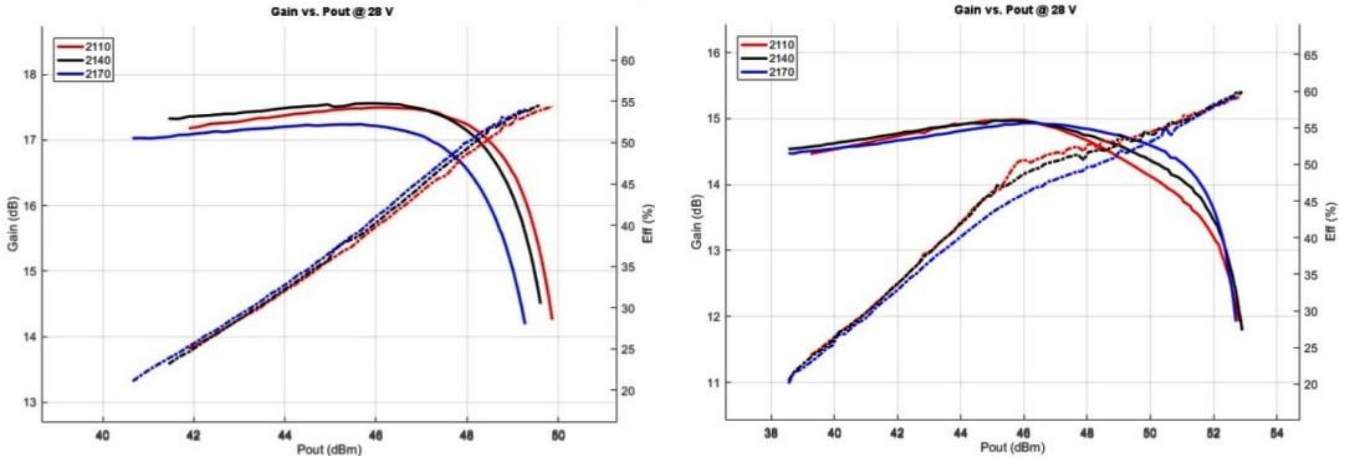


Figure 1. Power gain and drain efficiency as function of
Pulse output power (Single Section)

Power gain and drain efficiency as function of
Pulse output power (Doherty Circuit)

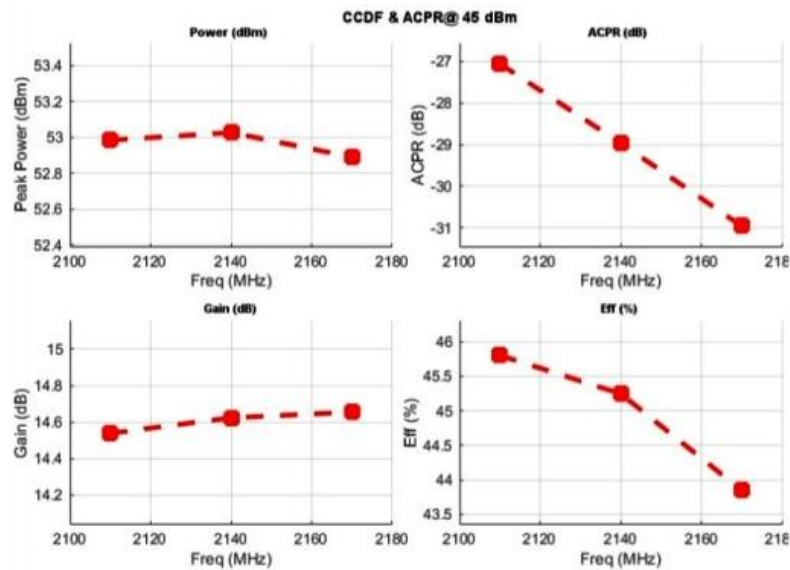
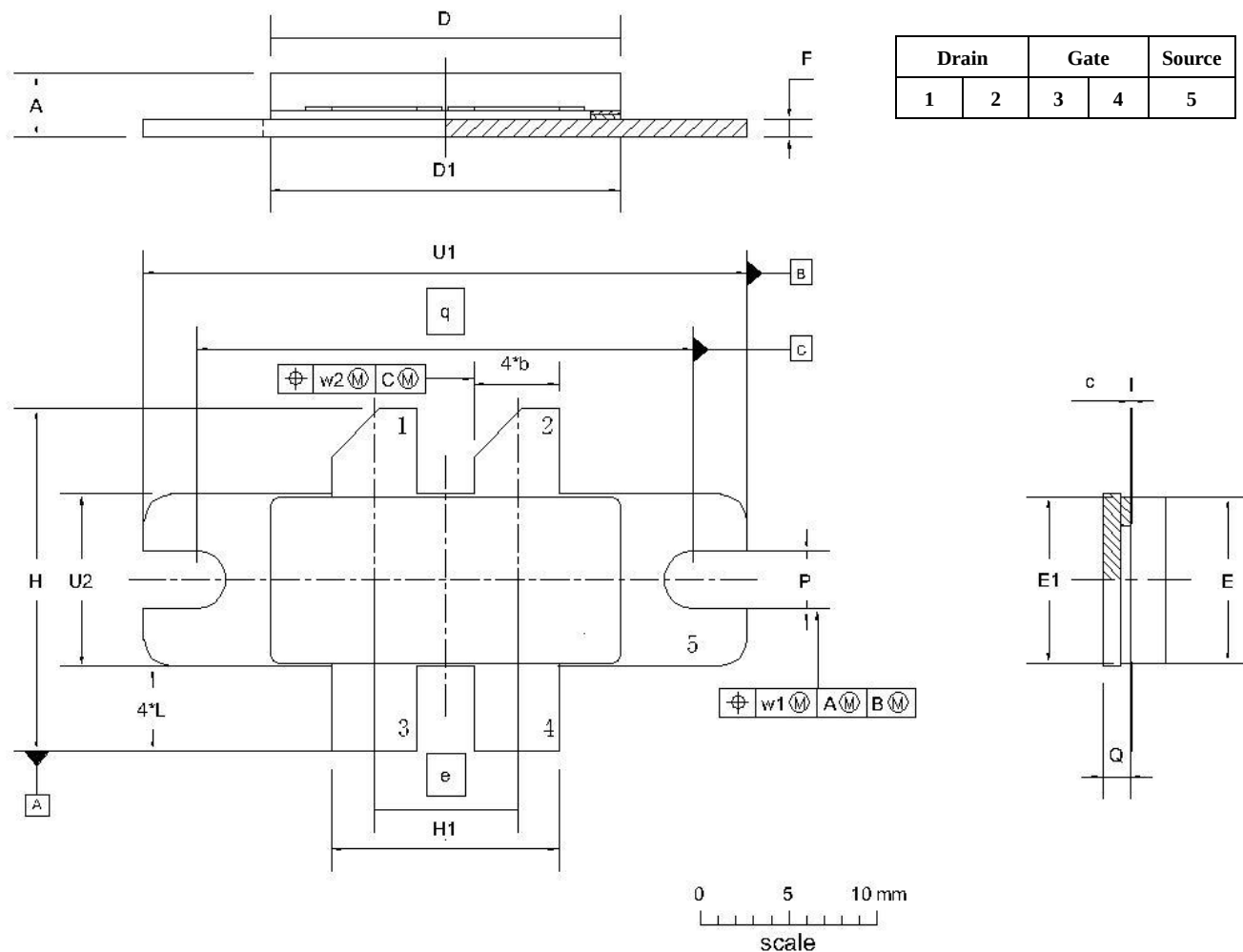


Figure 3. Single-Carrier WCDMA CCDF and ACPR_{5MHz} @ 30W
as function frequency (Doherty Circuit)



Package Outline

Eared Flanged Ceramic Package; 2 mounting holes; 4 leads



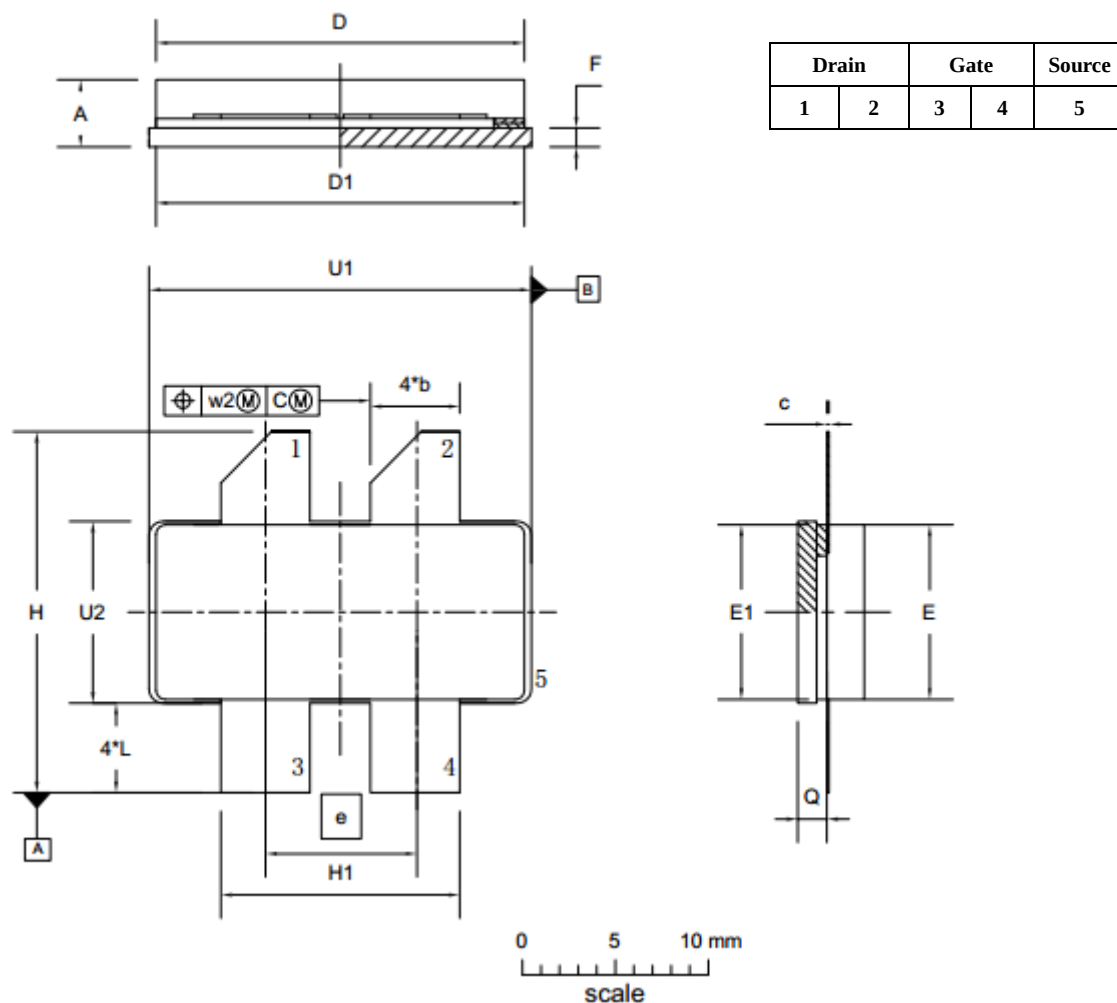
Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	p	Q	q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4E					03/12/2013



Earless Flanged Ceramic Package; 4 leads



UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	L	Q	U ₁	U ₂	W ₁	W ₂
mm	4.72	4.67	0.15	20.02	19.96	7.90	9.50	9.53	1.14	19.94	12.98	5.33	1.70	20.70	9.91	0.25	0.51
	3.43	4.93	0.08	19.61	19.66		9.30	9.25	0.89	18.92	12.73	4.32	1.45	20.45	9.65		
inches	0.186	0.194	0.006	0.788	0.786	0.311	0.374	0.375	0.045	0.785	0.511	0.210	0.067	0.815	0.390	0.01	0.02
	0.135	0.184	0.003	0.772	0.774		0.366	0.364	0.035	0.745	0.501	0.170	0.057	0.805	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/09/08	Rev 1.0	Preliminary Datasheet

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