



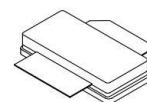
2400-2500MHz, 180W, High Power RF LDMOS FETs

Description

The ITCH25180B2 is a 180-watt, internally matched LDMOS FETs, designed for Multiple use especially RF Energy application including cooking, heating and medical with frequencies from 2400 to 2500 MHz.

It is qualified up to 32V operation.

ITCH25180B2



- Typical Performance (on Innogrator fixture with device soldered):

CW signal, Tcase = 25 degree C, frequency 2450MHz

Vdd(V)	Vgs(V)	Idq(mA)	Pin(dBm)	Pout(dBm)	Pout(W)	Gain(dB)	IDS(A)	Eff(%)
28	2.27	20	39.8	52.3	170	12.5	10.5	58%
32	2.26	20	39.3	53	200	13.6	11	56%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase= 85°C, Tj= 200°C, DC Power supply	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Breakdown Voltage ($V_{GS}=0V$; $I_D=100\mu A$)	V_{DSS}	65	——	——	V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28V$, $V_{GS} = 0V$)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current ($V_{GS} = 6V$, $V_{DS} = 0V$)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage ($V_{DS} = 28V$, $I_D = 600\mu A$)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage ($V_{DD} = 32V$, $I_{DQ} = 20mA$, Measured in Functional Test)	$V_{GS(Q)}$		2.25		V

Functional Tests (In Innegration Test Fixture, 50 ohm system) : $V_{DD} = 32Vdc$, $I_{DQ} = 20mA$, $f = 2450MHz$, CW Signal Measurements.,
 $P_{in}=10W$,

Power Gain	G_p	13	13.6	——	dB
Drain Efficiency@P3dB	η_D		56	——	%
3dB Compression Point	P_{-3dB}	180	200	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innegration Test Fixture, 50 ohm system): $V_{DD} = 32Vdc$, $I_{DQ} = 20mA$, $f = 2450MHz$

VSWR 10:1 at 180W pulse CW Output Power	No Device Degradation
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Figure 1

Signal: Pulse width 100us, duty cycle 10% ,
Vgs= 2.26V,Vdd= 28V,I_{dq}=20mA

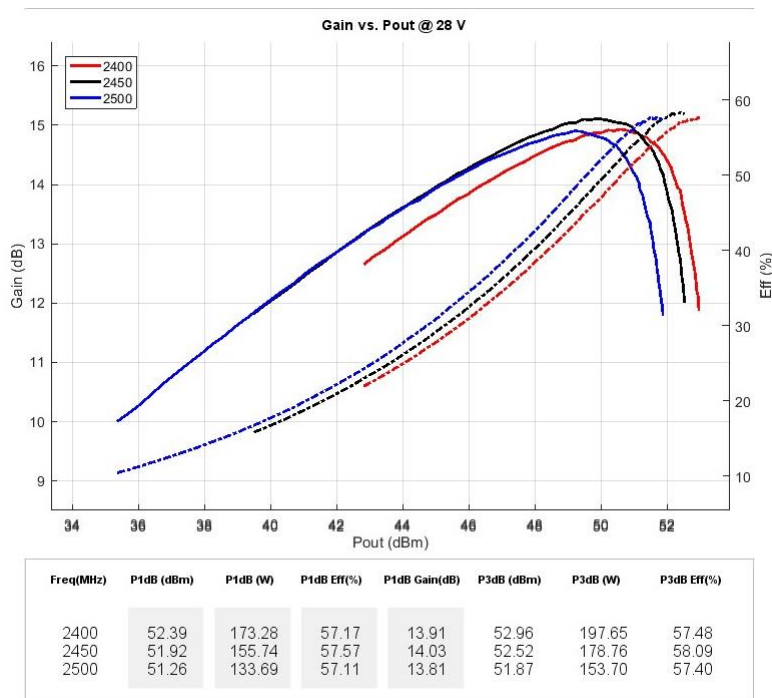




Figure 2

Signal: Pulse width 100us, duty cycle 10%

Vgs= 2.25V,Vds= 32V,Idq=50mA

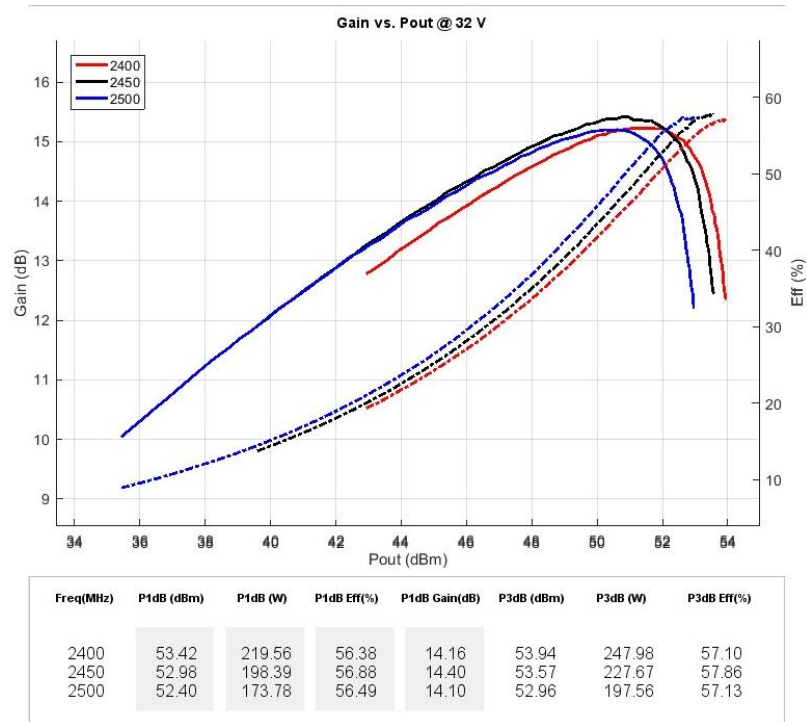


Figure3: Fixture circuit photo

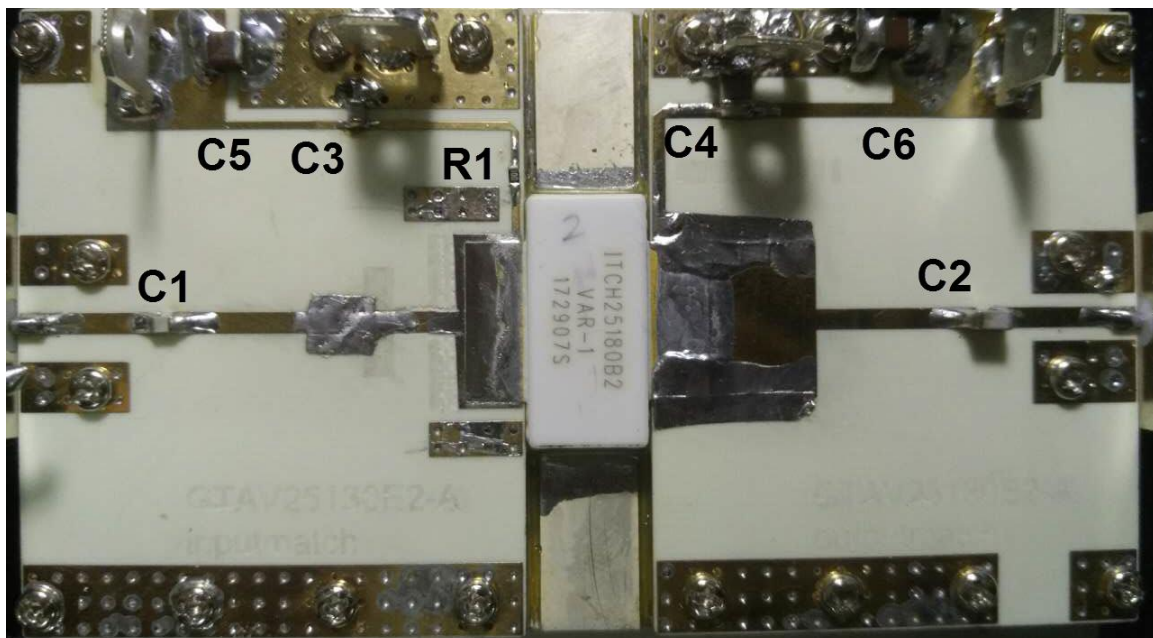


Figure 3: Layout picture (original Gerber file upon request)

Board material: Ro 4350B, Er = 3.48, thickness 20 mils, 1oz copper, unit mm ,

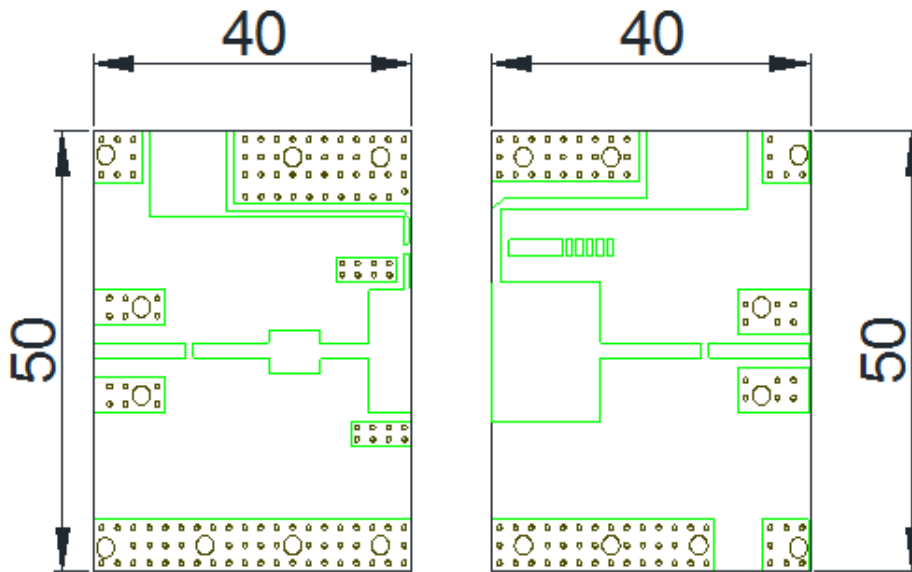


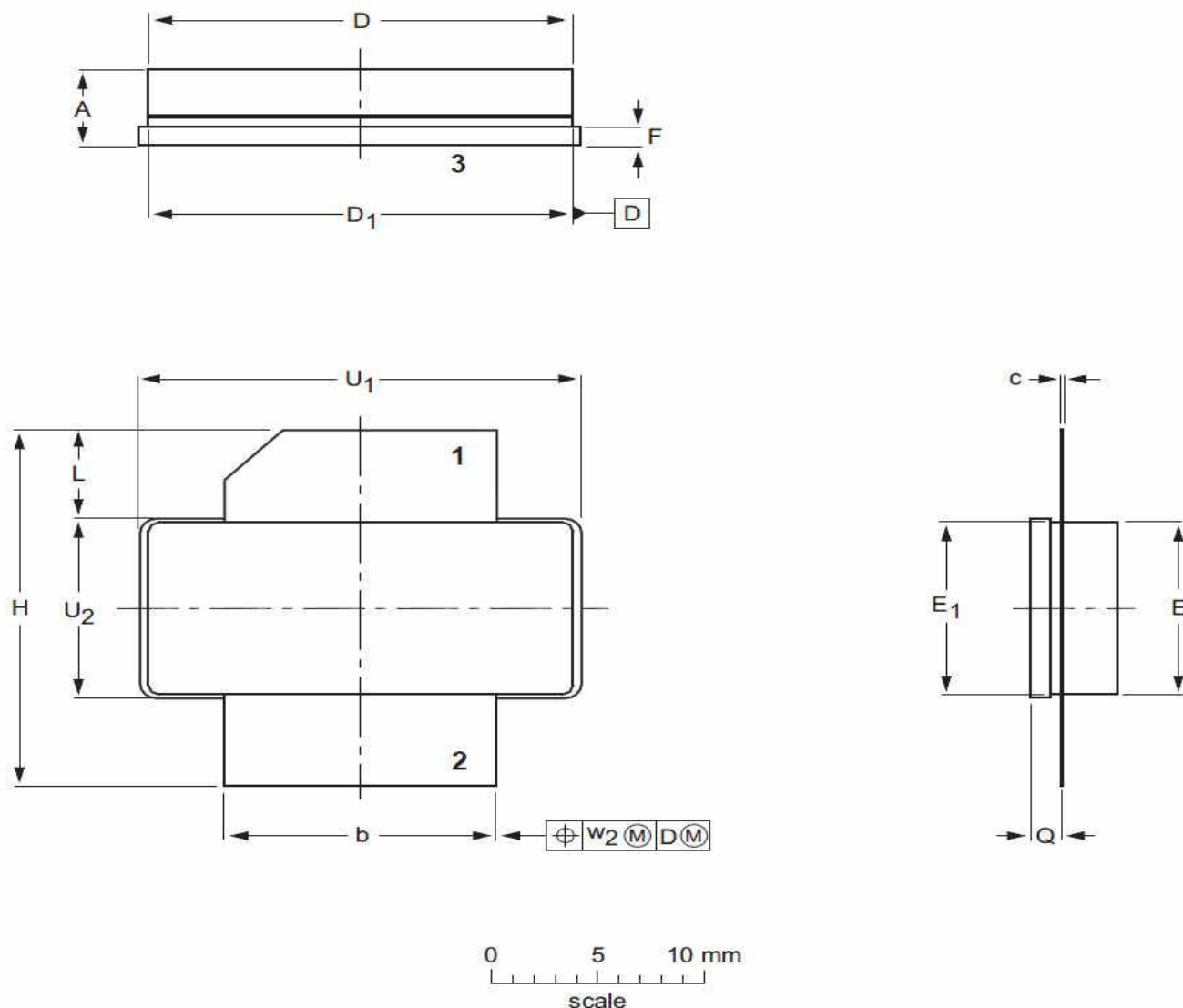
Table 5. List of components

C1, C3	ATC600F 20pF
C2, C4	ATC800B 22pF
C5, C6	10uF
R1	10 Ohm



Package Outline

Earless flanged ceramic package; 2 leads (1—DRAIN、2—GATE、3—SOURCE)



UNIT	A	b	c	D	D ₁	E	E ₁	F	H	L	Q	U ₁	U ₂	W ₂
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/3/31	V1	Preliminary Datasheet Creation
2017/7/14	V2	Modified test data
2017/8/10	V3	Modified test data

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