700MHz-2700MHz, 15W, 28V RF Power LDMOS FETs

Description

The ITCH27015E2 is a 15-watt, internally matched LDMOS FET, designed for cellular base station and ISM applications with frequencies from 700MHz to 2700 MHz

ITCH27015E2

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 100 mA，Pulse Width =10us, Duty Cycle =12%.

Frequency (MHz)	Gp (dB)	P_1dB (dBm)	η D (%)	P_3dB (dBm)	η D (%)
2620	19.8	42.5	56	43.5	59
2655	20	42	56	43.3	60
2690	19.9	41.6	55	42.9	61

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 100 mA，Pulse Width =50us, Duty Cycle =20%.

Frequency (MHz)	Gp (dB)	P_1dB (dBm)	η D (%)	P_3dB (dBm)	η D (%)
2400	19.4	43.0	57	44.0	61
2450	19.7	42.3	57	43.5	62
2500	19.9	41.7	57	42.8	61

Highlight: The fixture is used same board different BOM.

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=0V; I_{DS}=100uA	V_{DSS}	65			V
Zero Gate Voltage Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}			1	μA
Gate--Source Leakage Current	V_{GS} = 9 V, V_{DS} = 0 V	I_{GSS}			1	μA
Gate Threshold Voltage	V_{DS} = 28V, I_D = 300 μA	V_{GS}(th)		1.75		V
Gate Quiescent Voltage	V_{DS} = 28 V, I_{DS} = 100 mA, Measured in Functional Test	$V_{GS(Q)}$		2.65		V

Pulse CW Signal performance (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} =100 mA, f = 2690 MHz, Pulse CW, Pulse Width =10us, Duty Cycle =12%.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	Gp		19.9		dB
Drain Efficiency@P3dB	η_D		61		%
3dB Compression Point	P_{-3dB}		42.9		dBm
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 2690 MHz

VSWR 10:1 at 15W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

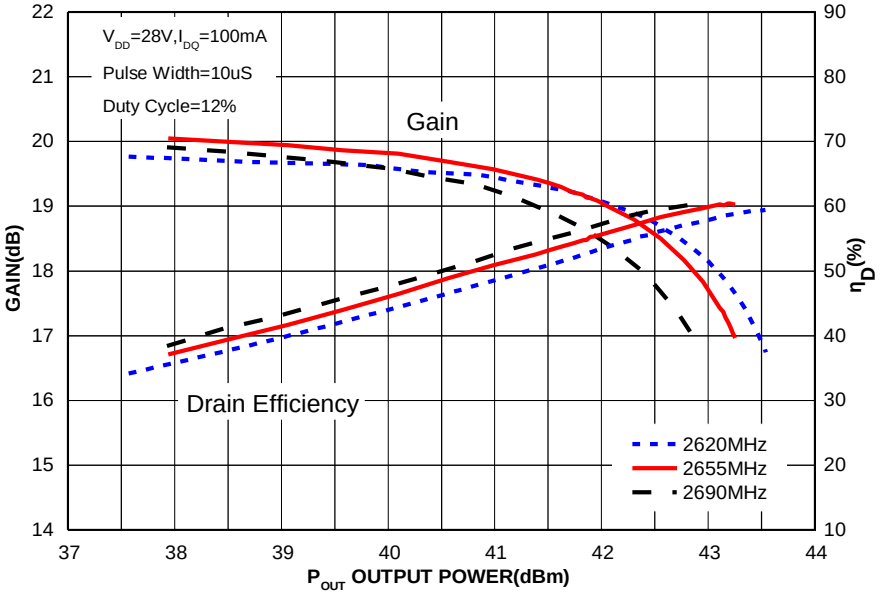


Figure 1. Power gain and drain efficiency as function of Pulse output power（2620-2690MHz）

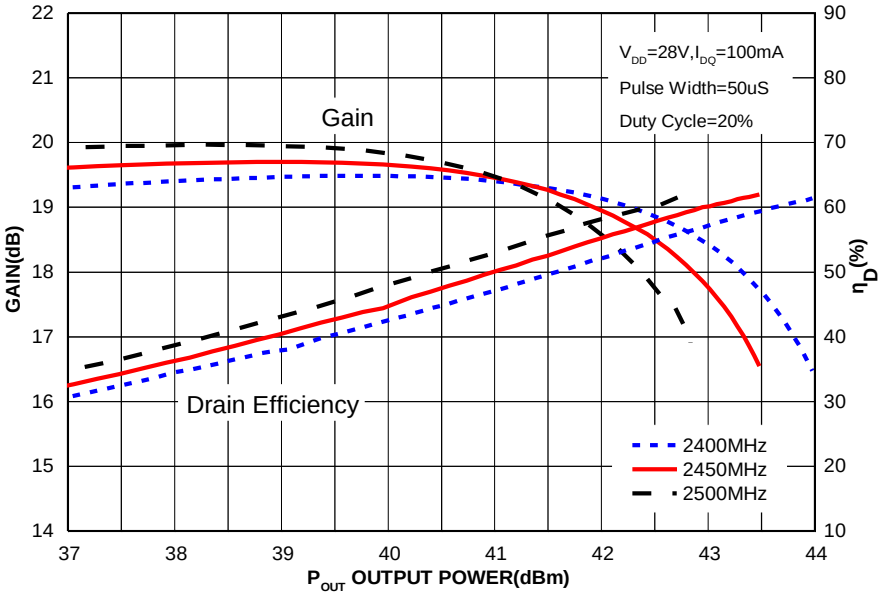
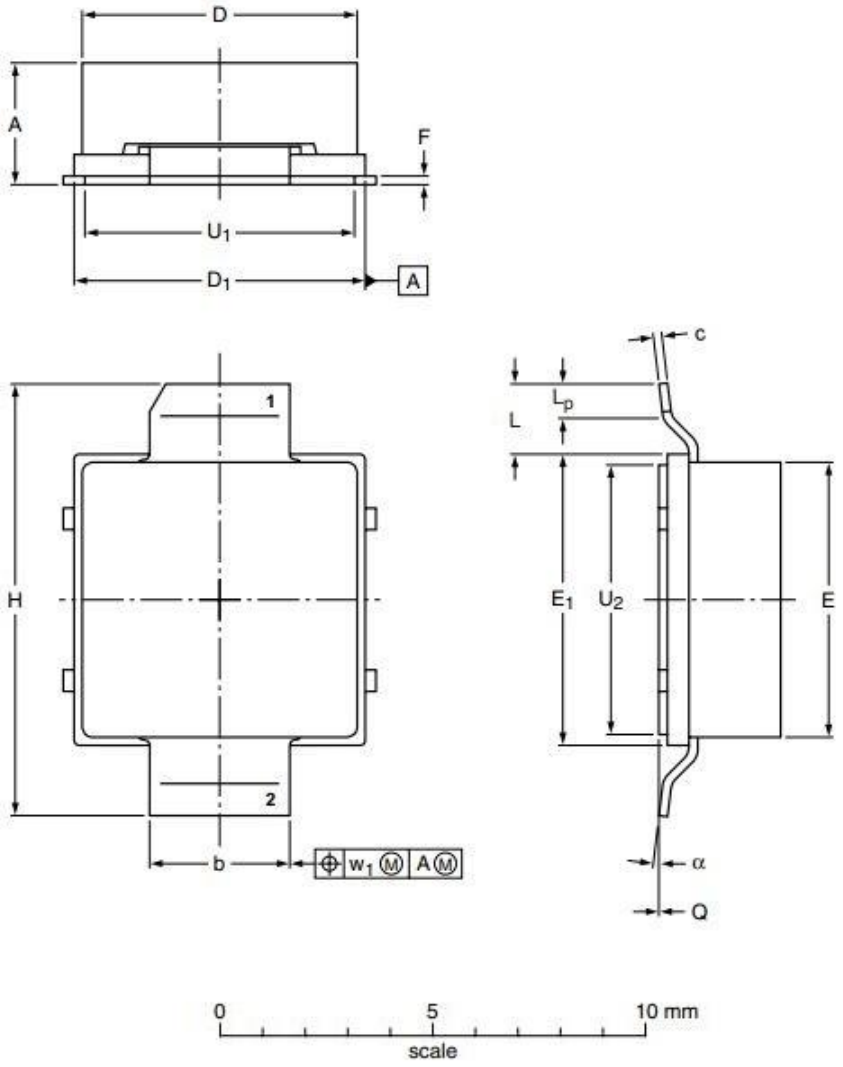


Figure 2. Power gain and drain efficiency as function of Pulse output power（2400-2500MHz）

Package Outline

Earless Flanged ceramic package; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	L_P	Q	U_1	U_2	w_1	α
mm	3.63 3.05	3.38 3.23	0.23 0.18	6.55 6.40	6.93 6.78	6.55 6.40	6.93 6.78	0.23 0.18	10.29 10.03	1.65	1.02 0.51	+0.05 −0.05	6.43 6.27	6.43 6.27	0.51	7° 0°
inches	0.143 0.120	0.133 0.127	0.009 0.007	0.258 0.252	0.273 0.267	0.258 0.252	0.273 0.267	0.009 0.007	0.405 0.395	0.065	0.040 0.020	+0.002 −0.002	0.253 0.247	0.253 0.247	0.02	7° 0°

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-E-A						10/22/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/02/06	Rev 1.0	Preliminary Datasheet
2017/03/16	Rev 2.0	Preliminary Datasheet

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