3400-3600MHz, 40W, 28V RF LDMOS FETs

ITCH36040A2

Description

The ITCH36040A2 is a 40-watt, internally-matched LDMOS FETs, designed for cellular application with frequencies from 3400 to 3600MHz. It can biased at class AB or Class C for linear or pulse application as well

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 28 Volts, I_{DQ} = 380 mA

Test signal: Pulsed CW, pulse width: 100Us, Duty cycle: 10%

Freq(MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
3400	45.67	36.93	44.80	12.85	46.38	43.43	45.17
3500	46.11	40.86	44.95	13.39	46.90	48.93	46.12
3600	45.68	37.01	44.07	13.53	46.46	44.29	45.09

Test signal: WCDMA_1C, (PAR=10.5dB @ 0.01% probability)

Freq(MHz)	Pout(dBm)	CCDF(dB)	Ppeak(dBm)	Ppeak(W)	ACPR(dBc)	Gain(dB)	Efficiency(%)
3400	38.02	8.39	46.41	43.75	-37.73	13.95	23.54
3500	37.99	8.70	46.70	46.73	-39.24	14.36	22.21
3600	38.00	8.46	46.47	44.36	-37.46	14.52	22.75

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65V, V_{GS} = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 300 μA)	$V_{GS}(th)$		1.75		V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 380 mA, Measured in Functional Test)	$V_{GS(Q)}$	1.8	2.8	3.8	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 380 mA, f =3500 MHz, Pulsed CW Signal Measurements.

Pulse width: 100uS,duty cycle: 10%

Power Gain	Gp		13		dB
1 dB Compression Point	P_{-1dB}		40		W
Drain Efficiency@P1dB	η_D	43	45		%
Input Return Loss	IRL		-10		dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 380 mA, f = 3500 MHz

VSWR 10:1 at 8W WCDMA Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1. Power gain and drain efficiency as function of average load power

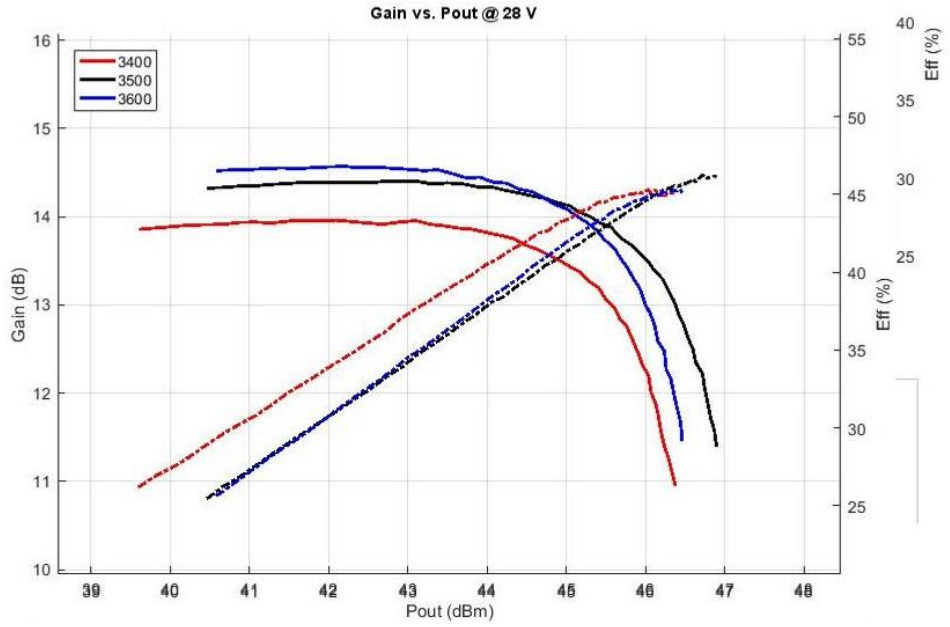


Figure 2. Network analyzer plots (S11/S21)

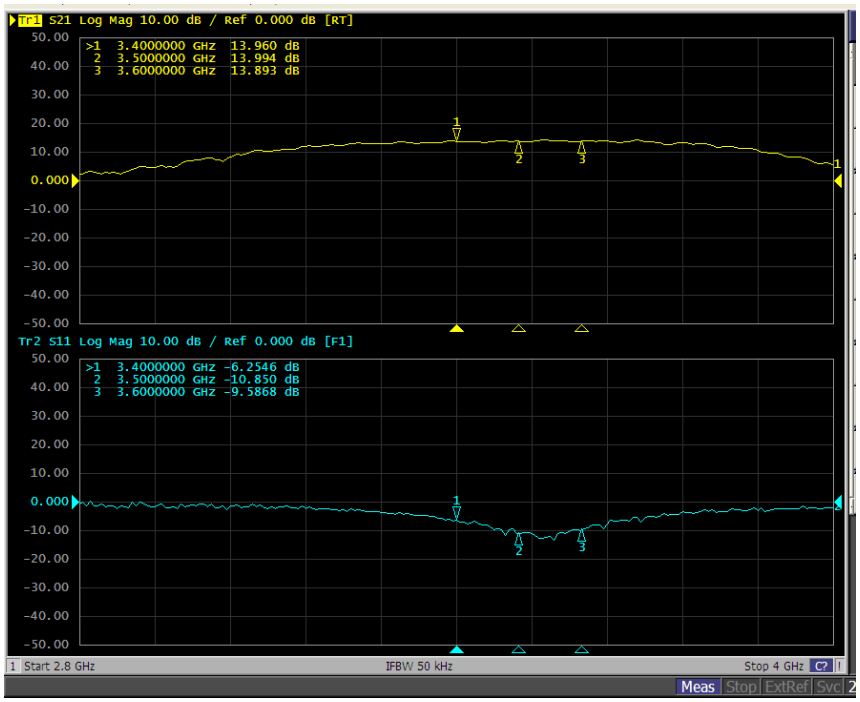
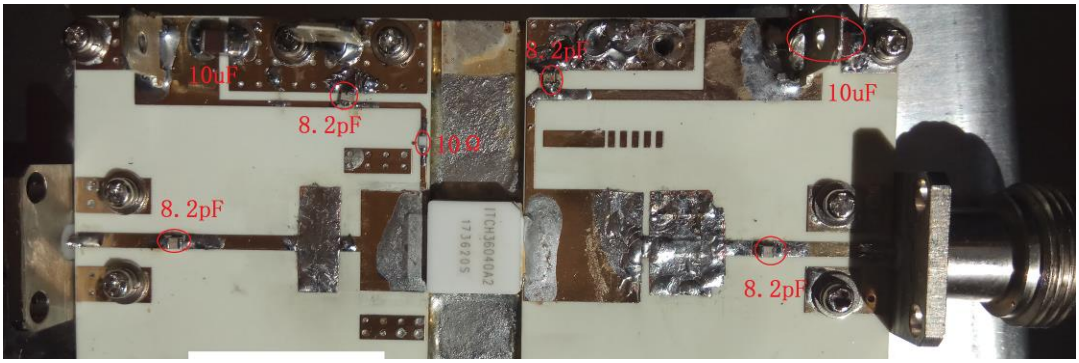
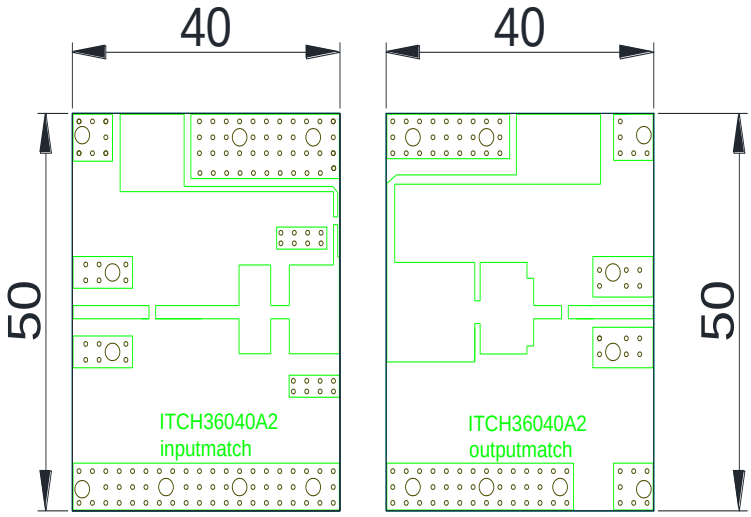


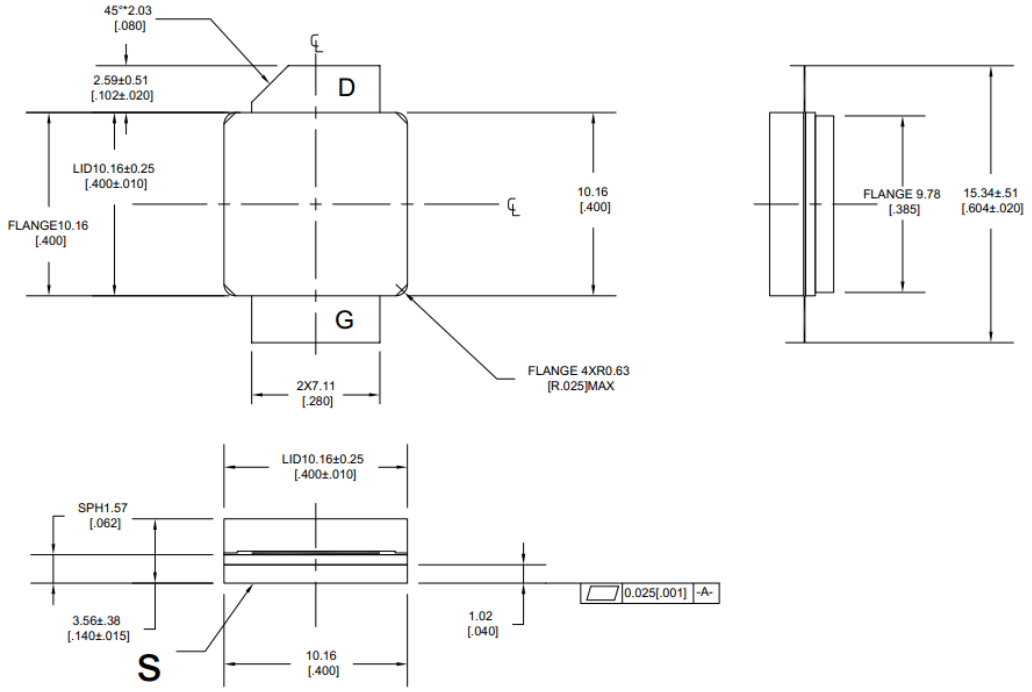
Figure 3. Photo of test fixture and BOM and layout





Package Outline

Earless Flanged ceramic package; 2 leads (A2)



Unit：mm [inch]

Tolerance .xx +/- 0.01 .xxx +/- 0.005 inches

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/9/14	Rev 1.0	Preliminary Datasheet Creation

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