ITD03N90A

N-Channel MOSFET

Lead Free Package and Finish

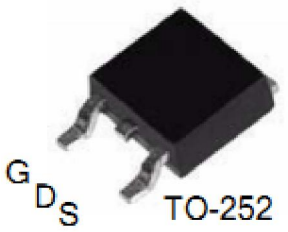
Applications:

- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D
900V	4.7Ω	3A

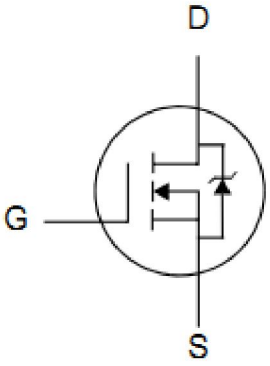
Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



TO-252

Packages
Not to Scale



Ordering Information

PART NUMBER	PACKAGE	BRAND
ITD03N90A	TO-252	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	ITD03N90A	Units
V_{DSS}	Drain-to-Source Voltage	900	V
I_D	Continuous Drain Current	3	A
I_{DM}	Pulsed Drain Current, V_{GS}@10V	12	A
P_D	Power Dissipation	75	W
	Derating Factor above 25℃	0.6	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy (NOTE *2)	125	mJ
E_{AR}	Avalanche Energy ,Repetitive (NOTE *1)	12	mJ
I_{AR}	Avalanche Current (NOTE *1)	1.5	A
dv/dt	Peak Diode Recovery dv/dt(NOTE *3)	5.0	V/ns
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	-55 to150	

Thermal Resistance

Symbol	Parameter	Typ.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	1.67	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	100		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	900	--	--	V℃	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V_{DS}=900V, V_{GS}=0V T_J=25℃
		--	--	250		V_{DS}=720V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -30V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance(NOTE *3)	--	4.7	5.5	Ω	V_{GS}=10V, I_D=1.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	V_{DS}=V_{GS},I_D=250μA
g_{fs}	Forward Transconductance(NOTE *3)	--	5	--	S	V_{DS}=15V, I_D=3A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	525	--	pF	V_{GS}= 0V,V_{DS} = 25V f =1.0MHz
C_{oss}	Output Capacitance	--	50	--		
C_{rss}	Reverse Transfer Capacitance	--	5	--		
Q_g	Total Gate Charge	--	15	--	nC	I_D=3A,V_{DD}=450V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	2.5	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	6	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	11		ns	V_{DD}=450V, I_D=3A, V_G=10V R_G=25Ω
t_{rise}	Rise Time	--	14			
$t_{d(OFF)}$	Turn-Off Delay Time	--	44			
t_{fall}	Fall Time	--	26			

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	3	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	12	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_{SD}=3A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	140	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	530	--	nC	

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=10mH, I_D=4.9A, Start T_J=25℃

*3. I_{SD} =3A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve：

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

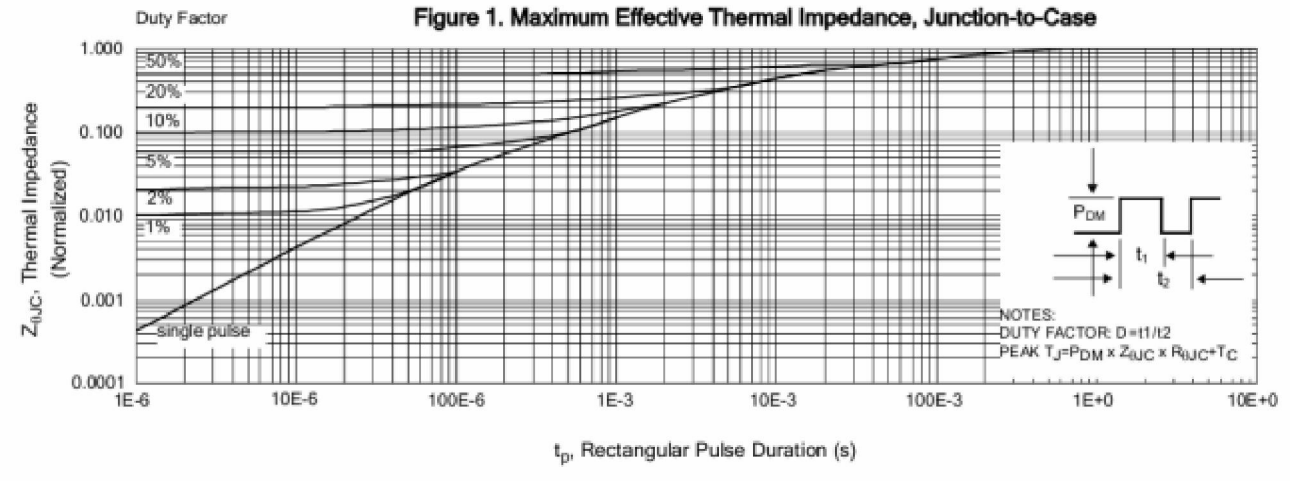


Figure 2. Maximum Power Dissipation vs Case Temperature

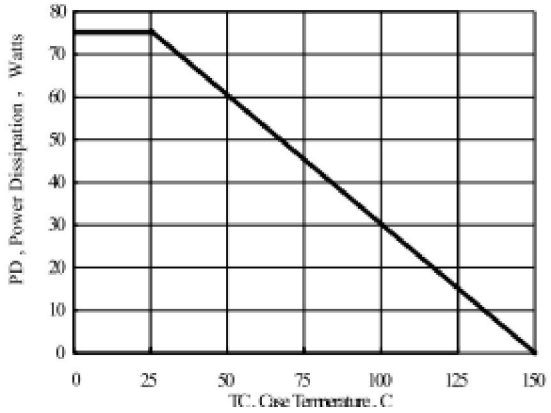


Figure 3. Maximum Continuous Drain Current vs Case Temperature

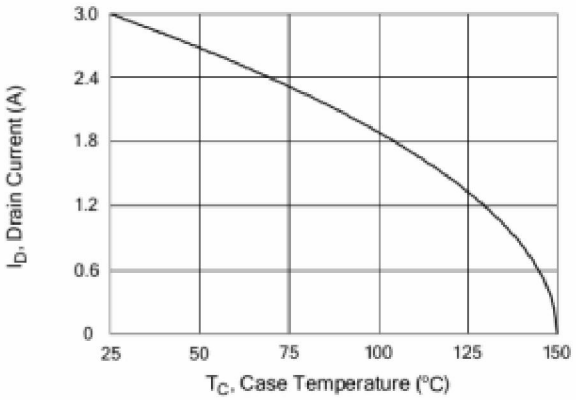


Figure 4. Typical Output Characteristics

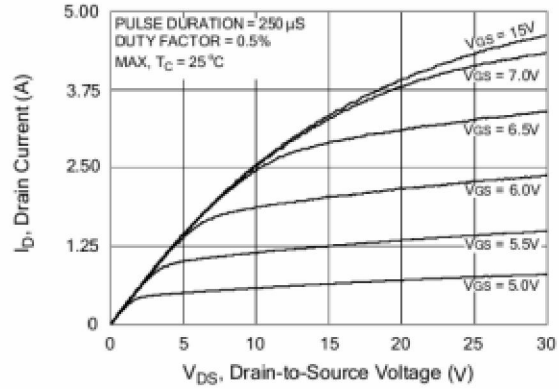


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

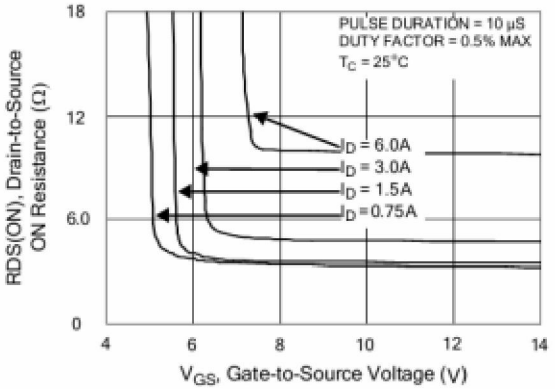


Figure 6. Maximum Peak Current Capability

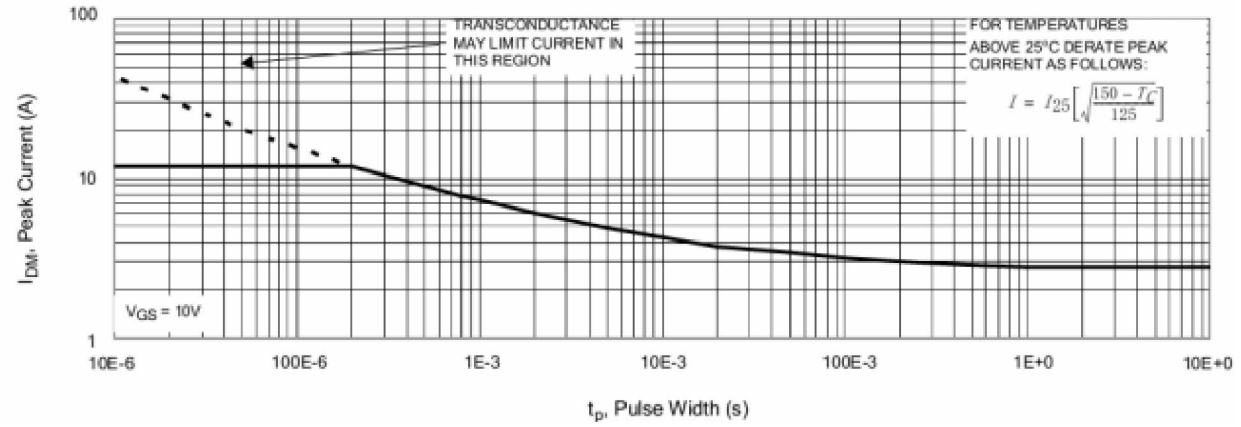


Figure 7. Typical Transfer Characteristics

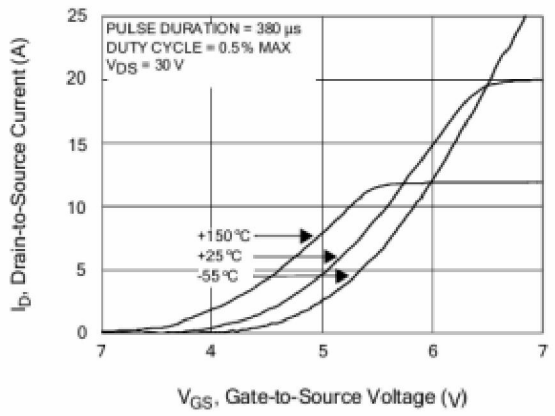


Figure 8. Unclamped Inductive Switching Capability

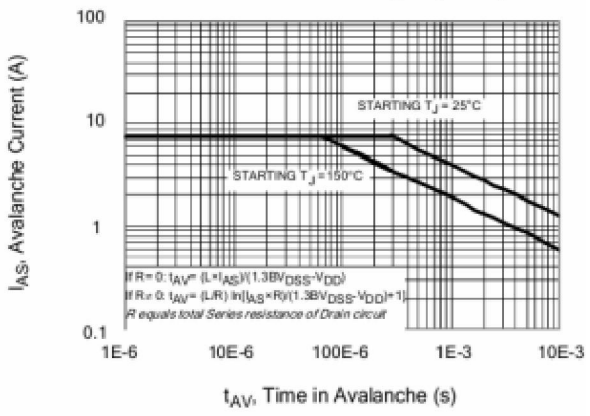


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

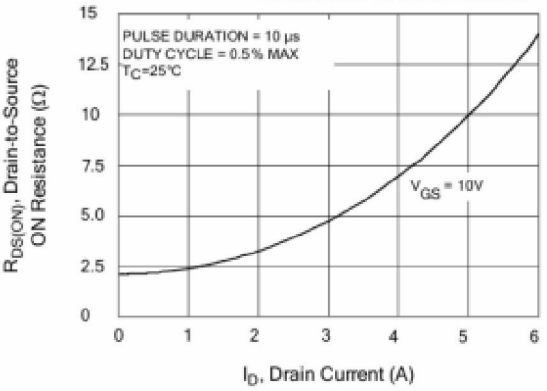


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

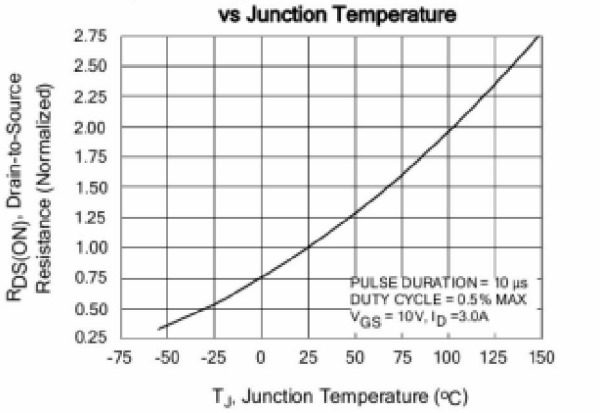


Figure 11. Typical Breakdown Voltage vs Junction Temperature

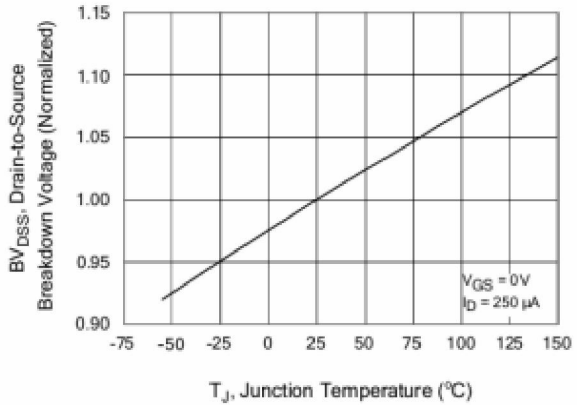


Figure 12. Typical Threshold Voltage vs Junction Temperature

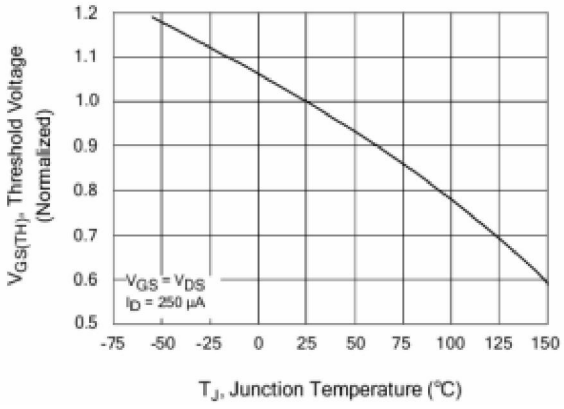


Figure 13. Maximum Forward Bias Safe Operating Area

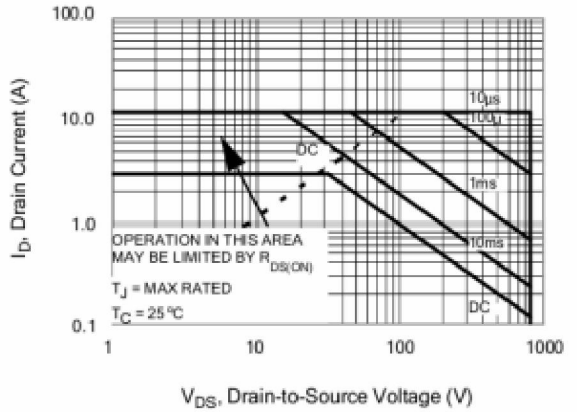


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

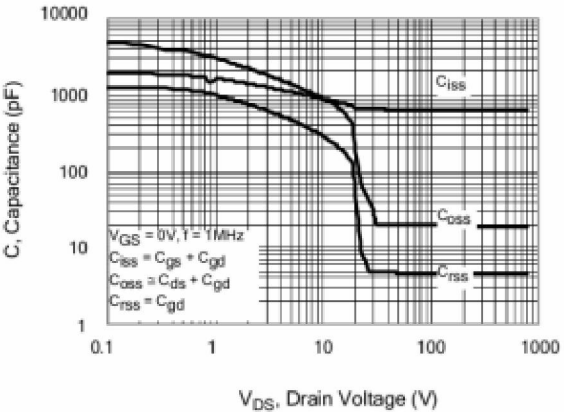


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

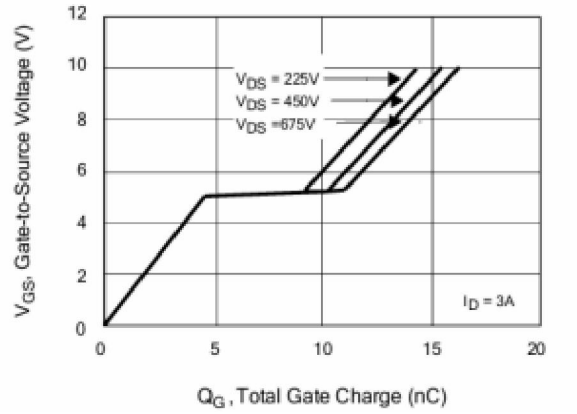
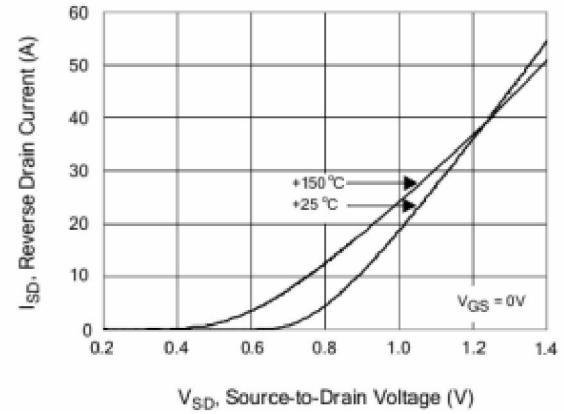


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

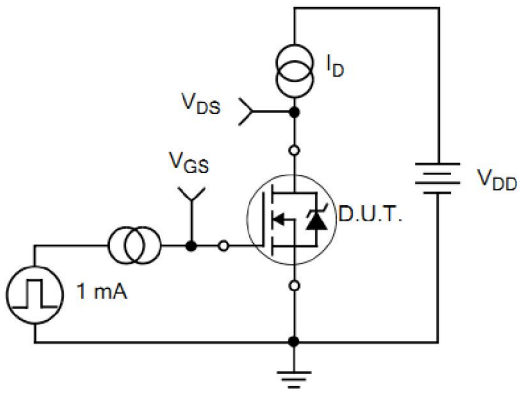


Figure 17. Gate Charge Test Circuit

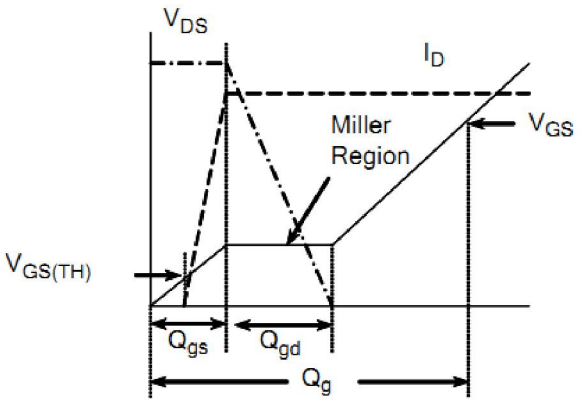


Figure18. Gate Charge Waveforms

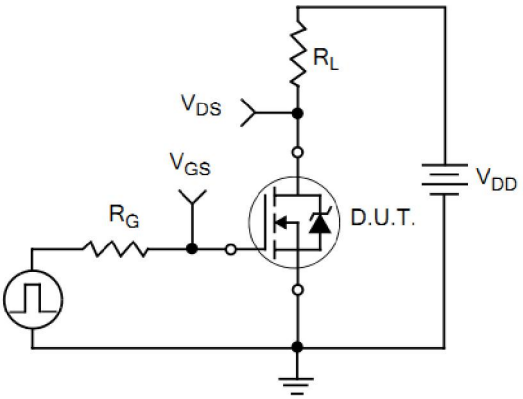


Figure19. Resistive Switching Test Circuit

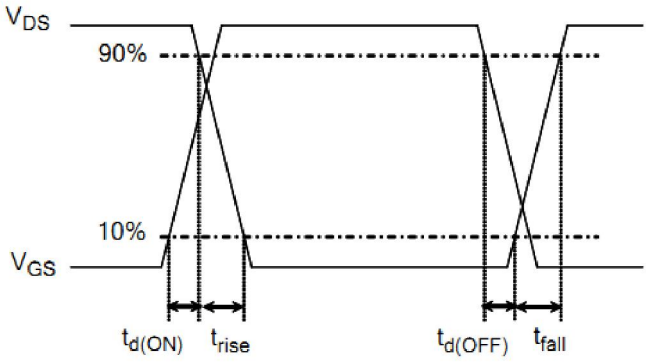


Figure 20. Resistive Switching Waveforms

Test Circuits and Waveforms

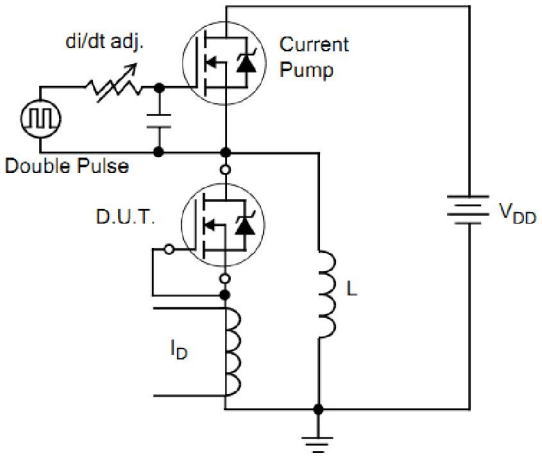


Figure 21. Diode Reverse Recovery Test Circuit

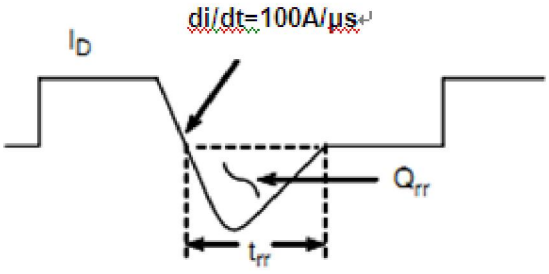


Figure 22. Diode Reverse Recovery Waveform

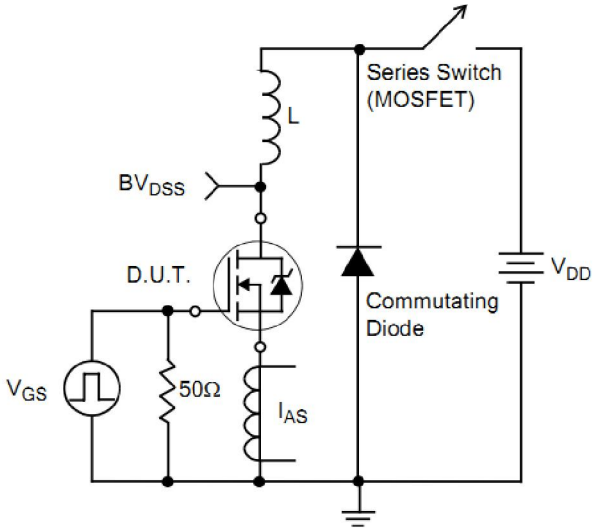
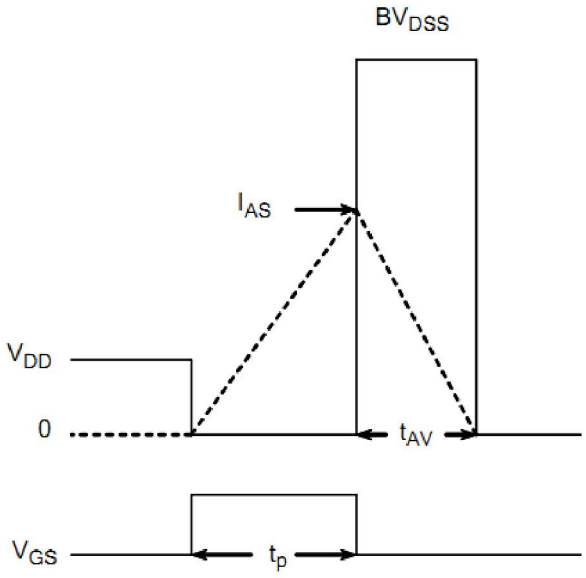


Figure23.Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure24.Unclamped Inductive Switching Waveform

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