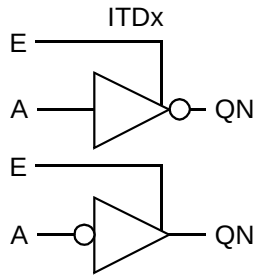
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ITD1x is a family of inverting internal tristate buffers with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

HDL Syntax

Verilog ..... ITDx *inst_name* (QN, A, E);

VHDL..... *inst_name*: ITDx port map (QN, A, E);

Pin Loading

Pin Name	Equivalent Loads			
	ITD1	ITD2	ITD4	ITD6
A	1.0	2.1	4.3	6.4
E	1.6	2.0	3.1	4.1
QN	0.6	0.6	2.5	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ITD1	2.0	TBD	2.9
ITD2	3.0	TBD	4.7
ITD4	5.0	TBD	7.9
ITD6	7.0	TBD	11.5

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	14	27	40	54 (max)
ITD1	From: A To: QN	t_{PLH} t_{PHL}	0.20 0.18	0.96 0.89	1.65 1.52	2.34 2.15	3.09 2.86
	From: E To: QN	t_{ZH} t_{ZL}	0.18 0.14	0.90 0.89	1.61 1.53	2.32 2.15	3.09 2.82
	Number of Equivalent Loads		**1**	**22**	**44**	**65**	**87 (max)**
ITD2	From: A To: QN	t_{PLH} t_{PHL}	0.16 0.13	0.76 0.71	1.34 1.23	1.91 1.73	2.52 2.24
	From: E To: QN	t_{ZH} t_{ZL}	0.15 0.10	0.75 0.69	1.35 1.24	1.91 1.72	2.50 2.22
	Number of Equivalent Loads		**1**	**38**	**77**	**116**	**154 (max)**
ITD4	From: A To: QN	t_{PLH} t_{PHL}	0.14 0.15	0.66 0.63	1.16 1.04	1.66 1.49	2.15 1.97
	From: E To: QN	t_{ZH} t_{ZL}	0.18 0.09	0.69 0.67	1.20 1.11	1.71 1.53	2.23 1.95
	Number of Equivalent Loads		**1**	**55**	**110**	**165**	**220 (max)**
ITD6	From: A To: QN	t_{PLH} t_{PHL}	0.07 0.07	0.70 0.66	1.18 1.09	1.60 1.48	1.99 1.84
	From: E To: QN	t_{ZH} t_{ZL}	0.21 0.03	0.71 0.60	1.18 1.02	1.65 1.42	2.13 1.82

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ITD1	ITD2	ITD4	ITD6
E	QN	t_{HZ} t_{LZ}	0.18 0.08	0.23 0.08	0.35 0.08	0.42 0.08