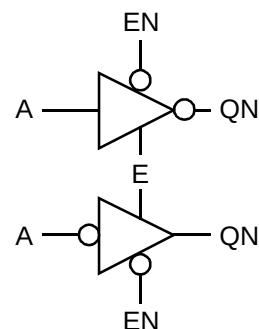


AMI5HG 0.5 micron CMOS Gate Array

Description

ITEx is a family of two-phase inverting internal tristate buffers.

Core
Logic

Logic Symbol	Truth Table																								
ITEx 	<table><tr><th>EN</th><th>E</th><th>A</th><th>QN</th></tr><tr><td>H</td><td>L</td><td>X</td><td>Z</td></tr><tr><td>L</td><td>H</td><td>L</td><td>H</td></tr><tr><td>L</td><td>H</td><td>H</td><td>L</td></tr><tr><td>L</td><td>L</td><td>X</td><td>IL</td></tr><tr><td>H</td><td>H</td><td>X</td><td>IL</td></tr></table> IL = Illegal	EN	E	A	QN	H	L	X	Z	L	H	L	H	L	H	H	L	L	L	X	IL	H	H	X	IL
EN	E	A	QN																						
H	L	X	Z																						
L	H	L	H																						
L	H	H	L																						
L	L	X	IL																						
H	H	X	IL																						

HDL Syntax

Verilog ITEx *inst_name* (QN, A, E, EN);

VHDL..... *inst_name*: ITEx port map (QN, A, E, EN);

Pin Loading

Pin Name	Equivalent Loads			
	ITE1	ITE2	ITE4	ITE6
A	1.0	2.1	4.3	6.4
E	0.5	0.9	2.0	3.1
EN	0.6	1.1	2.4	3.6
QN	0.6	1.2	2.5	3.8

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ITE1	1.0	TBD	1.2
ITE2	2.0	TBD	2.3
ITE4	4.0	TBD	4.7
ITE6	6.0	TBD	7.2

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

Core
Logic

ITE1	Number of Equivalent Loads		1	14	27	40	54 (max)
	From: A To: QN	t_{PLH} t_{PHL}	0.18 0.10	0.91 0.82	1.57 1.45	2.24 2.06	2.98 2.71
	From: EN To: QN	t_{ZH}	0.24	0.94	1.55	2.22	3.03
	From: E To: QN	t_{ZL}	0.20	0.87	1.46	2.05	2.69
	Number of Equivalent Loads		1	22	44	65	87 (max)
ITE2	From: A To: QN	t_{PLH} t_{PHL}	0.16 0.13	0.71 0.68	1.29 1.19	1.84 1.68	2.42 2.19
	From: EN To: QN	t_{ZH}	0.12	0.74	1.31	1.83	2.38
	From: E To: QN	t_{ZL}	0.20	0.79	1.27	1.71	2.17
	Number of Equivalent Loads		1	38	77	116	154 (max)
ITE4	From: A To: QN	t_{PLH} t_{PHL}	0.10 0.10	0.63 0.65	1.13 1.13	1.62 1.60	2.10 2.07
	From: EN To: QN	t_{ZH}	0.14	0.74	1.19	1.64	2.09
	From: E To: QN	t_{ZL}	0.01	0.66	1.16	1.61	2.03
	Number of Equivalent Loads		1	55	110	165	220 (max)
ITE6	From: A To: QN	t_{PLH} t_{PHL}	0.14 0.10	0.62 0.66	1.11 1.09	1.59 1.51	2.07 1.94
	From: EN To: QN	t_{ZH}	0.13	0.70	1.15	1.56	1.94
	From: E To: QN	t_{ZL}	0.16	0.66	1.07	1.49	1.93

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

From	Delay (ns) To	Parameter	Cell			
			ITE1	ITE2	ITE4	ITE6
EN	QN	t_{ZH}	0.14	0.14	0.13	0.13
E	QN	t_{LZ}	0.08	0.08	0.08	0.08