ITP17N50A

N-Channel MOSFET

Lead Free Package and Finish

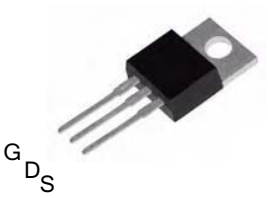
Applications:

- Adaptor
- Charger
- SMPS Standby Power

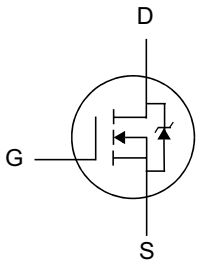
V_{DSS}	$R_{DS(ON)}$ (Typ.)	I_D
500 V	0.3 Ω	17 A

Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve



TO-220
Not to Scale



Ordering Information

PART NUMBER	PACKAGE	BRAND
ITP17N50A	TO-220	ITP17N50A

Absolute Maximum Ratings T_C=25 °C unless otherwise specified

Symbol	Parameter		ITP17N50A	Units
V_{DSS}	Drain-to-Source Voltage	(NOTE *1)	500	V
I_D	Continuous Drain Current		17	A
I_D@ 100 °C	Continuous Drain Current		12	
I_{DM}	Pulsed Drain Current, V_{GS}@ 10V	(NOTE *2)	68	
P_D	Power Dissipation		150	W
	Derating Factor above 25 °C		1.2	W/ °C
V_{GS}	Gate-to-Source Voltage		± 30	V
E_{AS}	Single Pulse Avalanche Engergy L=10 mH		1000	mJ
I_{AS}	Pulsed Avalanche Rating		17	A
dv/dt	Peak Diode Recovery dv/dt	(NOTE *3)	5.0	V/ns
T_L T_{PKG}	Maximum Temperature for Soldering Leads at 0.063 in (1.6 mm) from Case for 10 seconds Package Body for 10 seconds		300 260	°C
T_J and T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	

** Drain Current Limited by Maximum Junction Temperature*

Caution: *Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device*

Thermal Resistance

Symbol	Parameter	ITP17N50A	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.83	°C/W	Drain lead soldered to water cooled heatsink, P_D adjusted for a peak junction temperature of +150 °C.
$R_{\theta JA}$	Junction-to-Ambient	62		1 cubic foot chamber, free air.

OFF Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	V_{GS}=0V, I_D=250μA
$\Delta BV_{DSS}/\Delta T_J$	BreakdownVoltage Temperature Coefficient, Figure 11.	--	0.6	--	V/°C	Reference to 25°C, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1.0	μA	V_{DS}=500V, V_{GS}=0V
		--	--	100		V_{DS}=400V, V_{GS}=0V T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	--	--	0.1	uA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-0.1		V_{GS}= -30V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance Figure 9 and 10.	--	0.30	0.40	Ω	V_{GS}=10V, I_D=7.5A (NOTE *4)
$V_{GS(TH)}$	Gate Threshold Voltage, Figure 12.	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250μA
gfs	Forward Transconductance	--	11	--	S	V_{DS}=20V, I_D=17A (NOTE *4)

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2700	--	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz Figure 14
C_{oss}	Output Capacitance	--	1020	--		
C_{rss}	Reverse Transfer Capacitance	--	325	--		
Q_g	Total Gate Charge	--	56	--	nC	V_{DD}=250V I_D=17A
Q_{gs}	Gate-to-Source Charge	--	9	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	21	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	20	--	ns	V_{DD}=250V I_D=17A V_{GS}=10V R_G=30Ω
t_{rise}	Rise Time	--	39	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	255	--		
t_{fall}	Fall Time	--	71	--		

Source-Drain Diode Characteristics T_C=25 °C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	17	A	Integral pn-diode in MOSFET
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	68	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=17A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	340	--	ns	V_{GS}=0V I_F=17A, di/dt=100 A/μs
Q_{rr}	Reverse Recovery Charge	--	2825	--	nC	

Notes:

*1. T_J = +25 °C to +150 °C.

*2. Repetitive rating; pulse width limited by maximum junction temperature.

*3. I_{SD}=17A di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}, T_J=+150 °C.

*4. Pulse width ≤ 380μs; duty cycle ≤ 2%.

Test Circuits and Waveforms

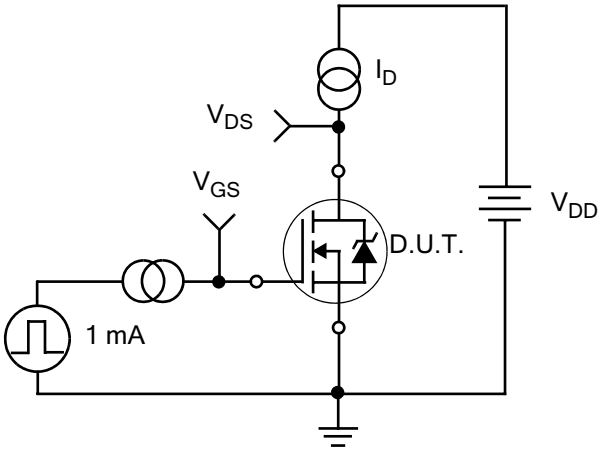


Figure 1. Gate Charge Test Circuit

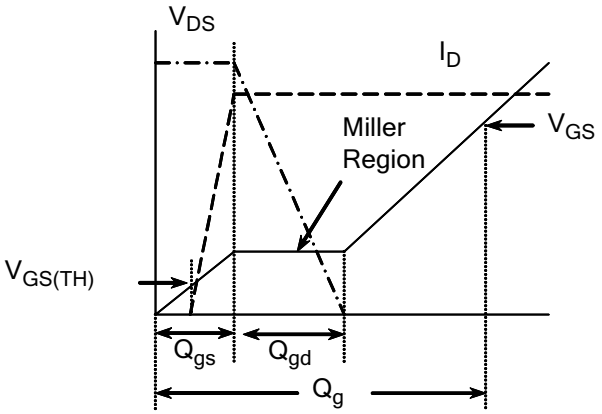


Figure 2. Gate Charge Waveform

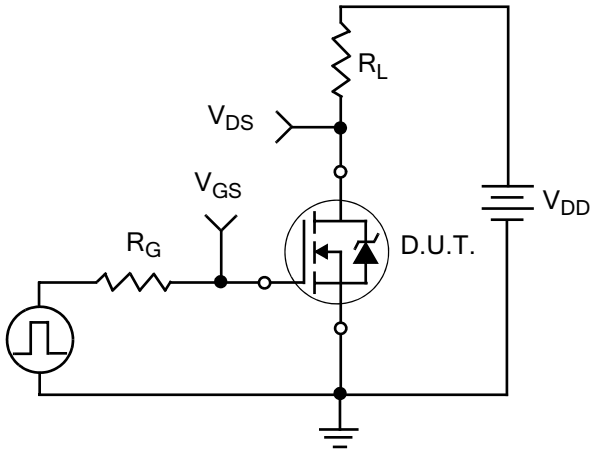


Figure 3. Resistive Switching Test Circuit

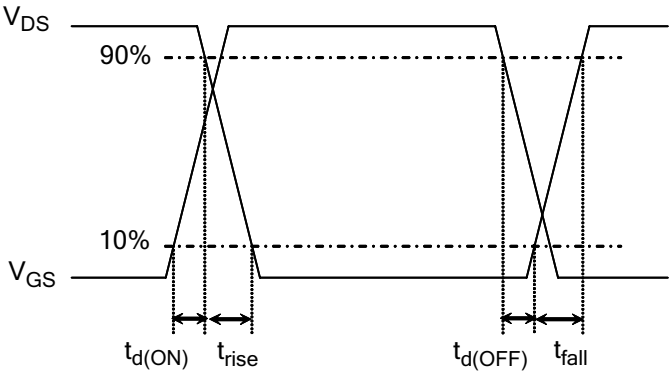


Figure 4. Resistive Switching Waveforms

Test Circuits and Waveforms

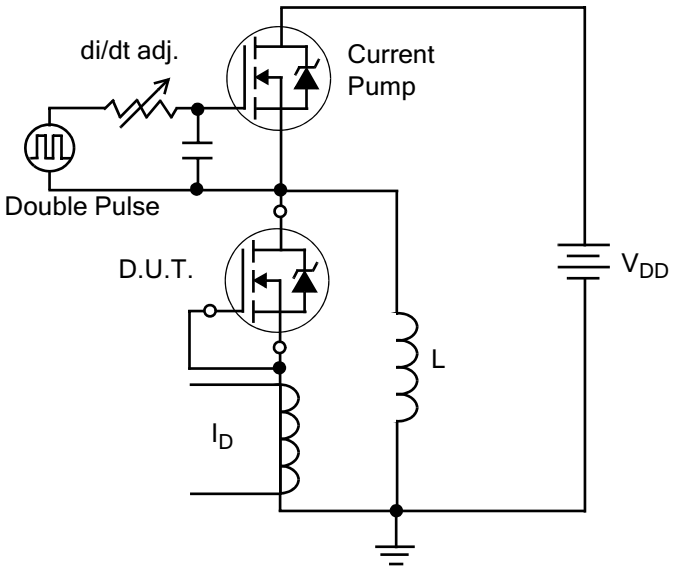


Figure 5. Diode Reverse Recovery Test Circuit

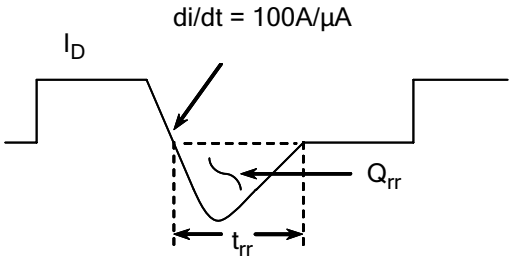


Figure 6. Diode Reverse Recovery Waveform

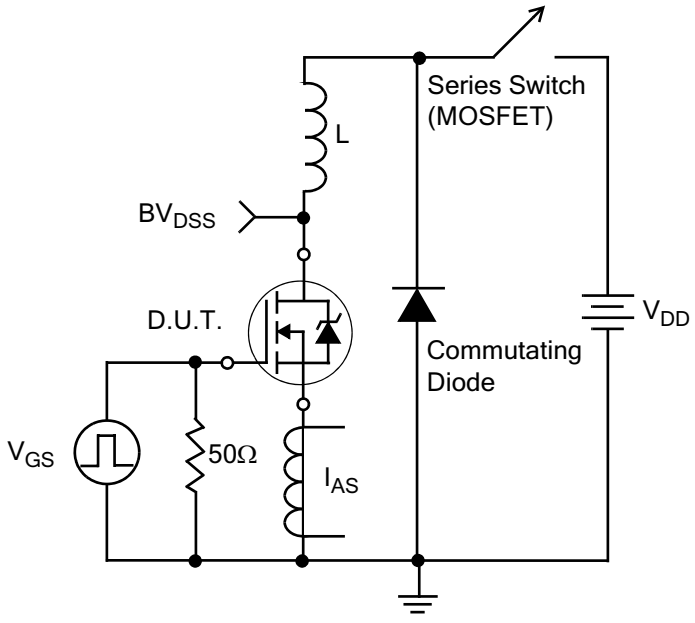
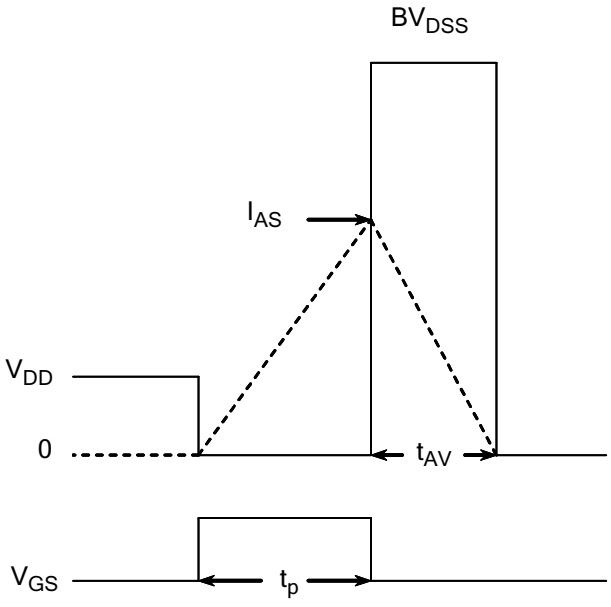


Figure 7. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}{}^2 L}{2}$$

Figure 8. Unclamped Inductive Switching Waveforms

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