Engineering Specification

12.1 inch SVGA Color TFT/LCD Module
Model Name:ITSV53L

Document Control Number : OEM53L-01

Note:Specification is subject to change without notice. Consequently it is better to contact to IBM before proceeding with the design of your product incorporating this module.

**Display Technology, Display Business Unit
International Business Machines Corporation**

IBM Engineering Specification

i Contents

ii Record of Revision

Date	Document Revision	Page	Summary
December 21,1998	OEM53L-01	All	First edition. This module is Based on ITSV53. Unique items are as follows: Bezel : modified ITSV53. Lamp cable : modified ITSV53. 50mm 2pin IF card : modified ITSV53. WA1(JAE) 20pin IF Signa l: modified ITSV53. LVDS Based on Internal Spec.(EC F21255 as of December 16,1998) Based on DWG October 12, 1998.

1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
   Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by IBM for any infringements of patents or other right of the third partied which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of IBM or others.

- The information contained herein may be changed without prior notice. It is therefore advisable to contact IBM before proceeding with the design of equipment incorporating this product.

2.0 General Description

This specification applies to the 12.1 inch Color TFT/LCD Module 'ITSV53L'.

This module is designed for a display unit of notebook style personal computer.

The screen format and electrical interface are intended to support the SVGA (800(H) x 600(V))screen.

Support color is native 262k colors (RGB 6-bit data driver).

All input signals are LVDS compatible.

2.1 Characteristics

The following items are characteristics summary on the table under 25 $^{\circ}$C condition:

ITEMS	SPECIFICATIONS
Screen Diagonal [cm]	30.8 (12.1")
Active Area [mm]	246.0(H) x 184.5(V)
Pixels H x V	800(x3) x 600
Pixel Pitch [mm]	0.3075(per one triad) x 0.3075
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
Typical White Luminance [cd/m^2]	150 Typ(Lamp Power : 3.1W)
Contrast Ratio	150 : 1 Typ.
Optical Rise Time/Fall Time [msec]	30 Typ
Nominal Input Voltage [Volt] VDD	+3.3
Power Consumption [watt]	3.83 Typ.(w/o Inverter loss)
Weight [grams]	370 Typ.
Physical Size [mm]	275(W) x 199(H) x 4.95(D) Typ.
Electrical Interface	Digital Video(6-bit for each color R/G/B) Sync Signal,DOTCLK,4pairs LVDS
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range ($^{\circ}$C) Operating Storage (Shipping)	0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches Color TFT/LCD Module:

IBM Engineering Specification
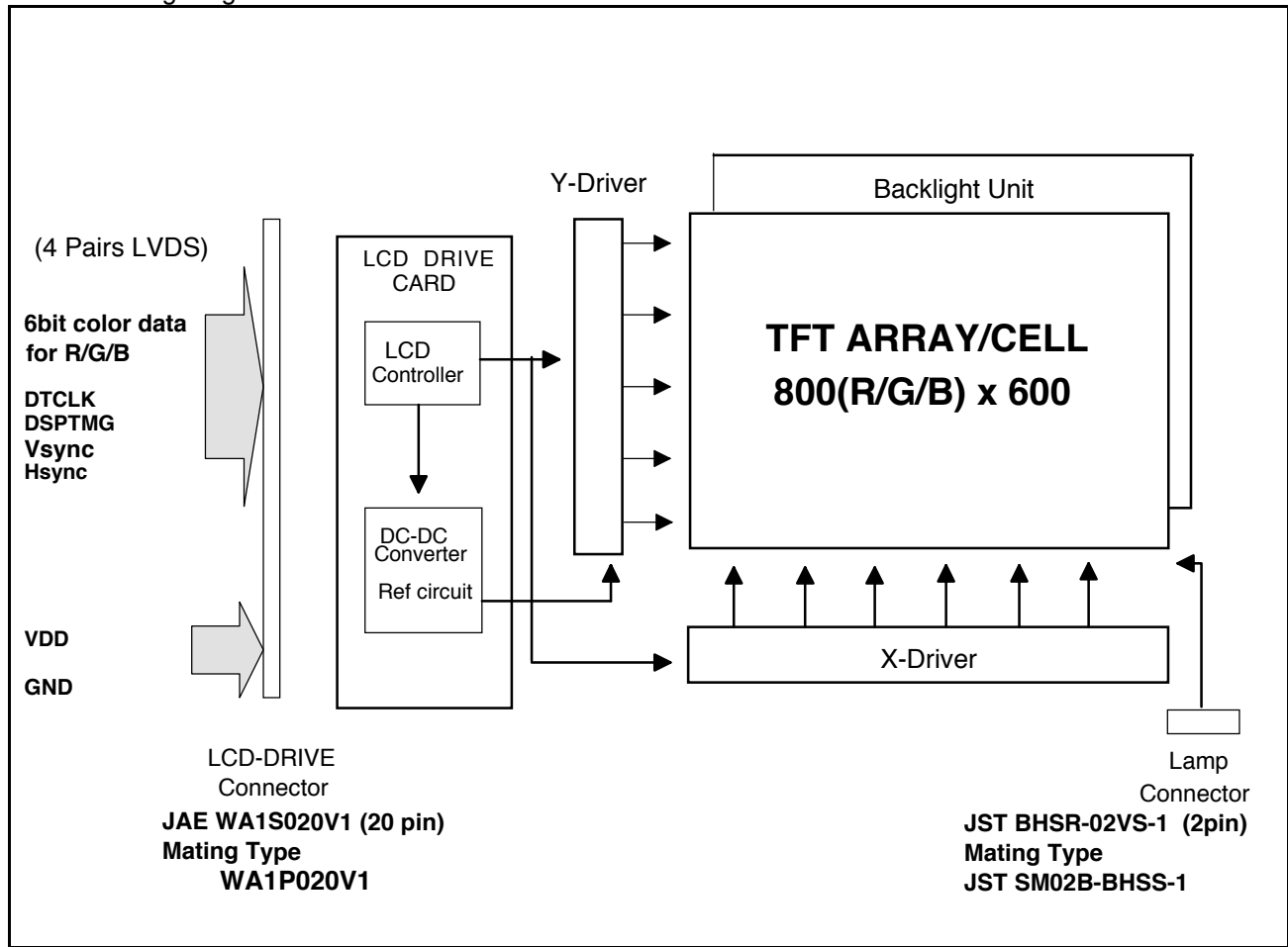
3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+ 4.0	V	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	V	
CFL Inrush current	ICFLL	-	20	mA	Note 2
CFL Ignition Voltage	ViCFLH	-	1,600	Vrms	Ta=0 ℃
CFL Current	ICFL	-	7	mArms	
Operationg Temperature	TOP	-5	+ 55	℃	Note 1
Operationg Humidity	HOP	8	95	%RH	Note 1
Storage Temperature	TST	-22	+ 65	℃	Note 1
Storage Humidity	HST	8	95	%RH	Note 1
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.
Note 2 : Duration=50 msec Max.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item	Conditions		Specification		
			Min	Typ.	Max
Viewing Angle (Degrees)	Horizontal K≥10	(Right) (Left)	40 40	50 50	
K:Contrast Ratio	Vertical K≥10	(Upper) (Lower)	10 20	15 30	
Contrast ratio				150	
Response Time	Rising			30	50
(ms)	Falling			30	50
Color	Red x			0.577	
Chromaticity	Red y			0.338	
(CIE)	Green x			0.310	
	Green y			0.563	
	Blue x			0.158	
	Blue y			0.157	
	White x			0.310	
	White y			0.346	
White Brightness (cd/m2) CFL 6mA				150	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	WA1S020V1
Mating Type / Part Number	WA1P020V1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Signal pin

Pin #	Signal Name	Pin #	Signal Name
1	*VDD (+3.3V)*	2	*VDD (+3.3V)*
3	*GND*	4	*GND*
5	*GND*	6	*GND*
7	*GND*	8	*GND*
9	*Reserved*	10	*Reserved(IBM Mfg option)*
11	*GND*	12	*RxCLK+*
13	*RxCLK-*	14	*RxIN2+*
15	*RxIN2-*	16	*RxIN1+*
17	*RxIN1-*	18	*RxIN0+*
19	*RxIN0-*	20	*GND*

Note:
    1. 'Reserved' pins are not allowed to connect any other line.
    2. Voltage levels of all input signals are LVDS compatible (except VDD).

5.3 Signal Description

This module shall contain column and row drivers to address any given pixel. The host attached PC system shall supply 18 bits (6bits per each color) data and 4-sync signals to these drivers and power supply for back-light. These interface signals and their timing relationship are described below.
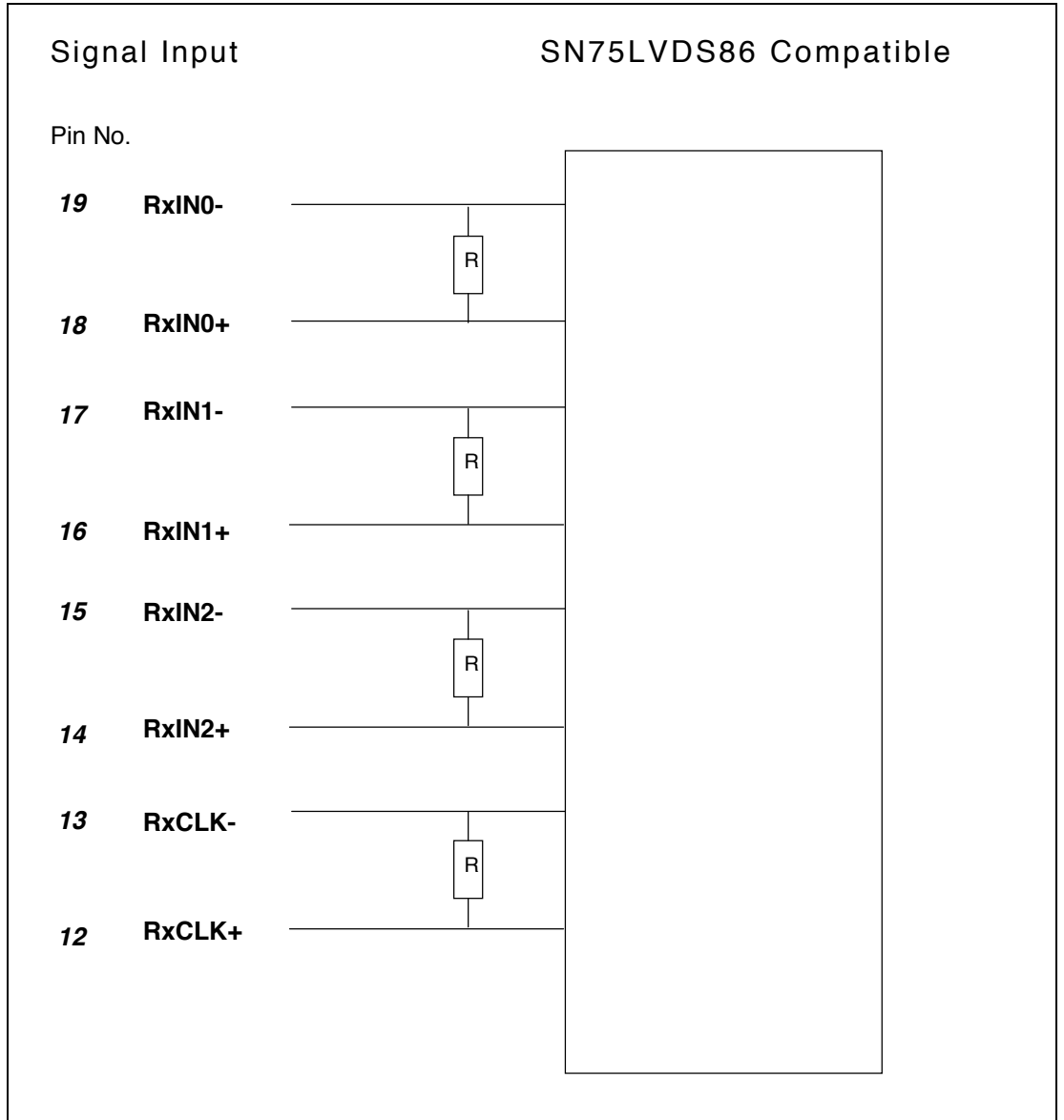
The module uses a LVDS compatible receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84(negative edge sampling) or compatible.

PIN #	SIGNAL NAME	Description
1	VDD	VDD (+3.3V)
2	VDD	VDD (+3.3V)
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	Reserved	Signal Reserved (No Connection)
10	Reserved	Signal Reserved (IBM Mfg option)
11	GND	Ground
12	RxCLK+	Positive LVDS differential clock input
13	RxCLK-	Negative LVDS differential clock input
14	RxIN2+	Positive LVDS differential data input (B2-B5, HSYNC, VSYNC, DSPTMG)
15	RxIN2-	Negative LVDS differential data input (B2-B5, HSYNC, VSYNC, DSPTMG)
16	RxIN1+	Positive LVDS differential data input (G1-G5, B0-B1)
17	RxIN1-	Negative LVDS differential data input (G1-G5, B0-B1)
18	RxIN0+	Positve LVDS differential data input (R0-R5, G0)
19	RxIN0-	Negative LVDS differential data input (R0-R5, G0)

20	GND	Ground

Note: '*Reserved' pis are not allowed to connect any other line.*
Output signals from any system shall be Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as follows;

Signal Input   SN75LVDS86 Compatible

Pin No.

19	**RxIN0-**
18	**RxIN0+**
17	RxIN1-
16	**RxIN1+**
15	RxIN2-
14	**RxIN2+**
13	RxCLK-
12	**RxCLK+**

The module uses a 100 ohm resistor between positive and negative data lines of each reciver input.

SIGNAL NAME	Description
+RED 5 +RED 4 +RED 3 +RED 2 +RED 1 +RED 0	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) **Red-pixel Data** Each red pixel's brightness data consists of these 6 bits pixel pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) **Green-pixel Data** Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) **Blue-pixel Data** Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock** The typical frequency is 40.00MHz. The signal is used to strobe the pixel data and the +DSPTMG signal. +DSPTMG signal is high.
+DSPTMG	**Display Timing** This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync** This signal is synchronized with -DTCLK.

HSYNC	**Horizontal Sync** This signal is synchronized with -DTCLK.
VDD	+3.3V Power Supply
GND	Ground

Note: Output signals from any system shall be Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Signal electrical characteristics are as follows;

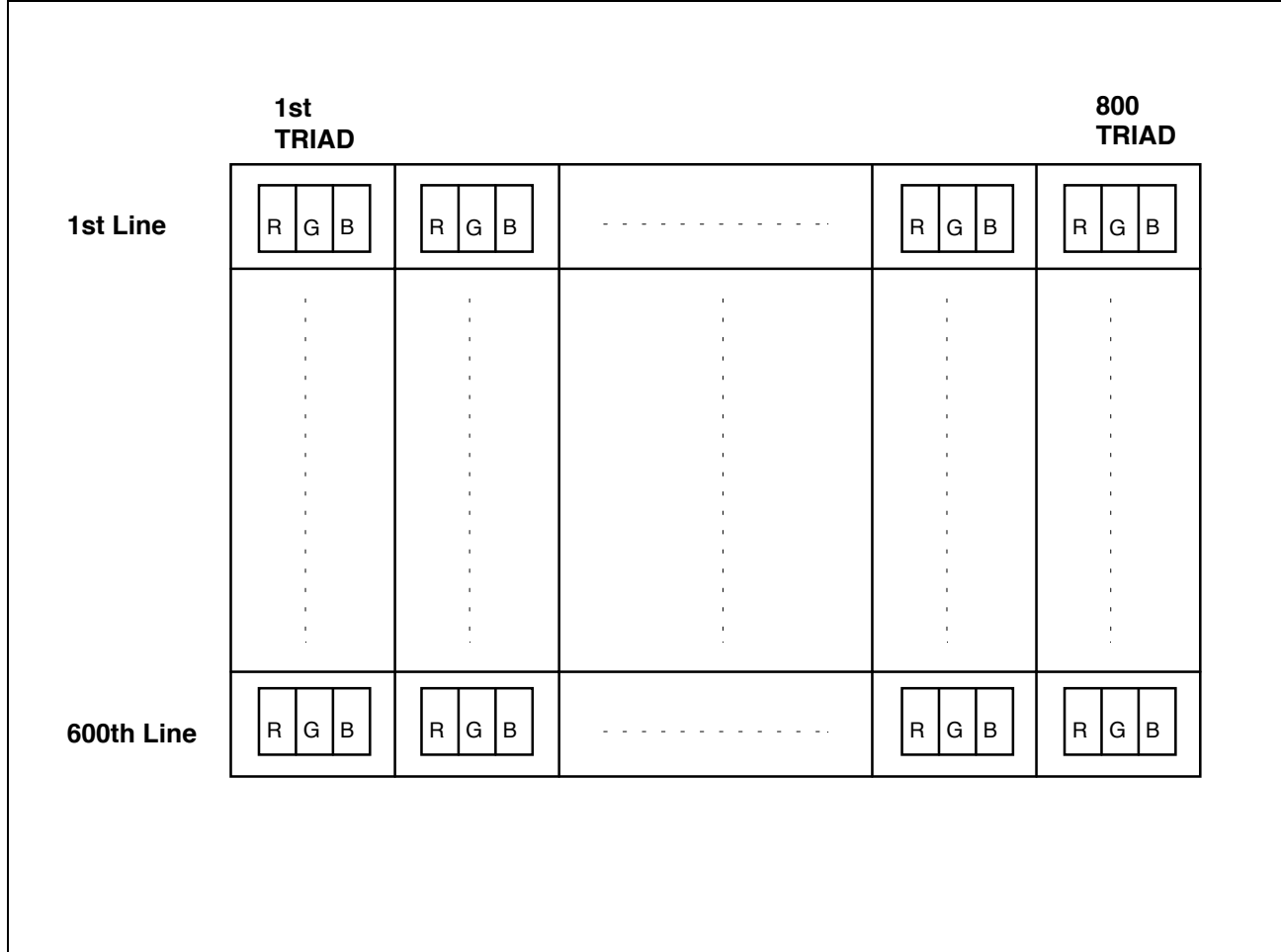| Parameter	Condition	Min	Max	unit
Vth	Differential Input High Voltage (Vcm=+1.2V)		100	mV
Vtl	Differential Input High Voltage (Vcm=+1.2V)	-100		mV

Note:
- It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.
- Input signals shall be low or Hi-Z state when VDD is off.

5.5 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.

7.0 Parameter guide line for CFL Inverter

SYMBOL	PARAMETER	MIN Note3	D.P-1 Note1	D.P-2 Note2	MAX	UNITS	CONDITION
(L63)	White Luminance	-	70	150	-	cd/m^2	(Ta=25°C)
ICFL	CFL current	2	2.5	6	6.5	mArms	(Ta=25°C) Note 5
fCFL	CFL Frequency	40	50	50	60	KHz	(Ta=25°C) Note 3
ViCFL	CFL Ignition Voltage	1,300	-	-	-	Vrms	(Ta=0°C) Note 6
VCFL	CFL Voltage (Reference)		582	522		Vrms	(Ta=25°C) Note 4
PCFL	CFL Power consumption		1.45	3.1		W	(Ta=25°C) Note 4

Note 1: Design Point-1 ; At White Luminance 70cd/m^2, PCFL=1.45W is required.
Note 2: Design Point-2 ; At White Luminance 150cd/m^2, PCFL=3.1 W is required.
Note 3: CFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD.
**Note 4:** Calculated value for reference (ICFL x VCFL = PCFL).
Note 5: It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4mA.
Note 6: CFL inverter should be able to give out a power that has a generating capacity of over 1,300 voltage. Lamp units need 1,300 voltage minimum for ignition.
Note : GND of the inverter should be connected to Frame GND.

The following chart is the current versus the luminance for your reference.

(Lamp Current vs Luminance)
Ta = 25°C
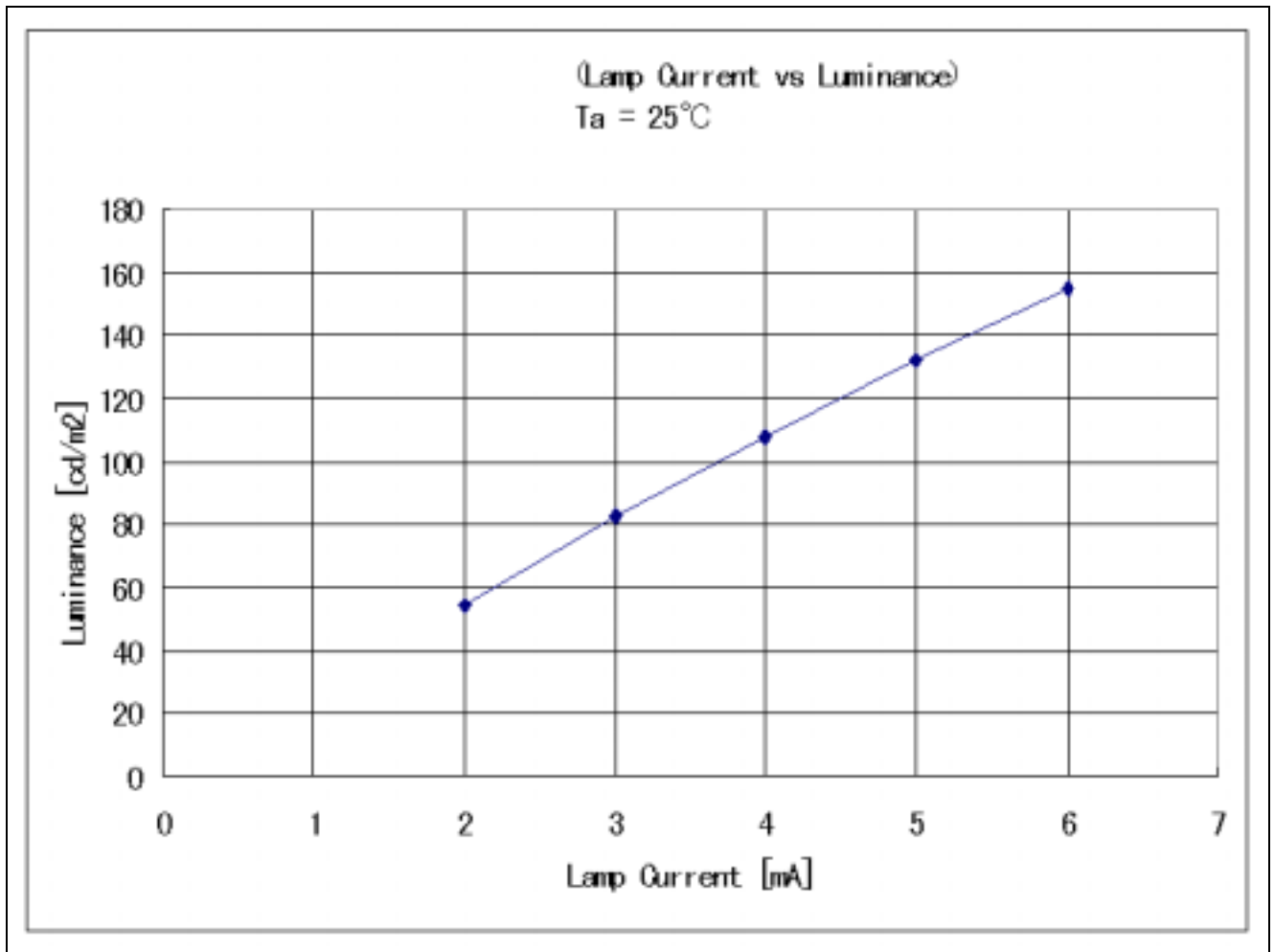
8.0 Interface Timings

Basically, Interface Timings should match the VESA 800 x 600 60Hz manufacturing guideline timing.

8.1 Timing Characteristics

Symbol		Min	Typ	Max	Unit
f_{dck}	DTCLK Frequency	36	40	42	MHz
t_{ck}	DTCLK Cycle Time	23.81	25	27.77	nsec
t_x	X Total Time	848	1,056	1,088	t_{ck}
t_{acx}	X Active Time		800		t_{ck}
t_{bkx}	X Blank Time	48	256	288	t_{ck}
H_{freq}	H-Frequency	35.16	37.88	38.46	KHz
H_w	H-Sync Width	8	128	152	t_{ck}
H_{fp}	H-Sync Front Porch	8	40	272	t_{ck}
H_{bp}	H-Sync Back Porch	8	88	272	t_{ck}
t_y	Y Total Time	611	628	1,025	t_x
t_{acy}	Y Active Time		600		t_x
t_{bky}	Y Blank Time		28		t_x
V_{freq}	Frame Rate	56.25	60	61	Hz
V_w	V-Sync Width	1	4	7	t_x
V_{fp}	V-Sync Front Porch	1	1	415	t_x
V_{bp}	V-Sync Back Porch	9	23	29	t_x

8.2 Supported Video Timing
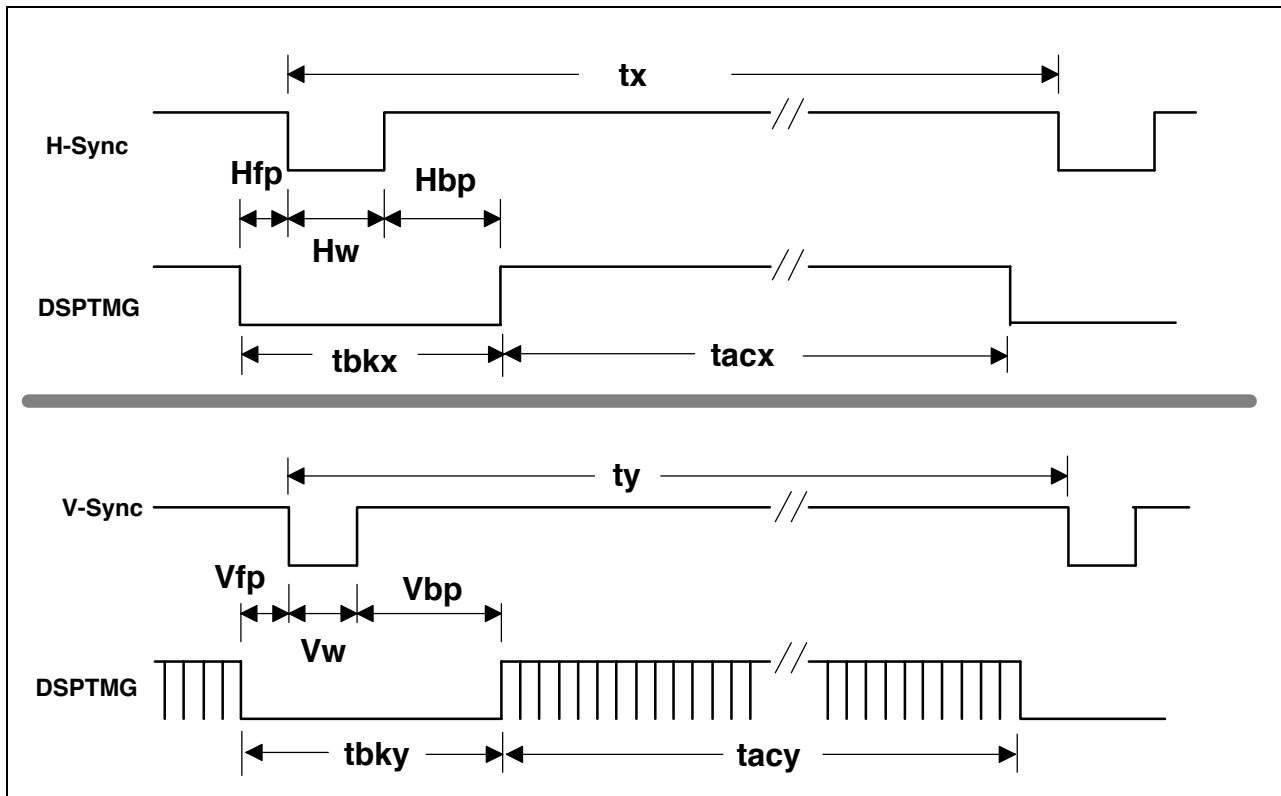
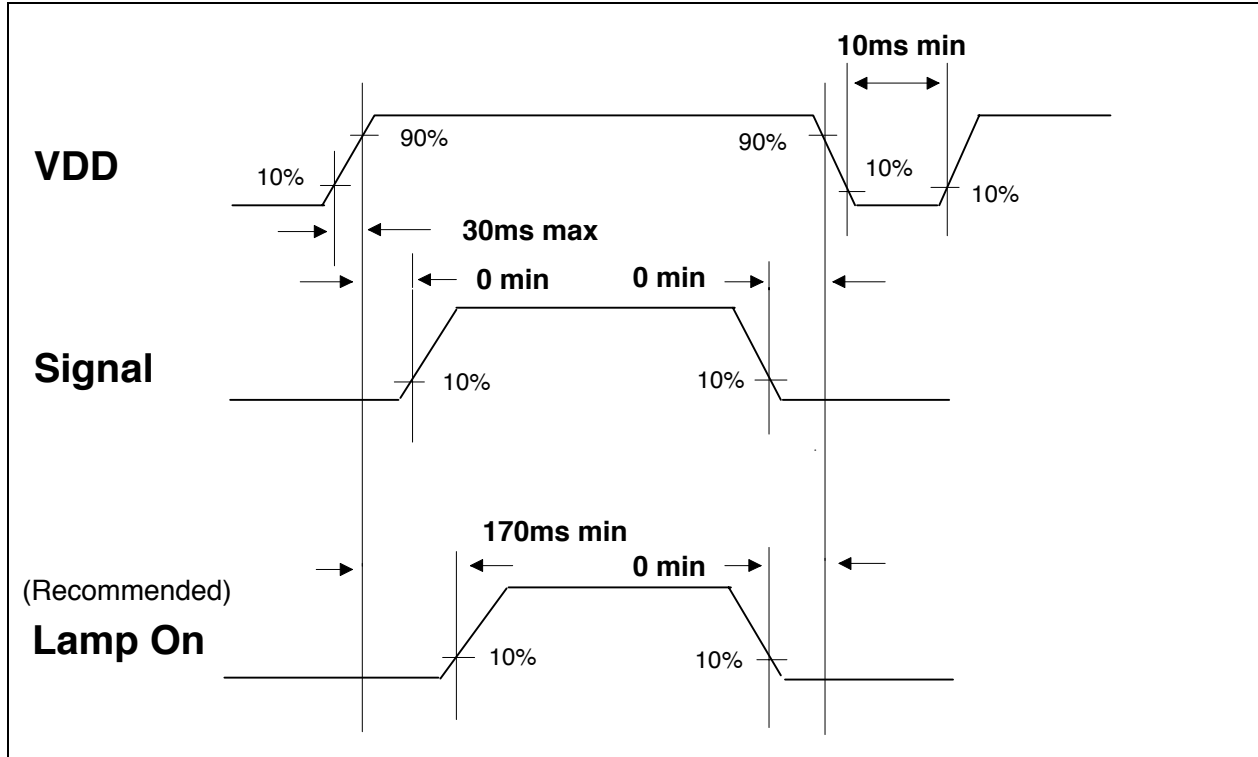## 9.0 Power Consumption

Input power specifications are as follows;

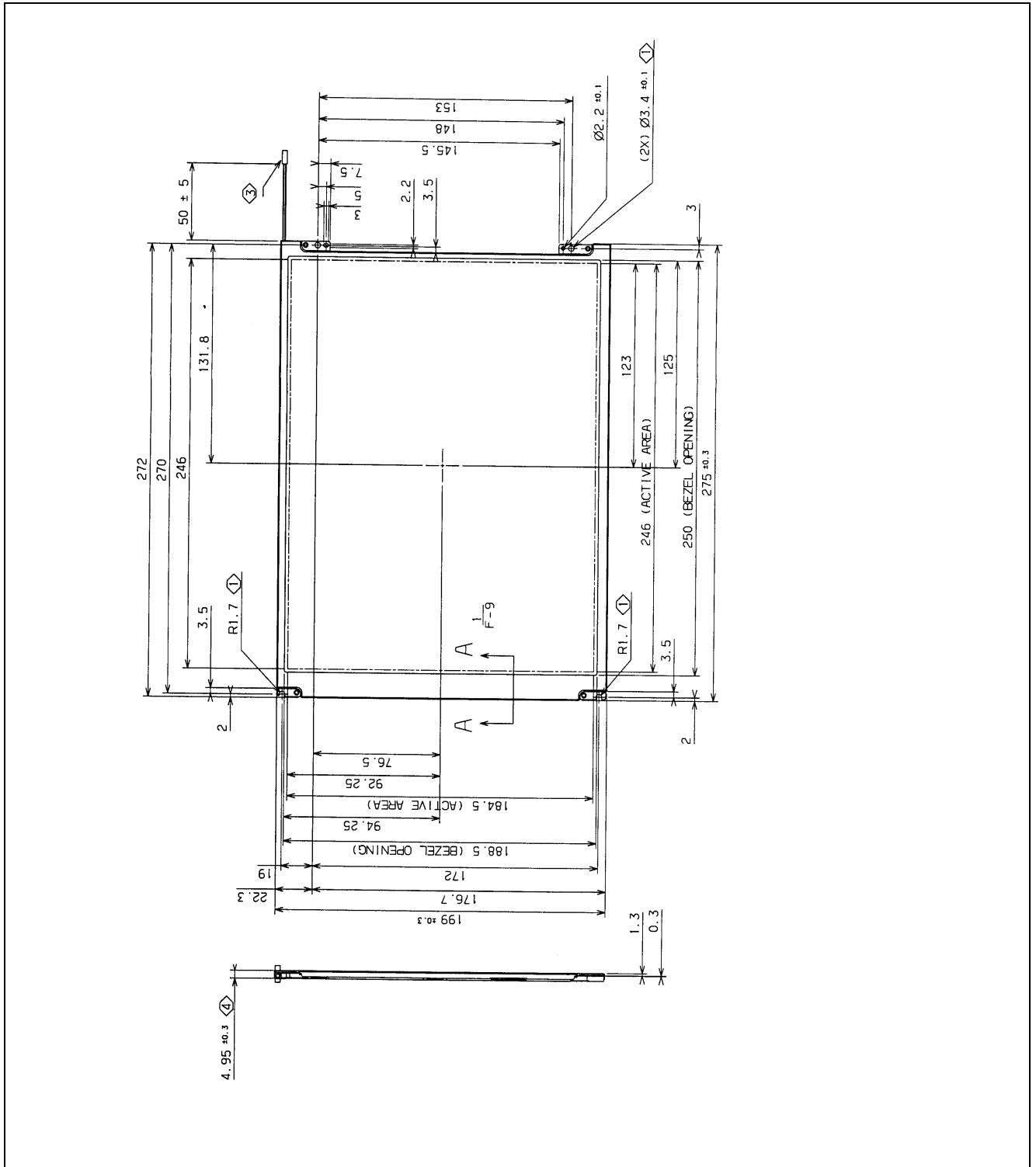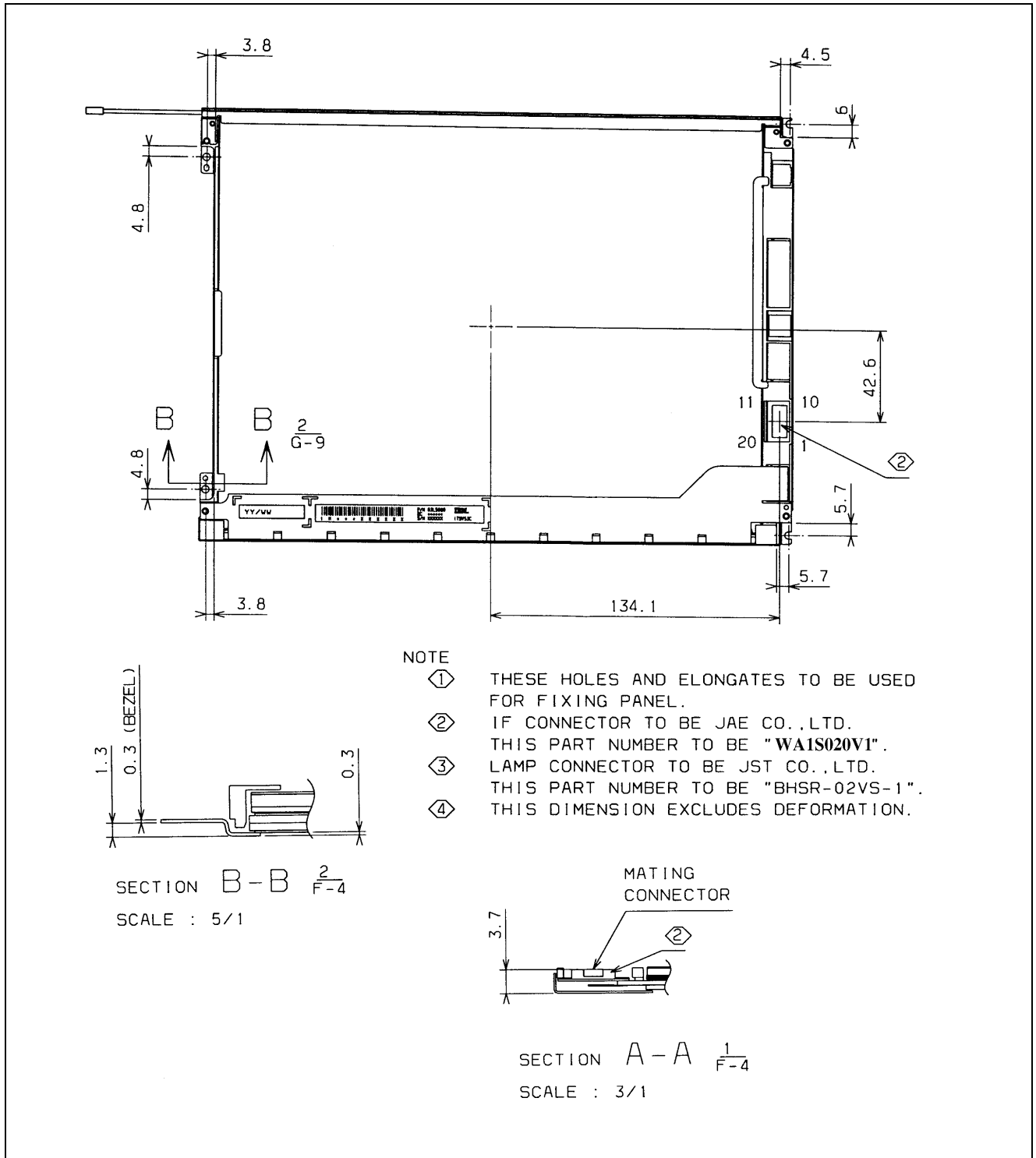| SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3	3.3	3.6	V	Load Capacitance 20uF
PDD	VDD Power	0.62	0.73	0.85	W	64-Gray Scale (Note 1)
PDD	VDD Power	0.95	1.15	1.3	W	Sub-pixel vertical stripe (Note 1)
PDD max	VDD Power max	-	-	1.42	W	Sub-pixel vertical stripe (Note 2)
IDD max	IDD Current max	–	–	394	mA	Sub-pixel vertical stripe (Note 2)
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Note 1: VDD=+3.3V

Note 2: VDD=+3.6V

10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.

11.0 Mechanical Characteristics

NOTE

⟨1⟩ THESE HOLES AND ELONGATES TO BE USED
     FOR FIXING PANEL.
⟨2⟩ IF CONNECTOR TO BE JAE CO.,LTD.
     THIS PART NUMBER TO BE "WA1S020V1".
⟨3⟩ LAMP CONNECTOR TO BE JST CO.,LTD.
     THIS PART NUMBER TO BE "BHSR-02VS-1".
⟨4⟩ THIS DIMENSION EXCLUDES DEFORMATION.

SECTION B-B 2/F-4

SCALE : 5/1

MATING
CONNECTOR

SECTION A-A 1/F-4

SCALE : 3/1

****** End Of Page ******