

Engineering Specification

**12.1 inches XGA Color TFT/LCD Module
Model Name:ITXG00**

Document Control Number : OEM00-04

Note:Specification is subject to change without notice. Consequently it is better to contact to IBM before proceeding with the design of your product incorporating this module.

**Display Business Unit
International Business Machines Corporation**

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ii Record of Revision

| Date | Document Revision | Page | Summary |
|------------------|-------------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| October 8,1999 | OEM00-01 | All | First Edition for customer. Based on Initial Internal Spec. as of October 1,1999. Based on Mechanical Drawing as of October 7,1999. |
| February 21,2000 | OEM00-02 | 4 5 7 8 11 13 15 16 17 21, 22 | To update the Handling Precautions To specify the Typical White Luminance of "Design Point 1" To specify/change the Lamp Power Consumption To change the Absolute Maximum Rating of "Vin" To specify the Color Chromaticity To update the figure To update the Signal Electrical Characteristics To update the Parameter Guide Line for CFL Inverter To add the reference figure To change the Timing Characteristics of "fdck", "tacx", and "tacy" To update the drawings (as of 07Dec99) |
| March 23,2000 | OEM00-03 | 13 18 22,23 | To update the LVDS Macro AC Characteristics To correct the Timing Characteristics of "fdck" and "tck" To update the drawings to change the CFL cable length |
| May 29,2000 | OEM00-04 | 4 5 20 22,23 24 | To update Handling Precautions To update Logic Power Consumption and Lamp Power Consumption To update Power Consumption To update the drawings (as of 10May00) To add National Test Lab Requirement |



1.0 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) Do not stick the adhesive tape on the reflector sheet at the back of the module.
- 10) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge.
Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
- 11) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 12) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 13) The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- 14) Small amount of materials having no flammability grade is used in the LCD module.
The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL1950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end product.
- 15) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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2.0 General Description

This specification applies to the 12.1 inches Color TFT/LCD Module 'ITXG00'.

This module is designed for a display unit of notebook style personal computer.

The screen format and electrical interface are intended to support the XGA (1024(H) x 768(V))screen.

Support color is native 262k colors (RGB 6-bit data driver).All input signals are LVDS interface compatible.

This module does not contain a inverter card for backlight.

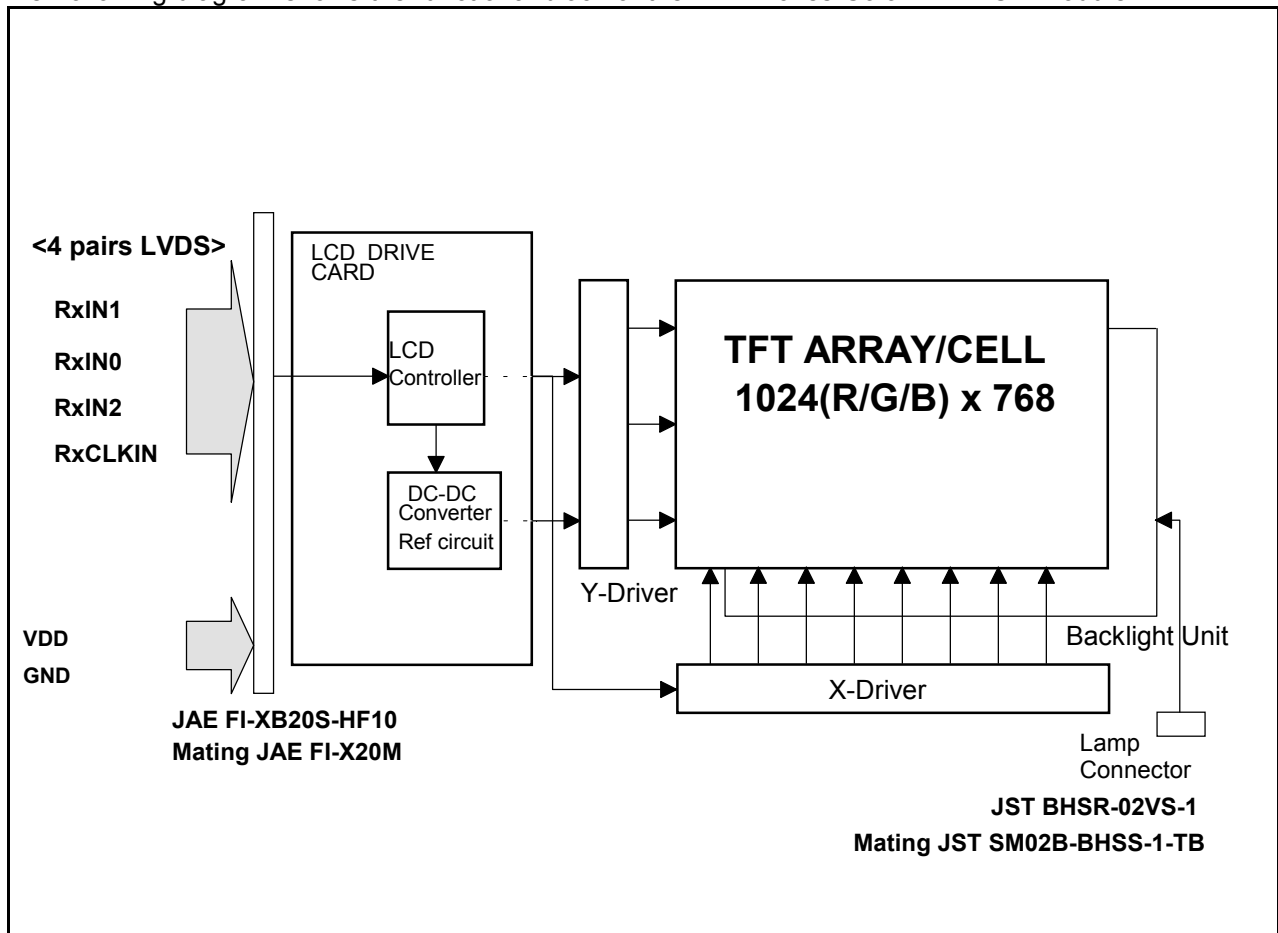
2.1 Characteristics

The following items are characteristics summary on the table under 25 °C condition:

| ITEMS | SPECIFICATIONS |
|------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| Screen Diagonal [mm] | 307.2 (12.1") |
| Active Area [mm] | 245.76(H) x 184.32(V) |
| Pixels H x V | 1024(x3) x 768 |
| Pixel Pitch [mm] | 0.240(per one triad x3) x 0.240 |
| Pixel Arrangement | R.G.B. Vertical Stripe |
| Display Mode | Normally White |
| Typical White Luminance [cd/m ²] Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA) | 90 Typ.(Center), 80 Typ (5 points average) 150 Typ.(Center), 140 Typ.(5 points average) |
| Contrast Ratio | 200 : 1 Typ. |
| Optical Rise Time/Fall Time [msec] | 30 Typ., 50 Max.(each) |
| Nominal Input Voltage [Volt] VDD | +3.3 Typ. |
| Logic Power Consumption[watt] (VDD line) | 1.3 Typ. |
| Lamp Power Consumption [watt] Design Point 1:(ICFL=3.5mA) Design Point 2:(ICFL=6.5mA) | 2.0 Typ. 3.5 Typ. |
| Weight [grams] | 370 Typ.(w/o Inverter) |
| Physical Size [mm] | 262(W) x 198(H) x 5.7(D) Typ. |
| Electrical Interface | 6-bit digital video for each color R/G/B, 3 sync, Clock 4 pairs LVDS |
| Support Color | Native 262K colors (RGB 6-bit data driver) |
| Temperature Range (°C) Operating Storage (Shipping) | 0 to +50 -20 to +60 |

2.2 Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

| Item | Symbol | Min | Max | Unit | Conditions |
|-------------------------------------------|--------|------|------------|-------|-----------------|
| Supply Voltage Logic/LCD Drive Voltage | VDD | -0.3 | +4.5 | V | |
| Input Voltage of Signal | Vin | -0.3 | VDD+0.3 | V | |
| CFL Inrush current | ICFLL | - | 20 | mA | Note 2 |
| CFL Current | ICFL | - | 7 | mArms | |
| CFL Ignition Voltage | Vs | - | 1800 | Vrms | |
| Operating Temperature | TOP | 0 | +50 | °C | Note 1 |
| Operating Relative Humidity | HOP | 8 | 95 | %RH | Note 1 |
| Storage Temperature | TST | -20 | +60 | °C | Note 1 |
| Storage Relative Humidity | HST | 5 | 95 | %RH | Note 1 |
| Vibration | | | 1.5 10-200 | G Hz | |
| Shock | | | 50 18 | G ms | Half sine wave. |

Note 1 : Maximum Wet-Bulb should be 39°C and No condensation.

Note 2 : Duration=50 msec Max.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25°C condition:

| Item | Conditions | Specification | |
|------------------------------------------------|--------------------------|---------------------------------------------|---------|
| | | Typ. | Note |
| Viewing Angle (Degrees) | Horizontal (Right) | 40 | - |
| | K _{≥10} (Left) | 40 | - |
| K: Contrast Ratio | Vertical (Upper) | 15 | - |
| | K _{≥10} (Lower) | 30 | - |
| Contrast ratio | | 200 | - |
| Response Time (ms) | Rising | 30 | 50(Max) |
| | Falling | 30 | 50(Max) |
| Color Chromaticity (CIE) | Red x | 0.577 | - |
| | Red y | 0.338 | - |
| | Green x | 0.310 | - |
| | Green y | 0.554 | - |
| | Blue x | 0.158 | - |
| | Blue y | 0.124 | - |
| | White x | 0.313 | - |
| | White y | 0.329 | - |
| White Luminance (cd/m ²) CFL 6.5mA | | 150 Center 140 5 points average | |

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| | |
|------------------------------|----------------------|
| Connector Name / Designation | For Signal Connector |
| Manufacturer | JAE |
| Type / Part Number | FI-XB20S-HF10 |
| Mating Type / Part Number | FI-X20M |

| | |
|------------------------------|--------------------|
| Connector Name / Designation | For Lamp Connector |
| Manufacturer | JST |
| Type / Part Number | BHSR-02VS-1 |
| Mating Type / Part Number | SM02B-BHSS-1-TB |

5.2 Signal Pin

| Pin# | Signal | Pin# | Signal |
|------|--------|------|----------|
| 2 | VDD | 12 | RxIN2- |
| 3 | VDD | 13 | RxIN2+ |
| 4 | GND | 14 | GND |
| 5 | GND | 15 | RxCLKIN- |
| 6 | RxIN0- | 16 | RxCLKIN+ |
| 7 | RxIN0+ | 17 | GND |
| 8 | GND | 18 | Reserved |
| 9 | RxIN1- | 19 | Reserved |
| 10 | RxIN1+ | 20 | GND |
| 11 | GND | 21 | GND |

Note: Pin# 1 and 22 are connected to FG. Pin#s of mating connector are from #2 to #21.

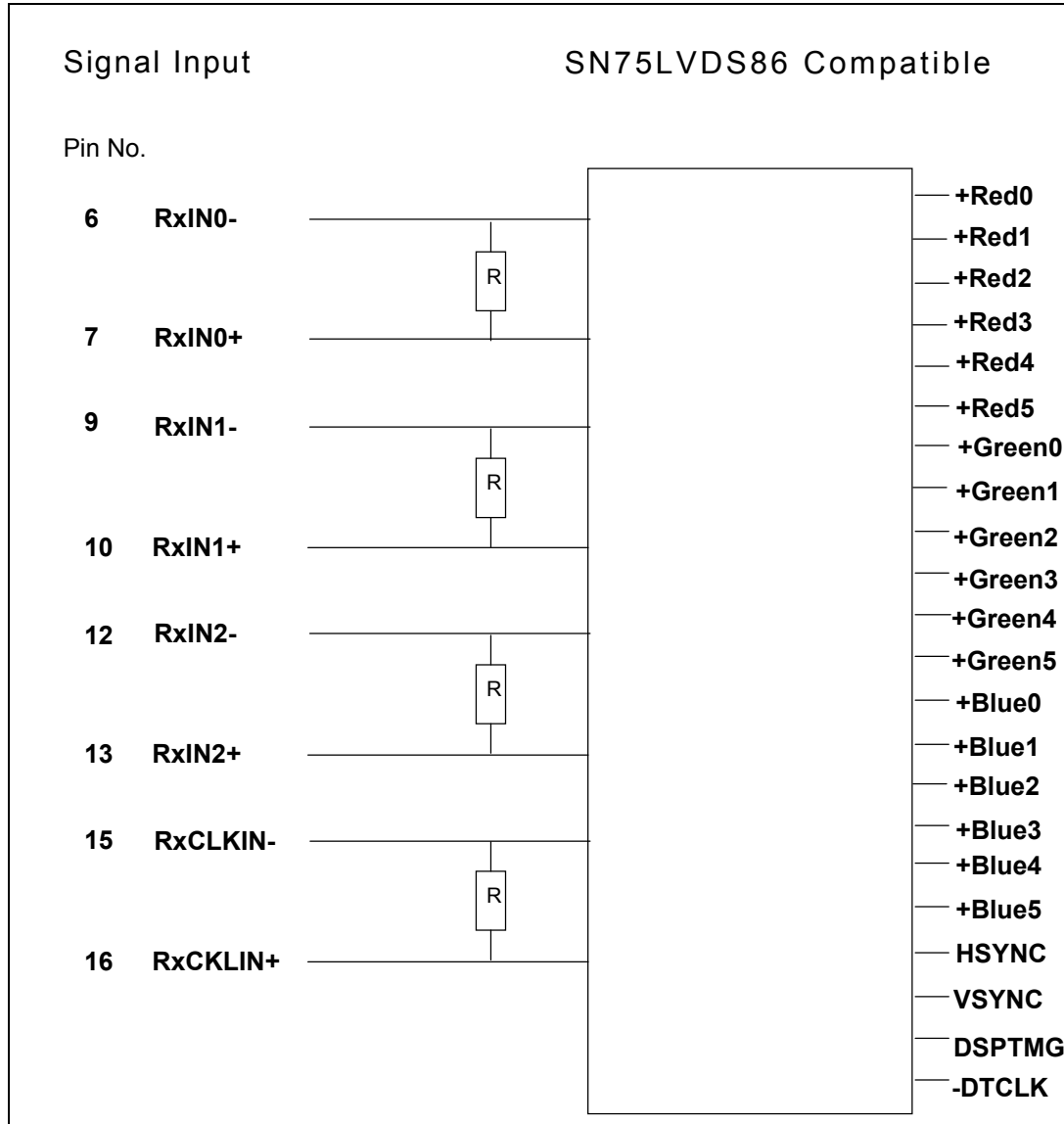
5.3 Signal Description

The module uses a LVDS compatible receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84(negative edge sampling) or compatible.

| Signal Name | Description |
|--------------------|------------------------------------------------------------------|
| RxIN0+, RxIN0- | LVDS differential data input (Red0-Red5, Green0) |
| RxIN1+, RxIN1- | LVDS differential data input (Green1-Green5,Blue0-Blue1) |
| RxIN2+, RxIN2- | LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG) |
| RxCLKIN+, RxCLKIN- | LVDS differential clock input |
| VDD | +3.3V Power Supply |
| GND | Ground |

Note: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as follows:



The module uses a 100ohm resistor between positive and negative data lines of each receiver input.



| SIGNAL NAME | Description | |
|----------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| +RED5 +RED4 +RED3 +RED2 +RED1 +RED0 | Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data | Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data. |
| +GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0 | Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data | Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data. |
| +BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0 | Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data | Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data. |
| -DTCLK | Data Clock | The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high. |
| DSPTMG | Display Timing | This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC | Vertical Sync | The signal is synchronized to -DTCLK . |
| HSYNC | Horizontal Sync | The signal is synchronized to -DTCLK . |

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

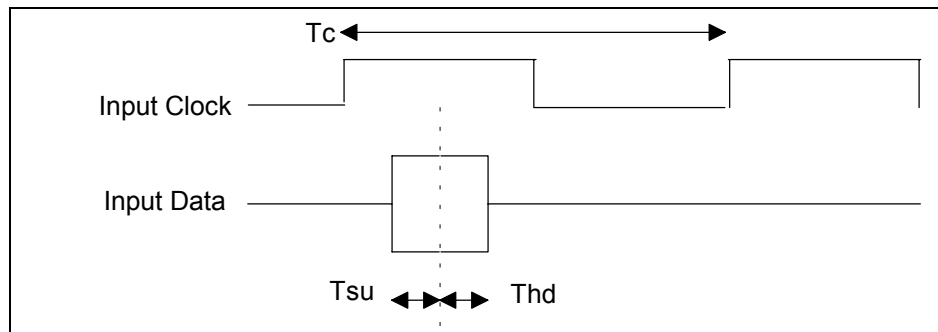
Signal electrical characteristics are as follows;

| Parameter | Condition | Min | Typ | Max | unit |
|-----------|---------------------------------------------|------|-----|-----|------|
| Vth | Differential Input High Voltage (Vcm=+1.2V) | | 50 | 100 | mV |
| Vtl | Differential Input High Voltage (Vcm=+1.2V) | -100 | 50 | | mV |
| Vcm | Vth-Vtl=200mV | 1.0 | 1.2 | 1.5 | V |
| dVcm | Vth-Vtl=200mV | -50 | | 50 | mV |

LVDS Macro AC characteristics are as follows:

| | Symbol | Min | Typ | Max | unit | Conditions |
|-----------------------|--------|-------|-------|-------|------------|-------------------------------------------------------------|
| Clock Frequency | Fc | 50 | 65 | 67 | [MHz] | |
| Cycle Time | Tc | 14.93 | 15.38 | 20.00 | [ns] | |
| PLL Lock Time | Tpll | | | 10 | [ms] | |
| Data Setup Time | Tsu | 600 | | | [ps] | Fc=65MHz, Jitter<50ps, Vth-Vtl=200mV, Vcm=1.2V, Delta Vcm=0 |
| Data Hold Time | Thd | 600 | | | [ps] | |
| Cycle-to-cycle Jitter | TCCJM | -150 | | 150 | [ps] | |
| Cycle Modulation Rate | TCJavg | | | 20 | [ps/clock] | Note |

Note: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

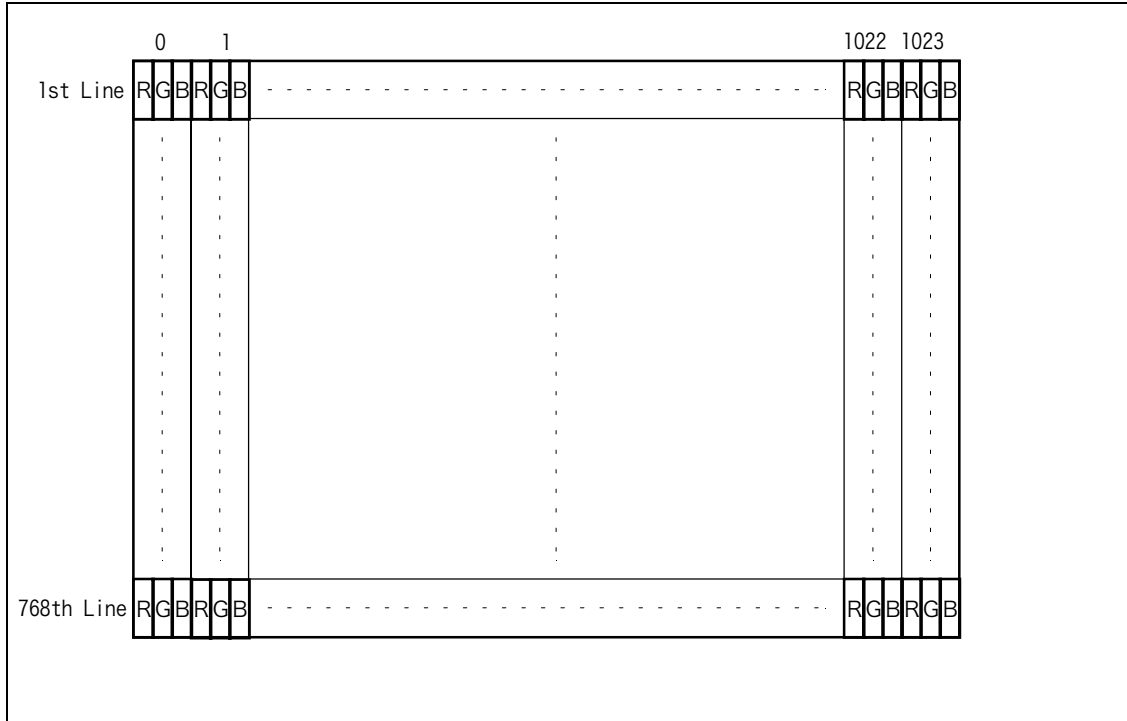


5.5 Signal for Lamp connector

| Pin # | Signal Name |
|-------|-------------------|
| 1 | Lamp High Voltage |
| 2 | Lamp Low Voltage |

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format image.



7.0 Parameter Guide Line for CFL Inverter

| PARAMETER | MIN | DP-1 | DP-2 | MAX | UNITS | CONDITION |
|-----------------------------------------------|-------|----------|------------|-----|-------------------|----------------------------|
| White Luminance center 5 points average | - | 90 80 | 150 140 | - | cd/m ² | (Ta=25°C) |
| CFL current(ICFL) | 2.5 | 3.5 | 6.5 | 6.5 | mArms | (Ta=25°C) Note 4 |
| CFL Frequency(FCFL) | 40 | 42 | 42 | 60 | KHz | (Ta=25°C) Note 1 |
| CFL Ignition Voltage(Vs) | 1,250 | - | - | - | Vrms | (Ta= 0°C) Note 3 |
| CFL Voltage (Reference)(VCFL) | - | 560 | 545 | - | Vrms | (Ta=25°C) Note 2 |
| CFL Power consumption(PCFL) | - | 1.96 | 3.54 | - | W | (Ta=25°C) Note 2 |

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,250 voltage. Lamp units need 1,250 voltage minimum for ignition.

Note 4: It should be employed the inverter which has "Duty Dimming", if ICFL is less than 4 mA.

Note 5: DP-1 and DP-2 are IBM recommended Design Points.

*1 All of characteristics listed are measured under the condition using the IBM Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

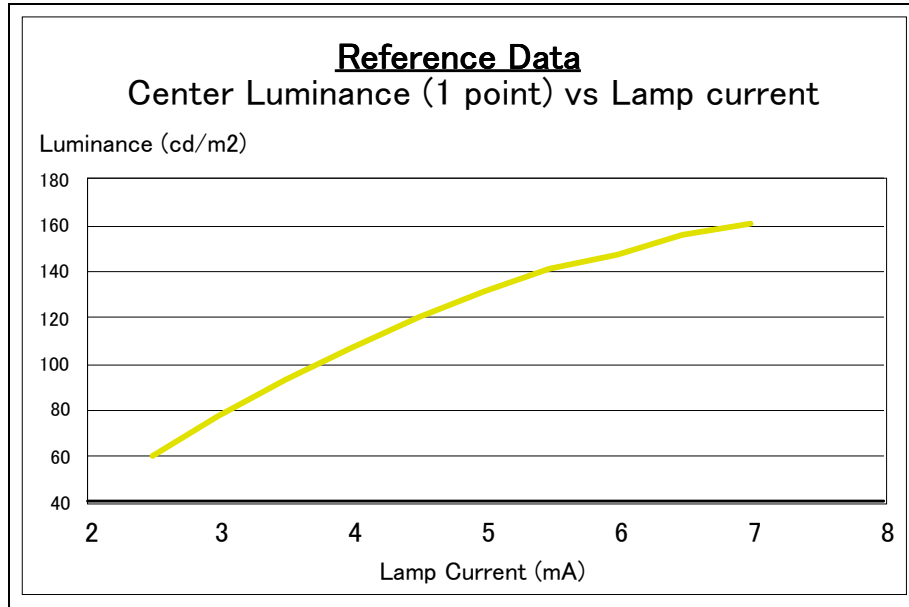
*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

The following chart is CFL current versus the luminance for your reference.



8.0 Interface Timings

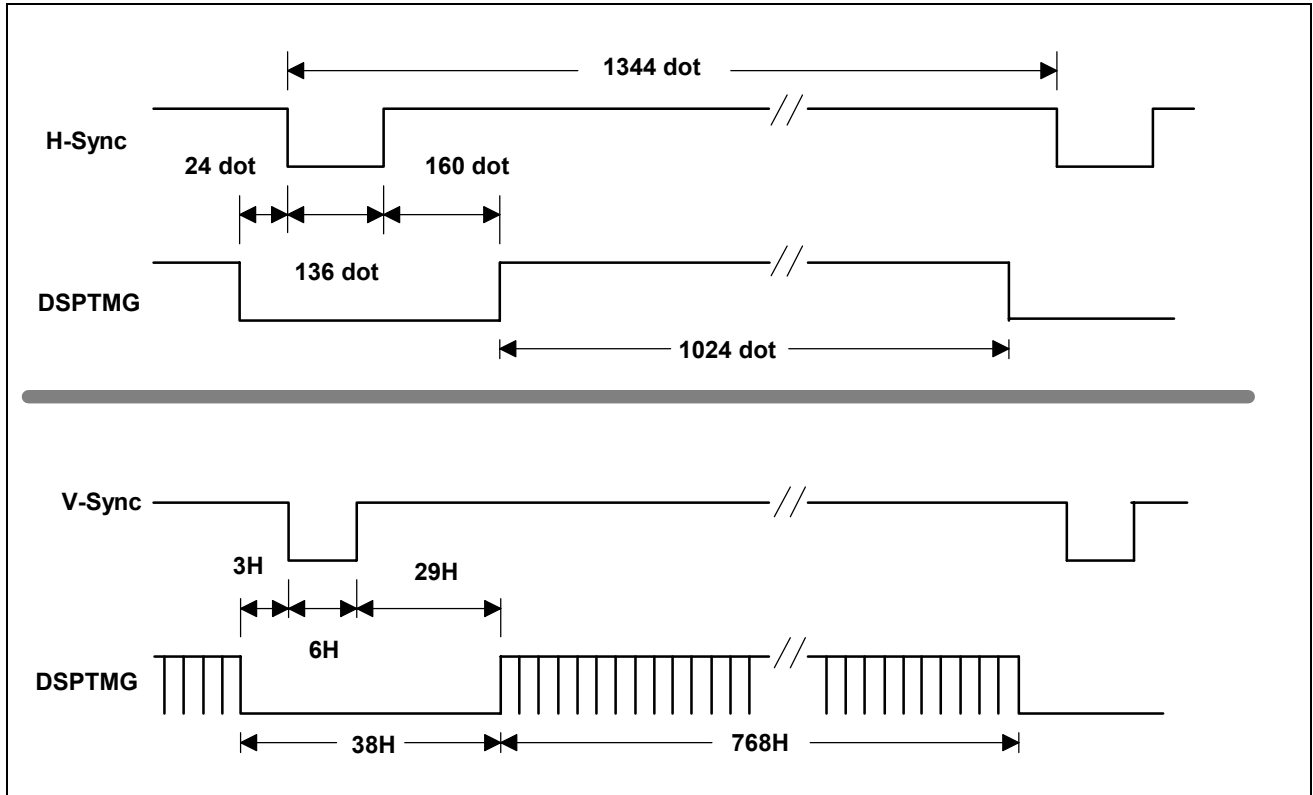
Basically, interface timings should match the VESA 1024x768 / 60 Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

| Symbol | | MIN | TYP | MAX | Unit |
|--------|--------------------|-------|--------|-------|------|
| fdck | DTCLK Frequency | 50.00 | 65.00 | 67.00 | MHz |
| tck | DTCLK cycle time | 14.93 | 15.38 | 20.00 | nsec |
| tx | X total time | 1206 | 1344 | 2047 | tck |
| tacx | X active time | 1024 | 1024 | 1024 | tck |
| tblkx | X blank time | 90 | 320 | | tck |
| Hsync | H frequency | | 48.363 | | KHz |
| Hsw | H-Sync width | 2 | 136 | | tck |
| Hbp | H back porch | 1 | 160 | | tck |
| Hfp | H front porch | 0 | 24 | | tck |
| ty | Y total time | 771 | 806 | 1023 | tx |
| tacy | Y active time | 768 | 768 | 768 | tx |
| Vsync | Frame rate | (55) | 60 | 61 | Hz |
| Vw | V-sync Width | 1 | 6 | | tx |
| Vfp | V-sync front porch | 1 | 3 | | tx |
| Vbp | V-sync back porch | 7 | 29 | 63 | tx |

Note: Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

8.2 Timing Definition





9.0 Power Consumption

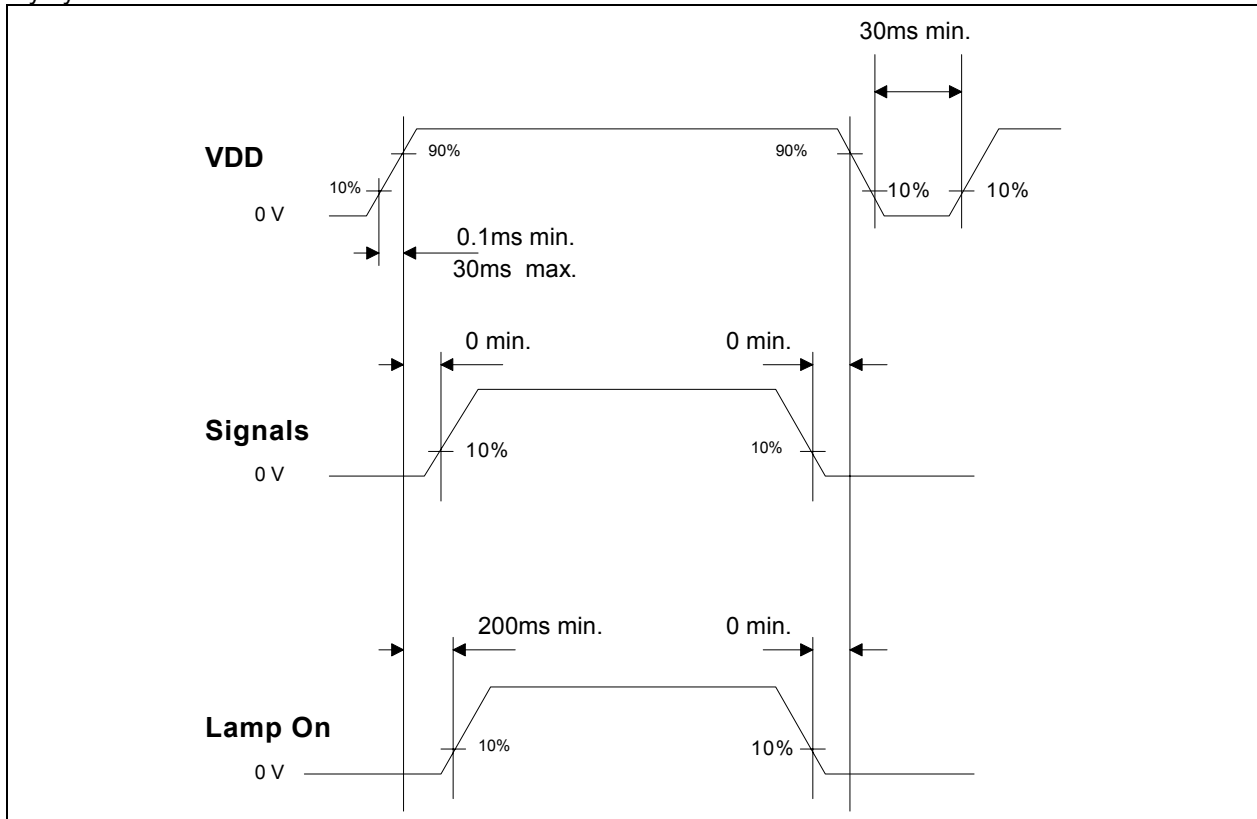
Input power specifications are as follows;

| SYMBOL | PARAMETER | Min | Typ | Max | UNITS | CONDITION |
|---------|------------------------------------------|-----|-----|-----|-------|-------------------------|
| VDD | Logic/LCD Drive Voltage | 3 | 3.3 | 3.6 | V | Load Capacitance 20uF |
| PDD | VDD Power | | 1.3 | | W | All Black Pattern |
| PDD Max | PDD max | | | 1.6 | W | Max Pattern Note |
| IDD | IDD Current | | 380 | | mA | All Black Pattern |
| IDD Max | IDD Current max | | | 480 | mA | Max Pattern Note |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | mVp-p | |
| VDDns | Allowable Logic/LCD Drive Ripple Noise | | | 100 | mVp-p | |

Note :VDD= 3.3 V

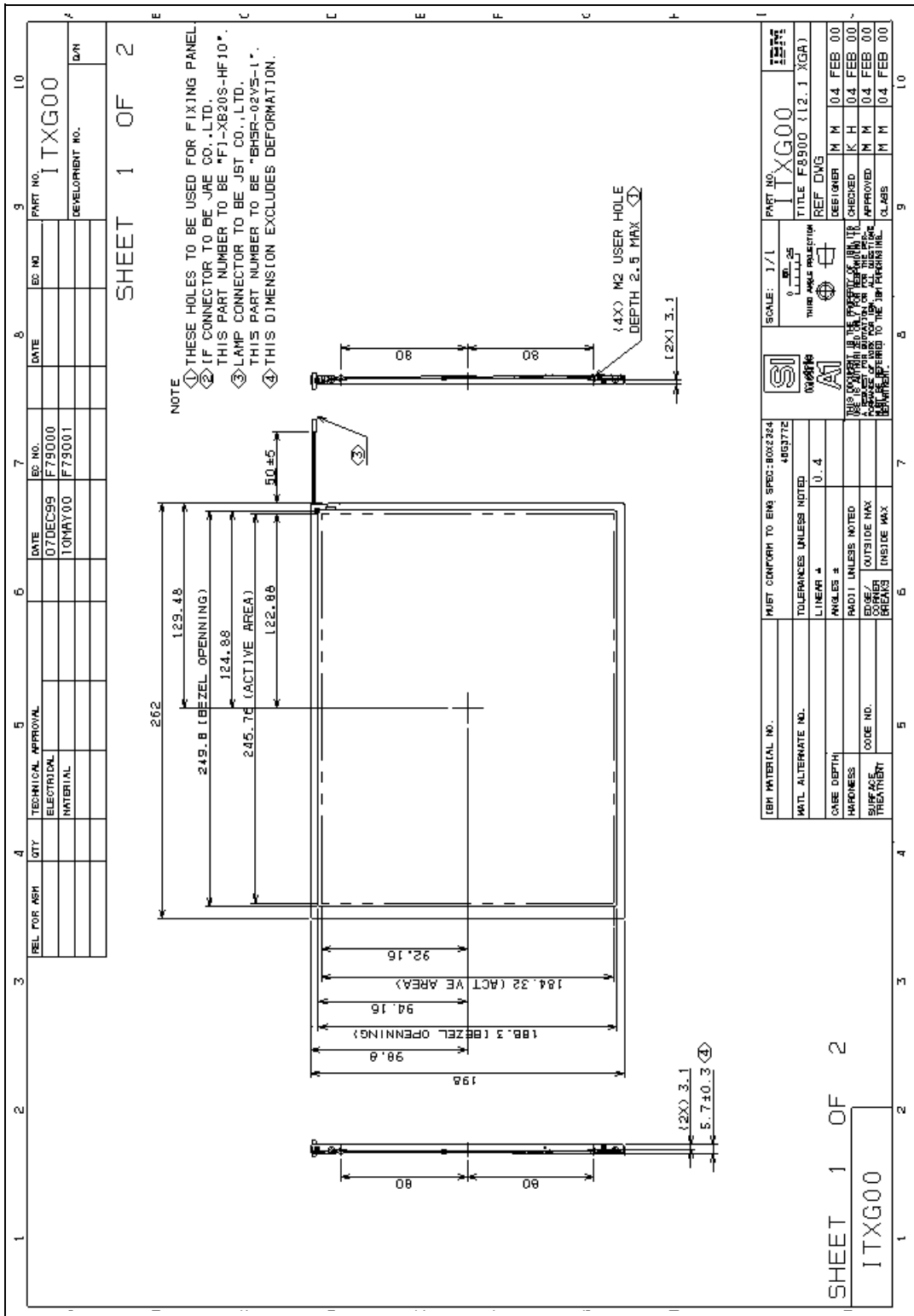
10.0 Power ON/OFF Sequence

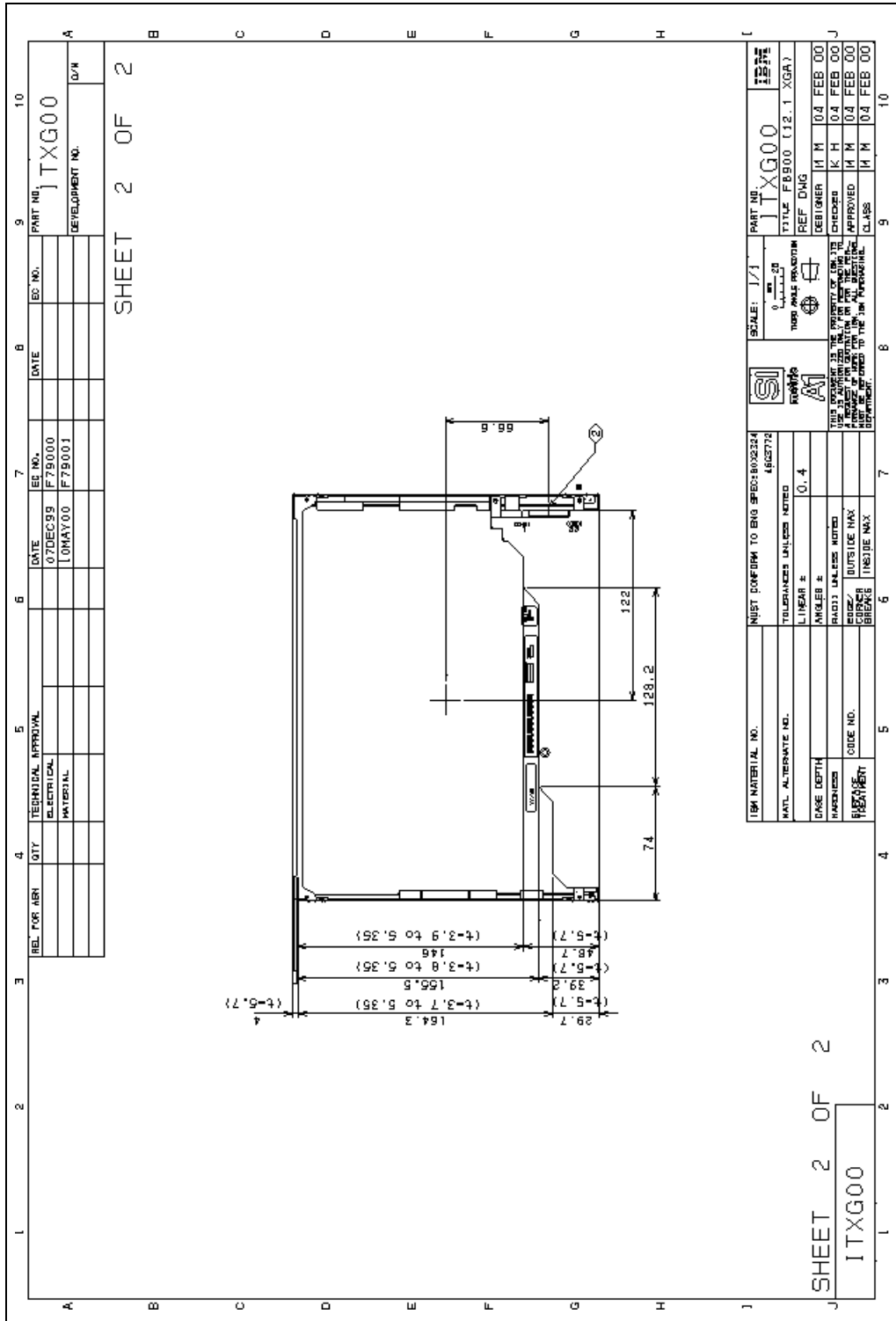
VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.





11.0 Mechanical Characteristics





SHEET 2 OF 2

SHEET 2 OF 2
ITXG00

12.0 National Test Lab Requirement

The display module satisfied all requirements for compliance to
UL 1950, 3rd Edition U.S.A. Information Technology Equipment

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