IV1Q12050T4 – 1200V 50mΩ SiC MOSFET

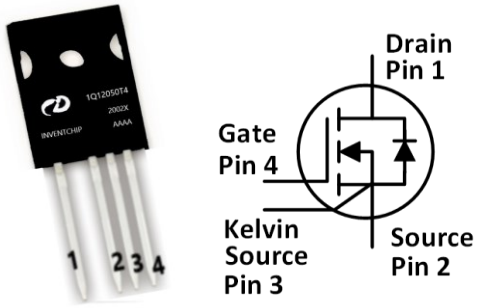
Features:

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design

Applications:

- Solar inverters
- UPS
- Motor drivers
- High voltage DC/DC converters
- Switch mode power supplies

Package:



Part Number	Package
IV1Q12050T4	TO247-4

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	1200	V	V_{GS}=0V, I_D=100μA	
V_{GS}	Gate-Source voltage	-5 to 20	V	Recommended maximum	
I_D	Drain current (continuous)	58	A	V_{GS}=20V, T_C=25°C	Fig. 21
		43	A	V_{GS}=20V, T_C=100°C	
I_{DM}	Drain current (pulsed)	145	A	Pulse width limited by SOA	Fig. 24
P_{TOT}	Total power dissipation	344	W	T_C=25°C	Fig. 22
T_{stg}	Storage temperature range	-55 to 175	°C		
T_J	Operating junction temperature	-55 to 175	°C		
T_L	Solder Temperature	260	°C	Wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{\theta(J-C)}$	Thermal Resistance from Junction to Case	0.436	°C/W	Fig. 23

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		5	100	μA	V_{DS}=1200V, V_{GS}=0V	
I_{GSS}	Gate leakage current		1	±100	nA	V_{DS}=0V, V_{GS}=-5~20V	
V_{TH}	Gate threshold voltage		3.2		V	V_{GS}=V_{DS}, I_D=6mA	Fig. 8, 9
			2.2			V_{GS}=V_{DS}, I_D=6mA @ T_C=175°C	
R_{ON}	Static drain-source on-resistance		50	65	mΩ	V_{GS}=20V, I_D=20A @T_J=25°C	Fig. 4, 5, 6, 7
			80		mΩ	V_{GS}=20V, I_D=20A @T_J=175°C	
C_{iss}	Input capacitance		2750		pF	V_{DS}=800V, V_{GS}=0V, f=1MHz, V_{AC}=25mV	Fig. 16
C_{oss}	Output capacitance		106		pF		
C_{rss}	Reverse transfer capacitance		5.2		pF		
E_{oss}	C_{oss} stored energy		43		μJ		Fig. 17
Q_g	Total gate charge		120		nC	V_{DS}=800V, I_D=20A, V_{GS}=-5 to 20V	Fig. 18
Q_{gs}	Gate-source charge		25		nC		
Q_{gd}	Gate-drain charge		48		nC		
R_g	Gate input resistance		2.8		Ω	f=1MHz	
E_{ON}	Turn-on switching energy		455.4		μJ	V_{DS}=800V, I_D=30A, V_{GS}=-2 to 20V, $R_{G(ext)}$=3.3Ω, L=450μH	Fig. 19, 20
E_{OFF}	Turn-off switching energy		213.6		μJ		
$t_{d(on)}$	Turn-on delay time		8.9		ns		
t_r	Rise time		28.9				
$t_{d(off)}$	Turn-off delay time		25.6				
t_f	Fall time		17.2				

Reverse Diode Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		4.9		V	I_{SD}=20A, V_{GS}=0V	Fig. 10, 11, 12
			4.4		V	I_{SD}=20A, V_{GS}=0V, T_J=175°C	
t_{rr}	Reverse recovery time		44.4		ns	V_{GS}=-2V/+20V, I_{SD}=30A, V_R=800V, di/dt=1000A/us, $R_{G(ext)}$=10Ω L=450μH	
Q_{rr}	Reverse recovery charge		212.6		nC		
I_{RRM}	Peak reverse recovery current		10.8		A		

Typical Performance (curves)

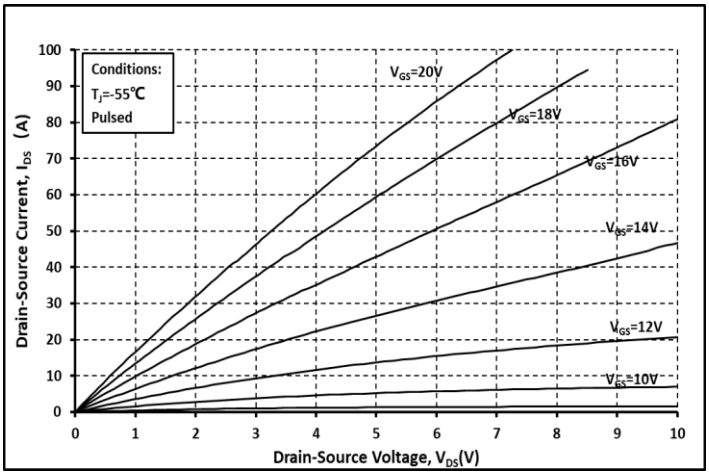


Fig. 1 Output Curve @ T_J=-55℃

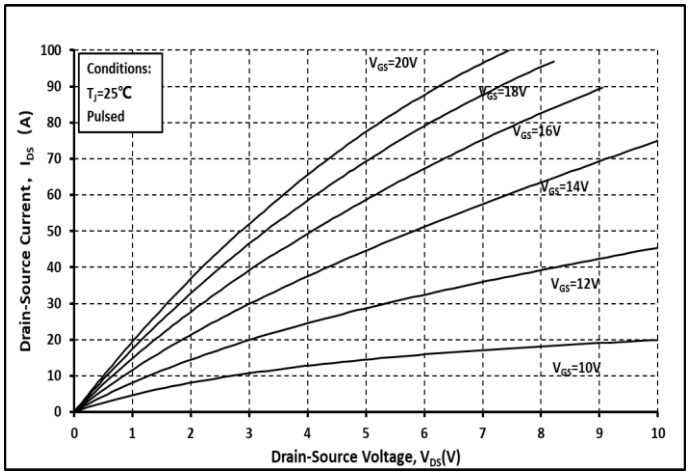


Fig. 2 Output Curve @ T_J=25℃

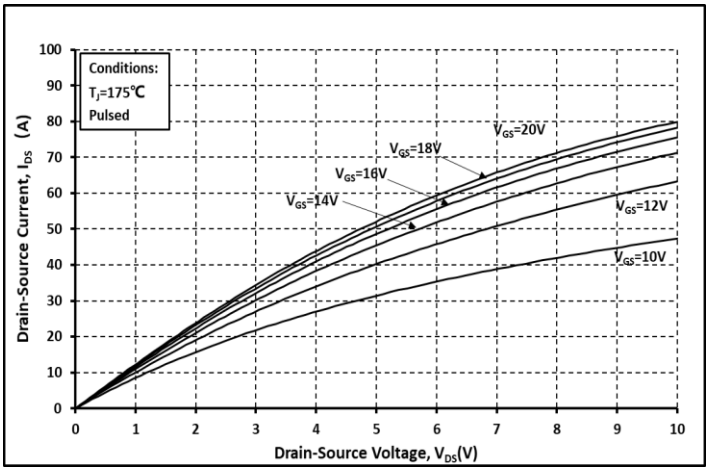


Fig. 3 Output Curve @ T_J=175℃

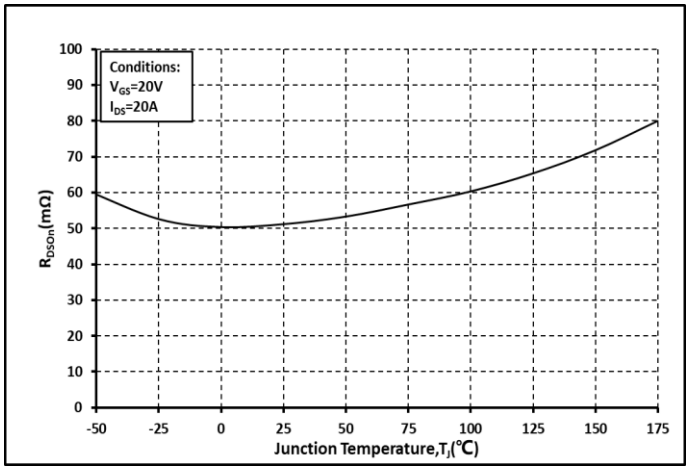


Fig. 4 Ron vs. Temperature

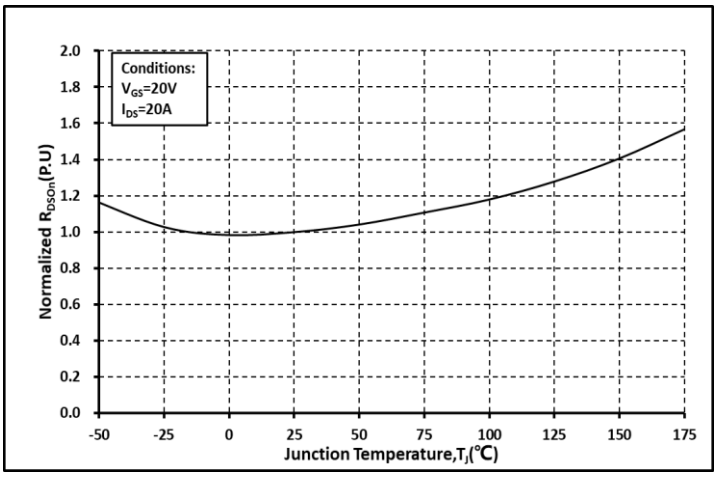


Fig. 5 Normalized Ron vs. Temperature

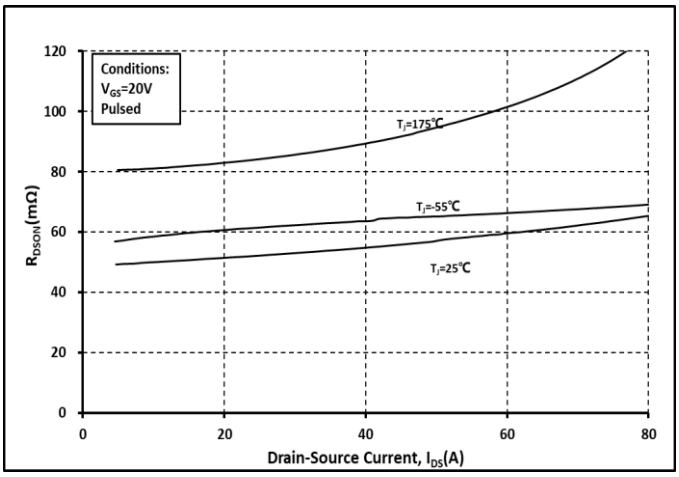


Fig. 6 Ron vs. I_{DS} @ Various Temperature

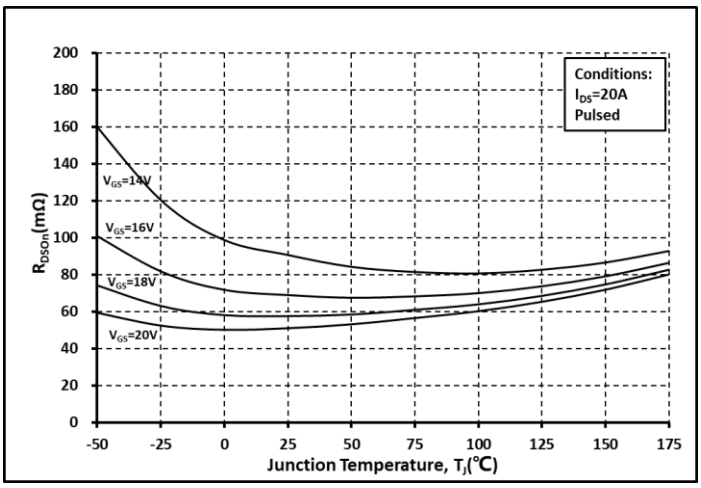


Fig. 7 Ron vs. Temperature @ Various V_{GS}

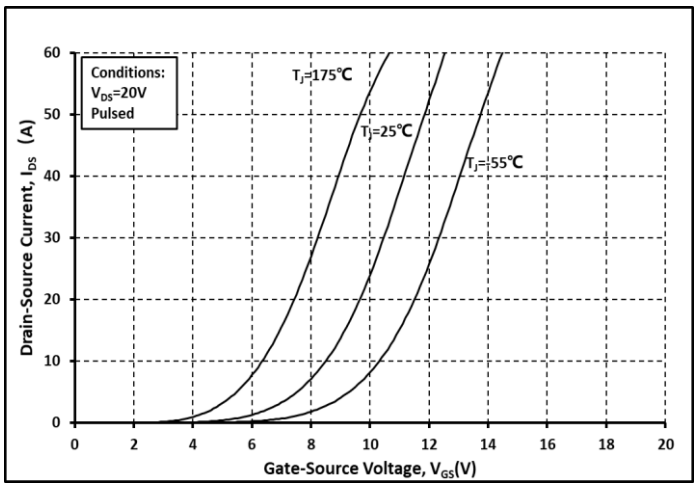


Fig. 8 Transfer Curves @ Various Temperature

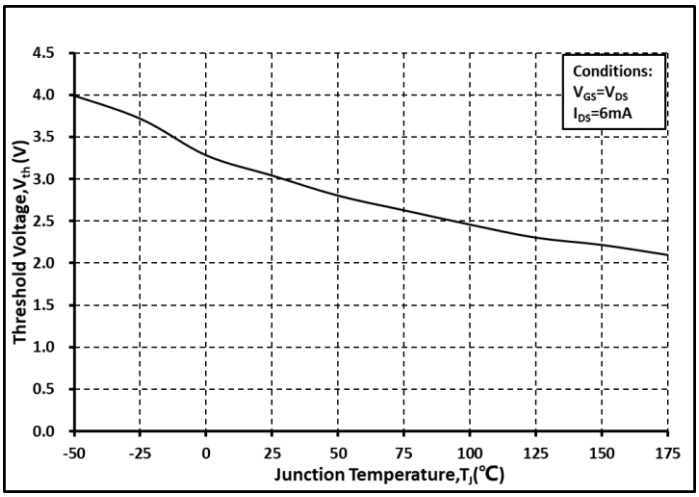


Fig. 9 Threshold Voltage vs. Temperature

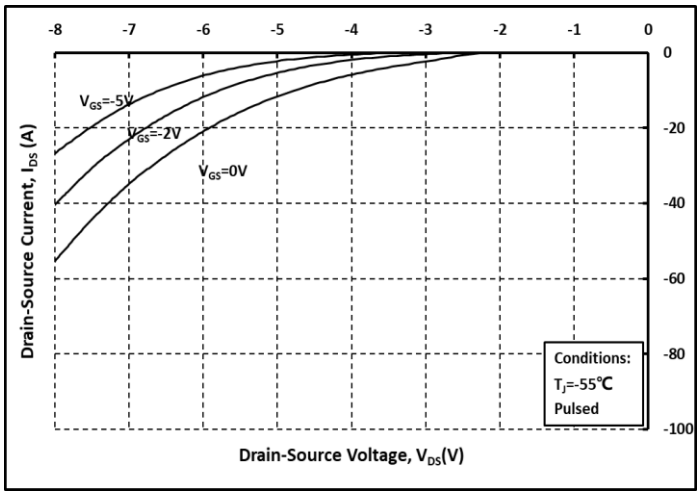


Fig. 10 Body Diode Curves @ T_J=-55°C

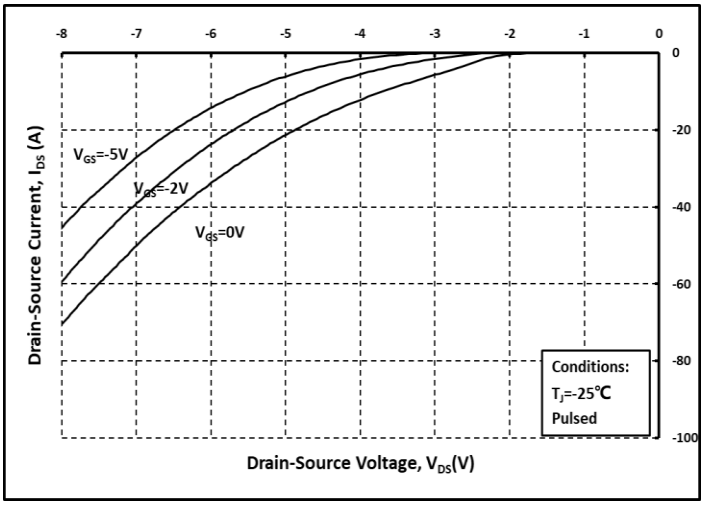


Fig. 11 Body Diode Curves @ T_J=25°C

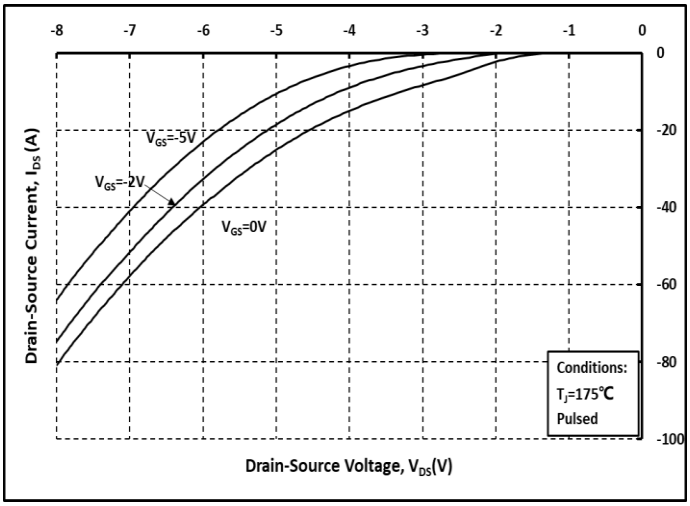


Fig. 12 Body Diode Curves @ T_J=175°C

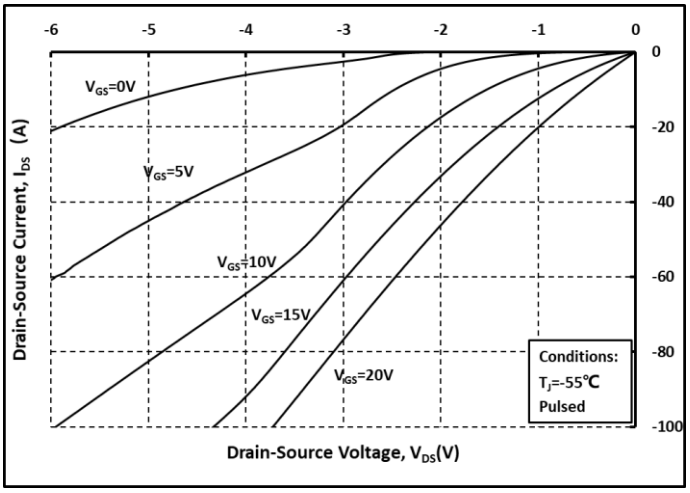


Fig. 13 3rd Quadrant Curves @ T_J=-55°C

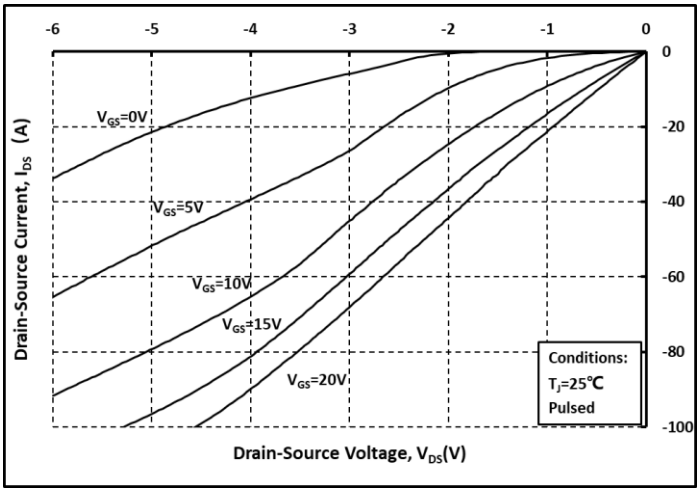


Fig. 14 3rd Quadrant Curves @ T_J=25°C

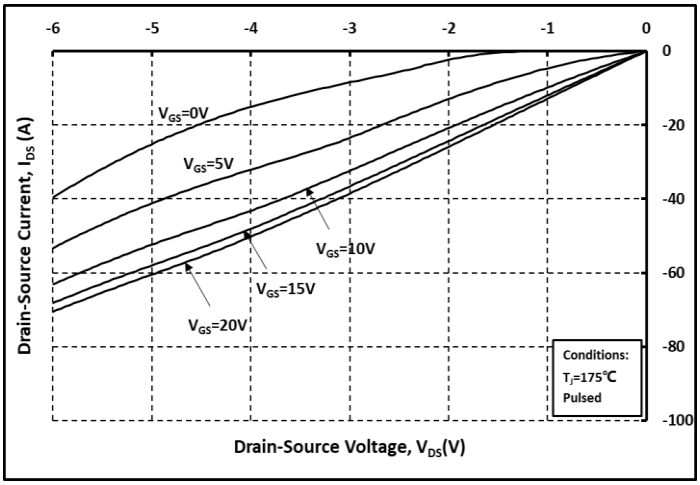


Fig. 15 3rd Quadrant Curves @ T_J=175°C

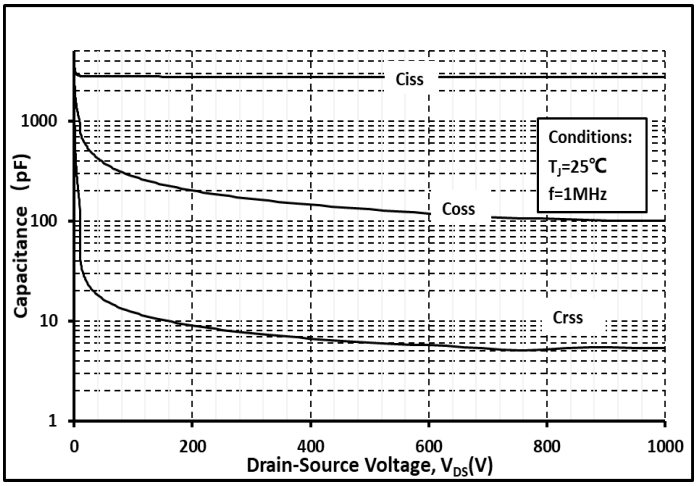


Fig. 16 Capacitance vs. V_{DS}

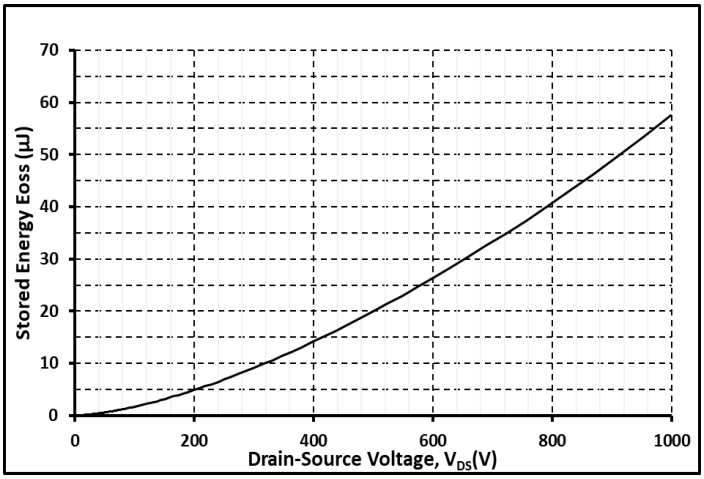


Fig. 17 Output Capacitor Stored Energy

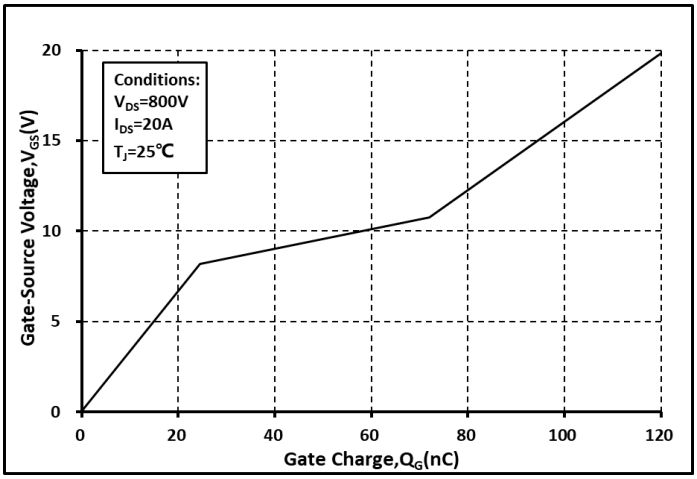


Fig. 18 Gate Charge Characteristics

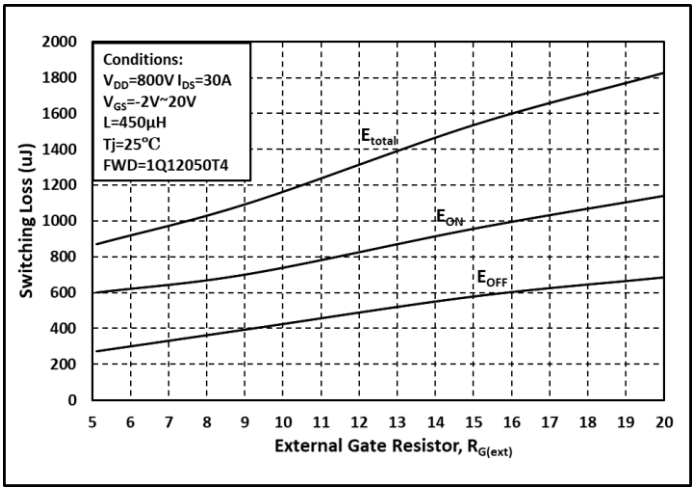


Fig. 19 Switching Energy vs. $R_{G(ext)}$

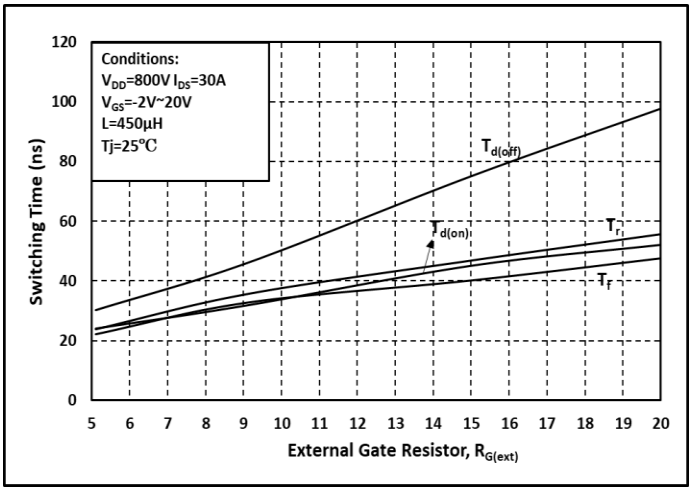


Fig. 20 Switching Times vs. $R_{G(ext)}$

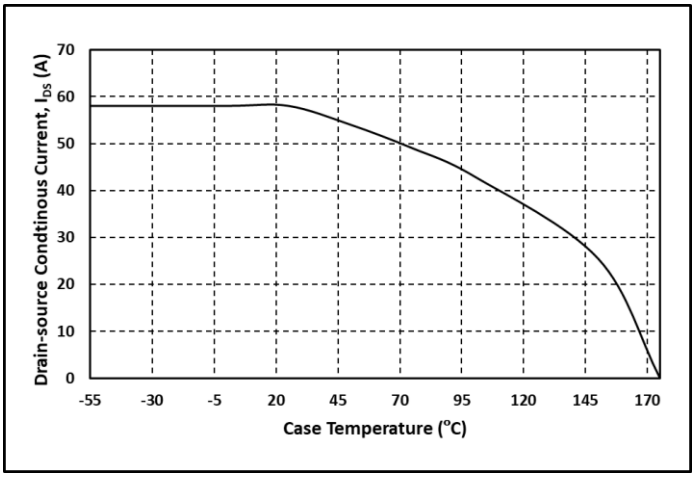


Fig. 21 Continuous Drain Current vs. Case Temperature

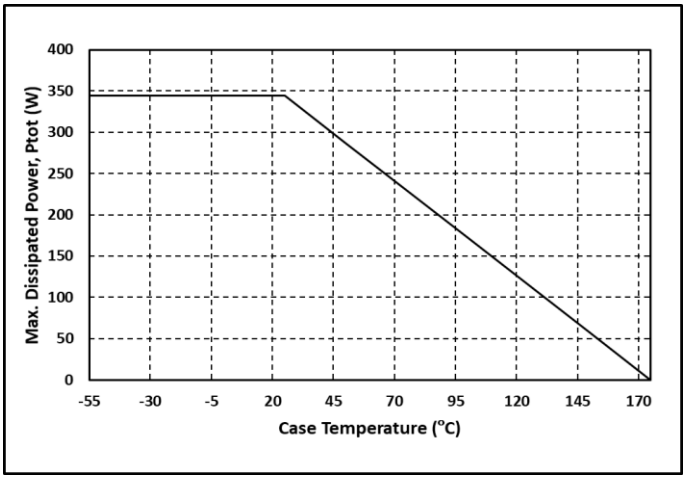


Fig. 22 Max. Power Dissipation Derating vs. Case Temperature

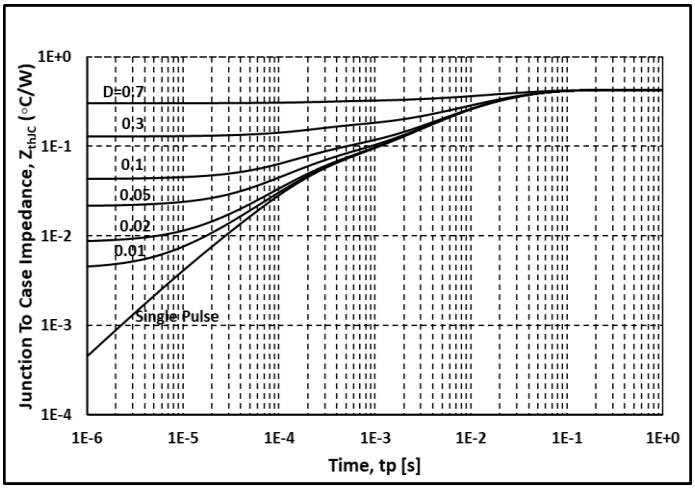


Fig. 23 Thermal Impedance

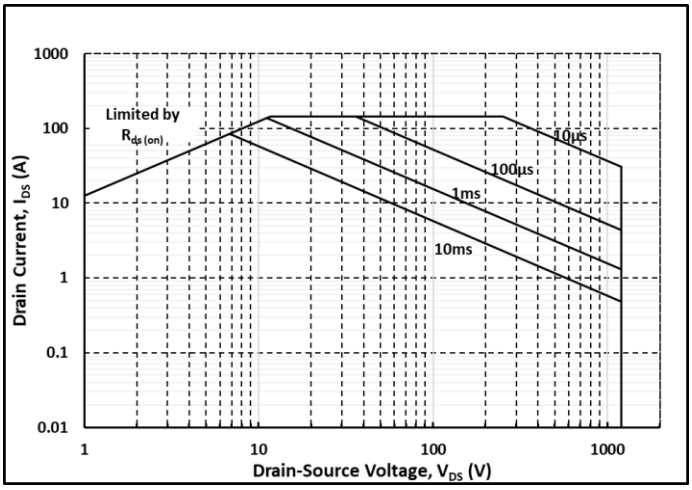
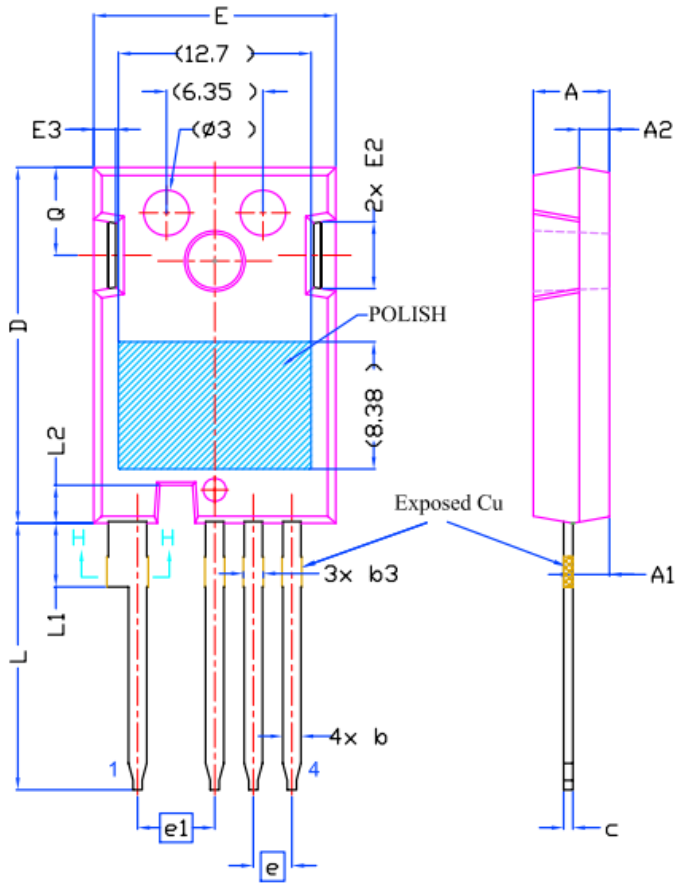
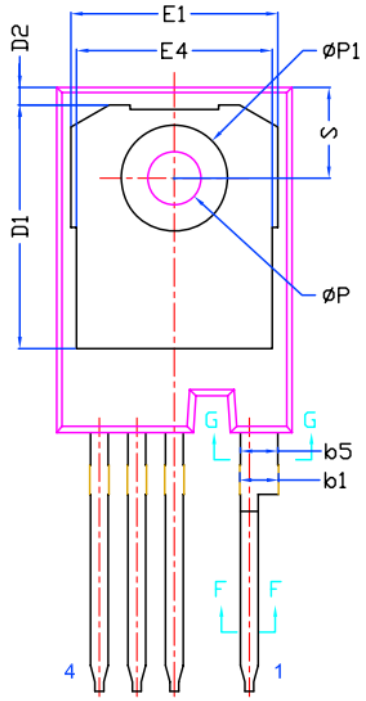
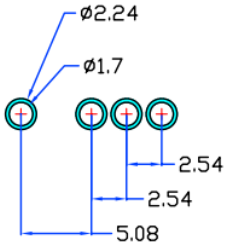


Fig. 24 Safe Operating Area

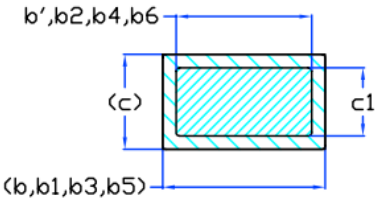
Package Dimensions







Recommended Solder Pad Layout



Section F--F, G--G, H--H

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
ØP	3.51	3.61	3.65
ØP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Note:

1. Package Reference: JEDEC TO247, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash

Notes

Current revision is preliminary one, for further information please contact IVCT's Office.

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