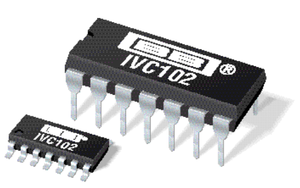


IVC102

PRECISION SWITCHED INTEGRATOR TRANSIMPEDANCE AMPLIFIER

APPLICATIONS

- PRECISION LOW CURRENT MEASUREMENT
- PHOTODIODE MEASUREMENTS
- IONIZATION CHAMBER MEASUREMENTS
- CURRENT/CHARGE-OUTPUT SENSORS
- LEAKAGE CURRENT MEASUREMENT

FEATURES

- ON-CHIP INTEGRATING CAPACITORS
- GAIN PROGRAMMED BY TIMING
- LOW INPUT BIAS CURRENT: 750fA max
- LOW NOISE
- LOW SWITCH CHARGE INJECTION
- FAST PULSE INTEGRATION
- LOW NONLINEARITY: 0.005% typ
- 14-PIN DIP, SO-14 SURFACE MOUNT

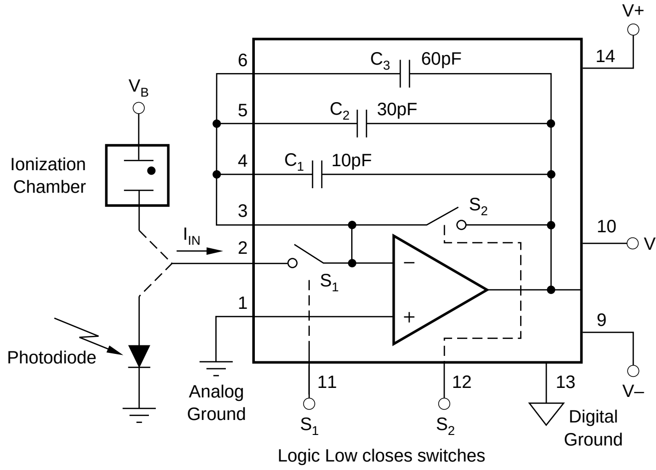
DESCRIPTION

The IVC102 is a precision integrating amplifier with FET op amp, integrating capacitors, and low leakage FET switches. It integrates low-level input current for a user-determined period, storing the resulting voltage on the integrating capacitor. The output voltage can be held for accurate measurement. The IVC102 provides a precision, lower noise alternative to conventional transimpedance op amp circuits that require a very high value feedback resistor.

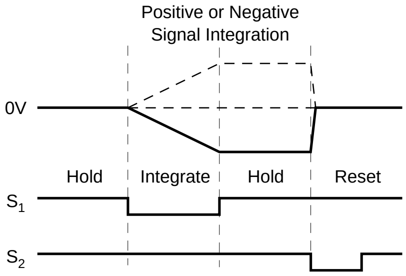
The IVC102 is ideal for amplifying low-level sensor currents from photodiodes and ionization chambers. The input signal current can be positive or negative.

TTL/CMOS-compatible timing inputs control the integration period, hold and reset functions to set the effective transimpedance gain and to reset (discharge) the integrator capacitor.

Package options include 14-Pin plastic DIP and SO-14 surface-mount packages. Both are specified for the –40°C to 85°C industrial temperature range.



$$V_O = \frac{-1}{C_{INT}}\int I_{IN}(t)\,dt$$



PDS-1329A
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SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, R_L = 2kΩ, $C_{INT} = C_1 + C_2 + C_3$, 1ms integration period(1), unless otherwise specified.

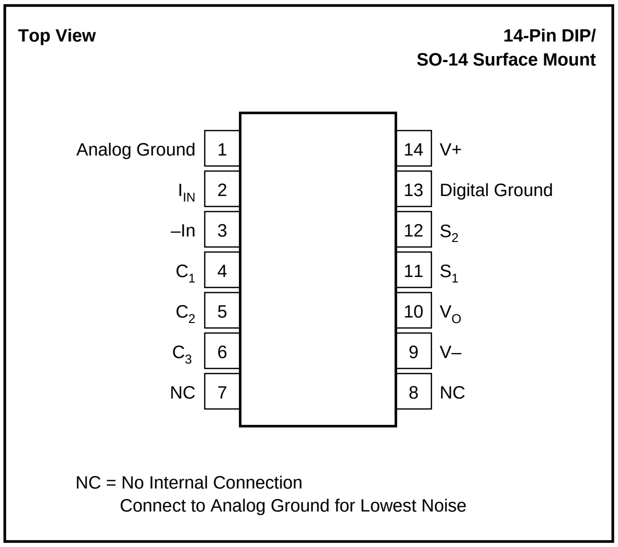
PARAMETER	CONDITIONS	IVC102P, U			UNITS
		MIN	TYP	MAX	
TRANSFER FUNCTION			$V_O = -(I_{IN})(T_{INT})/C_{INT}$		
Gain Error	$C_{INT} = C_1 + C_2 + C_3$		±5	+25/–17	%
vs Temperature			±25		ppm/°C
Nonlinearity	V_O = ±10V		±0.005		%
Input Current Range			±100		µA
Offset Voltage(2)	I_{IN} = 0, C_{IN} = 50pF		–5	±20	mV
vs Temperature			±30		µV/°C
vs Power Supply	V_S = +4.75/–10 to +18/–18V		150	750	µV/V
Droop Rate, Hold Mode			–1		nV/µs
OP AMP					
Input Bias Current	S_1, S_2 Open		–100	±750	fA
vs Temperature			See Typical Curve		
Offset Voltage (Op Amp V_{OS})			±0.5	±5	mV
vs Temperature			±5		µV/°C
vs Power Supply	V_S = +4.75/–10 to +18/–18V		10	100	µV/V
Noise Voltage	f = 1kHz		10		$nV/\sqrt{Hz}$
INTEGRATION CAPACITORS					
$C_1 + C_2 + C_3$		80	100	120	pF
vs Temperature			±25		ppm/°C
C_1			10		pF
C_2			30		pF
C_3			60		pF
OUTPUT					
Voltage Range, Positive	R_L = 2kΩ	(V+)–3	(V+)–1.3		V
Negative	R_L = 2kΩ	(V–)+3	(V–)+2.6		V
Short-Circuit Current			±20		mA
Capacitive Load Drive			500		pF
Noise Voltage			See Typical Curve		
DYNAMIC CHARACTERISTIC					
Op Amp Gain-Bandwidth			2		MHz
Op Amp Slew Rate			3		V/µs
Reset					
Slew Rate			3		V/µs
Settling Time, 0.01%	10V Step		6		µs
DIGITAL INPUTS	(TTL/CMOS Compatible)				
V_{IH} (referred to digital ground)	(Logic High)	2		5.5	V
V_{IL} (referred to digital ground)	(Logic Low)	–0.5		0.8	V
I_{IH}	V_{IH} = 5V		2		µA
I_{IL}	V_{IL} = 0V		0		µA
Switching Time			100		ns
POWER SUPPLY					
Voltage Range: Positive		+4.75	+15	+18	V
Negative		–10	–15	–18	V
Current: Positive			4.1	5.5	mA
Negative			–1.6	–2.2	mA
Analog Ground			–0.2		mA
Digital Ground			–2.3		mA
TEMPERATURE RANGE					
Operating Range		–40		85	°C
Storage		–55		125	°C
Thermal Resistance, θ_{JA}					
DIP			100		°C/W
SO-14			150		°C/W

NOTES: (1) Standard test timing: 1ms integration, 200µs hold, 100µs reset. (2) Hold mode output voltage after 1ms integration of zero input current. Includes op amp offset voltage, integration of input error current and switch charge injection effects.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Logic Input Voltage	V– to V+
Output Short Circuit to Ground	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	300°C

PIN CONNECTIONS



NC = No Internal Connection
Connect to Analog Ground for Lowest Noise

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
IVC102P	14-Pin DIP	010
IVC102U	SO-14 Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

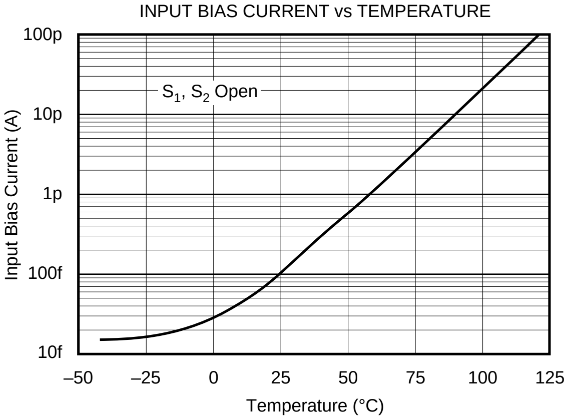
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

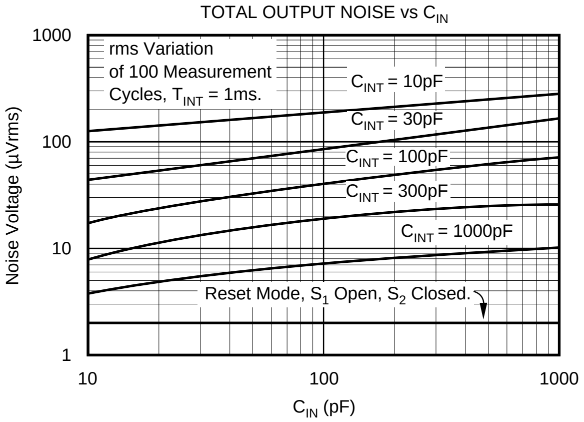
TYPICAL PERFORMANCE CURVES

At $T_A = +25°C$, $V_S = ±15V$, $R_L = 2kΩ$, $C_{INT} = C_1 + C_2 + C_3$, 1ms integration period, unless otherwise specified.

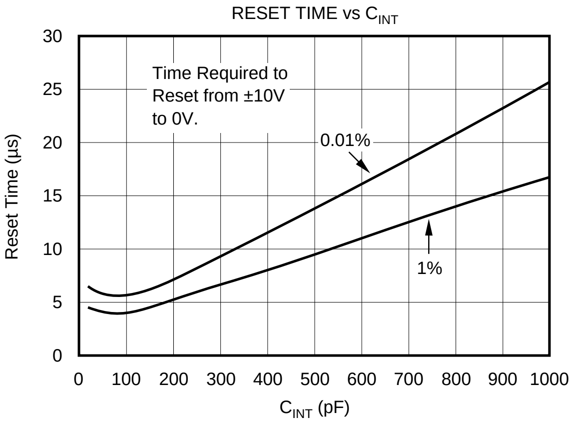
INPUT BIAS CURRENT vs TEMPERATURE



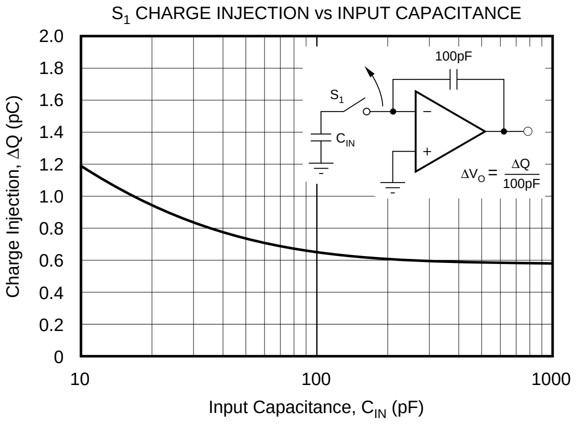
TOTAL OUTPUT NOISE vs C_{IN}



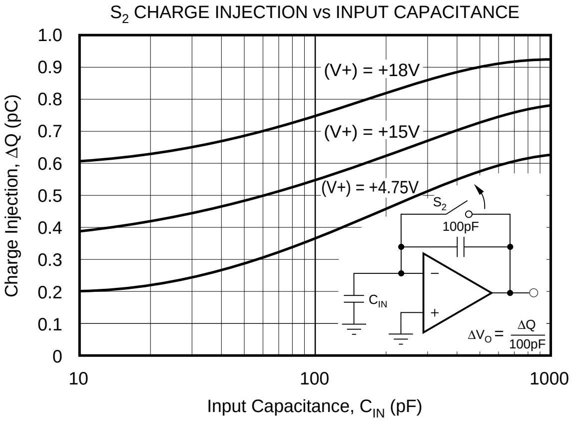
RESET TIME vs C_{INT}



S_1 CHARGE INJECTION vs INPUT CAPACITANCE



S_2 CHARGE INJECTION vs INPUT CAPACITANCE



APPLICATION INFORMATION

Figure 1 shows the basic circuit connections to operate the IVC102. Bypass capacitors are shown connected to the power supply pins. Noisy power supplies should be avoided or decoupled and carefully bypassed.

The Analog Ground terminal, pin 1, is shown internally connected to the non-inverting input of the op amp. This terminal connects to other internal circuitry and should be connected to ground. Approximately 200µA flows out of this terminal.

Digital Ground, pin 13, should be at the same voltage potential as analog ground (within 100mV). Analog and Digital grounds should be connected at some point in the system, usually at the power supply connections to the circuit board. A separate Digital Ground is provided so that noisy logic signals can be referenced to separate circuit board traces.

Integrator capacitors C_1, C_2 and C_3 are shown connected in parallel for a total C_{INT} = 100pF. The IVC102 can be used for a wide variety of integrating current measurements. The input signal connections and control timing and C_{INT} value will depend on the sensor or signal type and other application details.

BASIC RESET-AND-INTEGRATE MEASUREMENT

Figure 1 shows the circuit and timing for a simple reset-and-integrate measurement. The input current is connected directly to the inverting input of the IVC102, pin 3. Input current is shown flowing out of pin 3, which produces a positive-going ramp at V_O. Current flowing into pin 3 would produce a negative-going ramp.

A measurement cycle starts by resetting the integrator output voltage to 0V by closing S_2 for 10µs. Integration of the input current begins when S_2 opens and the input current begins to charge C_{INT}. V_O is measured with a sampling a/d converter at the end of an integration period, just prior to the next reset period. The ideal result is proportional to the average input current (or total accumulated charge).

Switch S_2 is again closed to reset the integrator output to 0V before the next integration period.

This simple measurement arrangement is suited to many applications. There are, however, limitations to this basic approach. Input current continues to flow through S_2 during the reset period. This leaves a small voltage on C_{INT} equal to the input current times R_{S2}, the on-resistance of S_2, approximately 1.5kΩ.

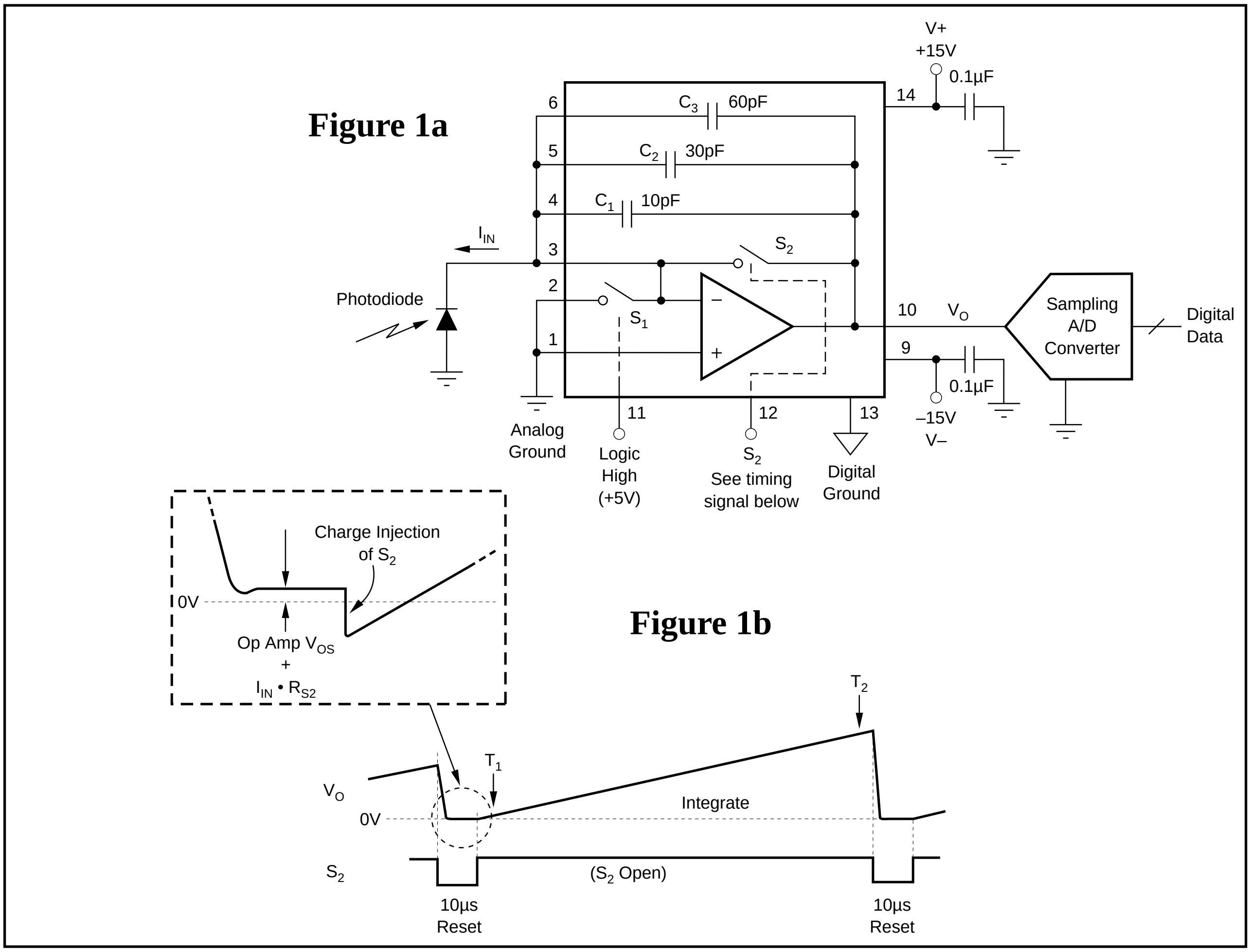


FIGURE 1. Reset-and Integrate Connections and Timing.

In addition, the offset voltage of the internal op amp and charge injection of S_2 contribute to the voltage on C_{INT} at the start of integration.

Performance of this basic approach can be improved by sampling V_O after the reset period at T_1 and subtracting this measurement from the final sample at T_2. Op amp offset voltage, charge injection effects and $I \cdot R_{S2}$ offset voltage on S_2 are removed with this two-point measurement. The effective integration period is the time between the two measurements, T_2-T_1.

COMPARISON TO CONVENTIONAL TRANSIMPEDANCE AMPLIFIERS

With the conventional transimpedance amplifier circuit of Figure 2a, input current flows through the feedback resistor, R_F, to create a proportional output voltage.

$$V_O = -I_{IN} R_F$$

The transimpedance gain is determined by R_F. Very large values of R_F are required to measure very small signal current. Feedback resistor values exceeding 100MΩ are common.

The IVC102 (Figure 2b) provides a similar function, converting an input current to an output voltage. The input current flows through the feedback capacitor, C_{INT}, charging it at a rate that is proportional to the input current. With a constant input current, the IVC102's output voltage is

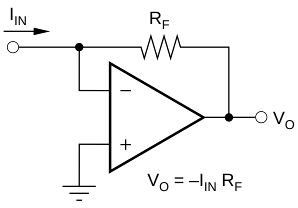
$$V_O = -I_{IN}\, T_{INT}/C_{INT}$$

after an integration time of T_{INT}.

V_O is proportional to the integration time, T_{INT}, and inversely proportional to the feedback capacitor, C_{INT}. The effective transimpedance gain is T_{INT}/C_{INT}. Extremely high gain that would be impractical to achieve with a conventional transimpedance amplifier can be achieved with small integration capacitor values and/or long integration times. For example the IVC102 with C_{INT} = 100pF and T_{INT} = 100ms provides an effective transimpedance of 1GΩ. A 10nA input current would produce a 10V output after 100ms integration.

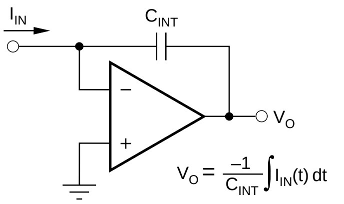
The integrating behavior of the IVC102 reduces noise by averaging the input noise of the sensor, amplifier, and external sources.

Conventional Transimpedance Amplifier
Figure 2a



Provides time-continuous output voltage proportional to I_{IN}.

Integrating Transimpedance Amplifier
Figure 2b



$$V_O = \frac{-1}{C_{INT}} \int I_{IN}(t)\, dt$$

for constant I_{IN}, at the end of T_{INT}

$$V_O = -I_{IN} \frac{T_{INT}}{C_{INT}}$$

Output voltage after integration period is proportional to average I_{IN} throughout the period.

FIGURE 2. Comparison to a Conventional Transimpedance Amplifier.

CURRENT-OUTPUT SENSORS

Figure 3 shows a model for many current-output sensors such as photodiodes and ionization chambers. Sensor output is a signal-dependent current with a very high source resistance. The output is generally loaded into a low impedance so that the terminal voltage is kept very low. Typical sensor capacitance values range from 10pF to over 100pF. This capacitance plays a key role in operation of the switched-input measurement technique (see next section).

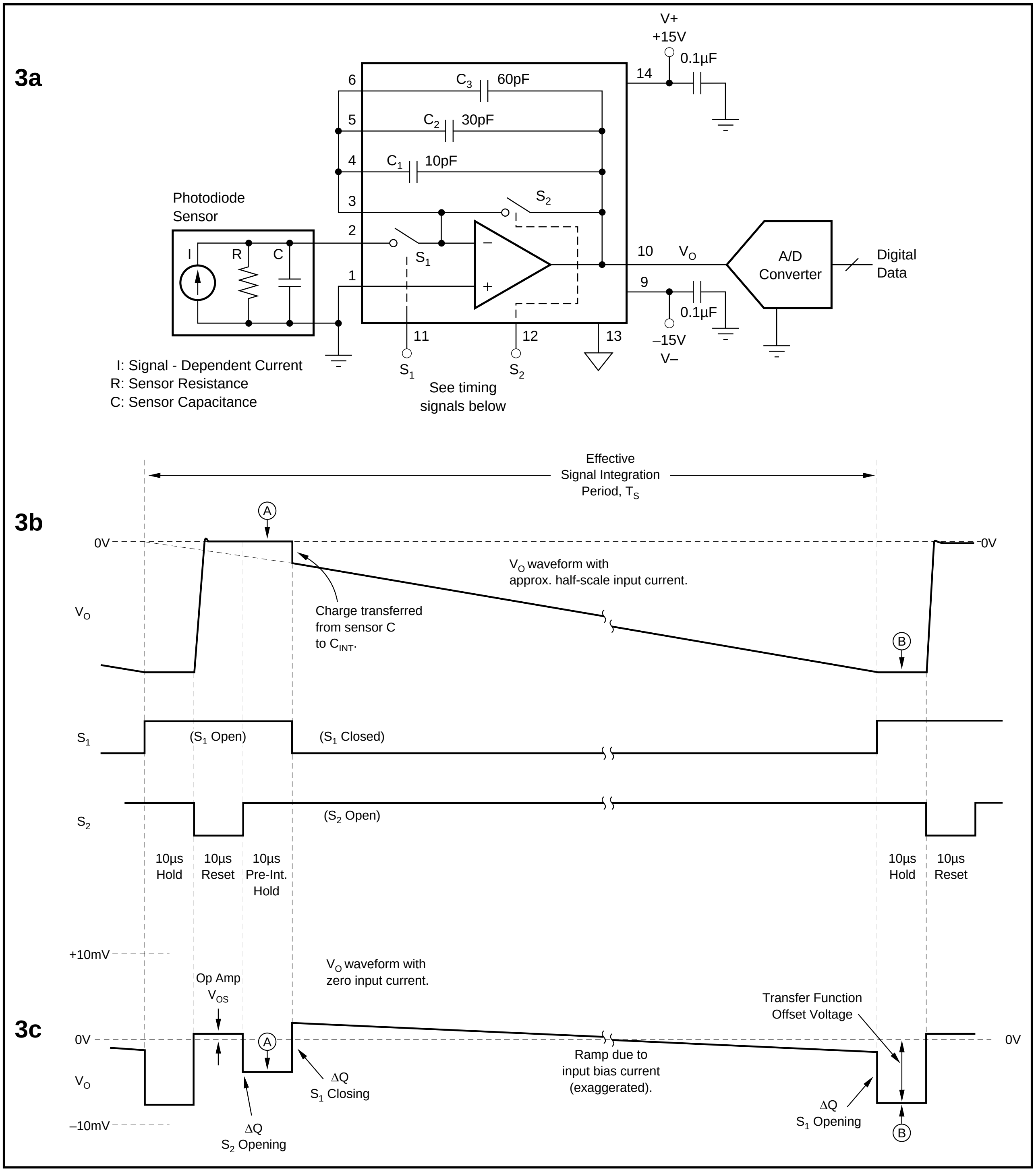


FIGURE 3. Switched-Input Measurement Technique.

SWITCHED-INPUT MEASUREMENT TECHNIQUE

While the basic reset-and-integrate measurement arrangement in Figure 1 is satisfactory for many applications, the switched-input timing technique shown in Figure 3 has important advantages. This method can provide continuous integration of the input signal. Furthermore, it can hold the output voltage constant after integration for stable conversion (desirable for a/d converter without a sample/hold). Input connections and timing are shown in Figure 3.

The timing diagram, Figure 3b, shows that S_1 is closed only when S_2 is open. During the short period that S_1 is open (30µs in this timing example), any signal current produced by the sensor will charge the sensor's source capacitance. This charge is then transferred to C_{INT} when S_1 is closed. As a result, no charge produced by the sensor is lost and the input signal is continuously integrated. Even fast input pulses are accurately integrated.

The input current, I_{IN}, is shown as a conventional current flowing into pin 2 in this diagram but the input current could be bipolar (positive or negative). Current flowing out of pin 2 would produce a positive-ramping V_O.

The timing sequence proceeds as follows:

Reset Period

The integrator is reset by closing switch S_2 with S_1 open. A 10µs reset time is recommended to allow the op amp to slew to 0V and settle to its final value.

Pre-Integration Hold

S_2 is opened, holding V_O constant for 10µs prior to integration. This pre-integration hold period assures that S_2 is fully open before S_1 is closed so that no input signal is lost. A minimum of 1µs is recommended to avoid switching overlap. The 10µs hold period shown in Figure 3b also allows an a/d converter measurement to be made at point A. The purpose of this measurement at A is discussed in the "Offset Errors" section.

Integration on C_{INT}

Integration of the input current on C_{INT} begins when S_1 is closed. An immediate step output voltage change occurs as the charge that was stored on the input sensor capacitance is transferred to C_{INT}. Although this period of charging C_{INT} occurs only while S_1 is closed, the charge transferred as S_1 is closed causes the *effective* integration time to be equal to the complete conversion period—see Figure 3b.

The integration period could range from 100µs to many minutes, depending on the input current and C_{INT} value. While S_1 is closed, I_{IN} charges C_{INT}, producing a negative-going ramp at the integrator output voltage, V_O. The output voltage at the end of integration is proportional to the average input current throughout the complete conversion cycle, including the integration period, reset and both hold periods.

Hold Period

Opening S_1 halts integration on C_{INT}. Approximately 5µs after S_1 is opened, the output voltage is stable and can be measured (at point B). The hold period is 10µs in this example. C_{INT} remains charged until a S_2 is again closed, to reset for the next conversion cycle.

In this timing example, S_1 is open for a total of 30µs. During this time, signal current from the sensor charges the sensor source capacitance. Care should be used to assure that the voltage developed on the sensor does not exceed approximately 200mV during this time. The I_{IN} terminal, pin 2, is internally clamped with diodes. If these diodes forward bias, signal current will flow to ground and will not be accurately integrated.

A maximum of 333nA signal current could be accurately integrated on a 50pF sensor capacitance for 30µs before 200mV would be developed on the sensor.

$$I_{MAX} = (50pF)\ (200mV) / 30\mu s = 333nA$$

OFFSET ERRORS

Figure 3c shows the effect on V_O due to op amp input offset voltage, input bias current and switch charge injection. It assumes zero input current from the sensor. The various offsets and charge injection (ΔQ) jumps shown are typical of that seen with a 50pF source capacitance. The specified "transfer function offset voltage" is the voltage measured during the hold period at B. Transfer function offset voltage is dominated by the charge injection of S_2 opening and op amp V_{OS}. The opening and closing charge injections of S_1 are very nearly equal and opposite and are not significant contributors.

Note that using a two-point difference measurement at A and B can dramatically reduce offset due to op amp V_{OS} and S_2 charge injection. The remaining offset with this B-A measurement is due to op amp input bias current charging C_{INT}. This error is usually very small and is exaggerated in the figure.

DIGITAL SWITCH INPUTS

The digital control inputs to S_1 and S_2 are compatible with standard CMOS or TTL logic. Logic input pins 11 and 12 are high impedance and the threshold is approximately 1.4V relative to Digital Ground, pin 13. A logic "low" closes the switch.

Use care in routing these logic signals to their respective input pins. Capacitive coupling of logic transitions to sensitive input nodes (pins 2 through 6) and to the positive power supply (pin 14) will dramatically increase charge injection and produce errors. Route these circuit board traces over a ground plane (digital ground) and route digital ground traces between logic traces and other critical traces for lowest charge injection. See Figure 4.

5V logic levels are generally satisfactory. Lower voltage logic levels may help reduce charge injection errors, depending on circuit layout. Logic high voltages greater than 5.5V, or higher than the V+ supply are not recommended.

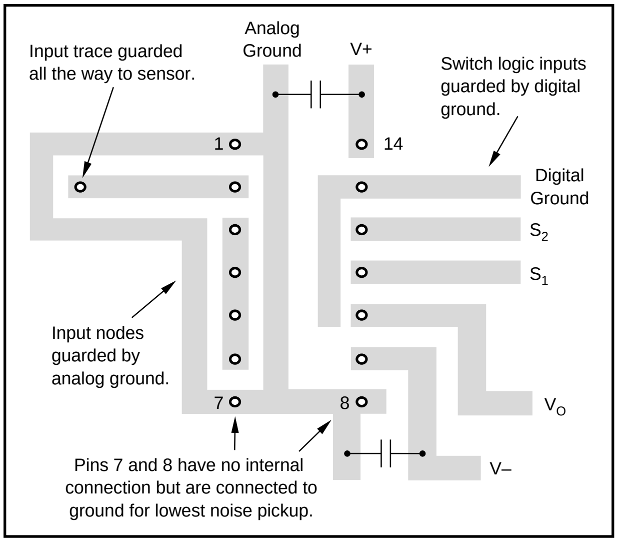


FIGURE 4. Circuit Board Layout Techniques.

INPUT BIAS CURRENT ERRORS

Careful circuit board layout and assembly techniques are required to achieve the very low input bias current capability of the IVC102. The critical input connections are at ground potential, so analog ground should be used as a circuit board guard trace surrounding all critical nodes. These include pins 2, 3, 4, 5 and 6. See Figure 4.

Input bias current increases with temperature—see typical performance curve Input Bias Current vs Temperature.

HOLD MODE DROOP

Hold-mode droop is a slow change in output voltage primarily due to op amp input bias current. Droop is specified using the internal C_{INT} = 100pF and is based on a –100fA typical input bias current. Current flows out of the inverting input of the internal op amp.

$$\text{Droop Rate} = \frac{-100\text{fA}}{C_{INT}}$$

With C_{INT} = 100pF, the droop rate is typically only 1nV/µs—slow enough that it rarely contributes significant error at moderate temperatures.

Since the input bias current increases with temperature, the droop rate will also increase with temperature. The droop rate will approximately double for each 10°C increase in junction temperature—see typical curves.

Droop rate is inversely proportional to C_{INT}. If an external integrator capacitor is used, a low leakage capacitor should be selected to preserve the low droop performance of the IVC102.

INPUT CURRENT RANGE

Extremely low input currents can be measured by integrating for long periods and/or using a small value for C_{INT}. Input bias current of the internal op amp is the primary source of error.

Larger input currents can be measured by increasing the value of C_{INT} and/or using a shorter integration time. Input currents greater than 200µA should not be applied to the pin 2 input, however. The approximately 1.5kΩ series resistance of S_1 will create an input voltage at pin 2 that will begin to forward-bias internal protection clamp diodes. Any current that flows through these protection diodes will not be accurately integrated. See "Input Impedance" section for more information on input current-induced voltage.

Input current greater than 200µA can, however, be connected directly to pin 3, using the simple reset-integrate technique shown in Figure 1. Current applied at this input can be externally switched to avoid excessive I•R voltage across S_2 during reset. Inputs up to 5mA at pin 3 can be accurately integrated if C_{INT} is made large enough to limit slew rate to less than 1V/µs. A 5mA input current would require C_{INT} = 5nF to produce a 1V/µs slew rate. The input current appears as load current to the internal op amp, reducing its ability to drive an external load.

CHOOSING C_{INT}

Internal capacitors C_1, C_2 and C_3 are high quality metal/oxide types with low leakage and excellent dielectric characteristics. Temperature stability is excellent—see typical curve. They can be connected for C_{INT} = 10pF, 30pF, 40pF, 60pF, 70pF, 90pF or 100pF. Connect unused internal capacitor pins to analog ground. Accuracy is ±20%, which directly influences the gain of the transfer function.

A larger value external C_{INT} can be connected between pins 3 and 10 for slower/longer integration. Select a capacitor type with low leakage and good temperature stability. Teflon®, polystyrene or polypropylene capacitors generally provide excellent leakage, temperature drift and voltage coefficient characteristics. Lower cost types such as NPO ceramic, mica or glass may be adequate for many applications. Larger values for C_{INT} require a longer reset time—see typical curves.

FREQUENCY RESPONSE

Integration of the input signal for a fixed period produces a deep null (zero response) at the frequency $1/T_{INT}$ and its harmonics. An ac input current at this frequency (or its harmonics) has zero average value and therefore produces no output. This property can be used to position response nulls at critical frequencies. For example, a 16.67ms integration period produces response nulls at 60Hz, 120Hz, 180Hz, etc., which will reject ac line frequency noise and its harmonics. Response nulls can be positioned to reduce interference from system clocks or other periodic noise.

Response to all frequencies above $f = 1/T_{INT}$ falls at –20dB/decade. The effective corner frequency of this single-pole response is approximately $1/2.8T_{INT}$.

For the simple reset-and-integrate measurement technique, T_{INT} is equal to the to the time that S_2 is open. The switched-input technique, however, effectively integrates the input signal throughout the full measurement cycle, including the reset period and both hold periods. Using the timing shown in Figure 3, the *effective* integration time is 1/Ts, where Ts is the repetition rate of the sampling.

INPUT IMPEDANCE

The input impedance of a perfect transimpedance circuit is zero ohms. The input voltage ideally would be zero for any input current. The actual input voltage when directly driving the integrator input (pin 3) is proportional to the output slew rate of the integrator. A 1V/µs slew rate produces approximately 100mV at pin 3. The input of the integrator can be modeled as a resistance:

$$R_{IN} = 10^{-7}/C_{INT} \tag{2}$$

with R_{IN} in Ω and C_{INT} in Farads.

Using the internal $C_{INT} = C_1 + C_2 + C_3 = 100\text{pF}$ (3)

$$R_{IN} = 10^{-7}/100\text{pF} = 1\text{k}\Omega$$

Teflon® E. I. Du Pont de Nemours & Co.

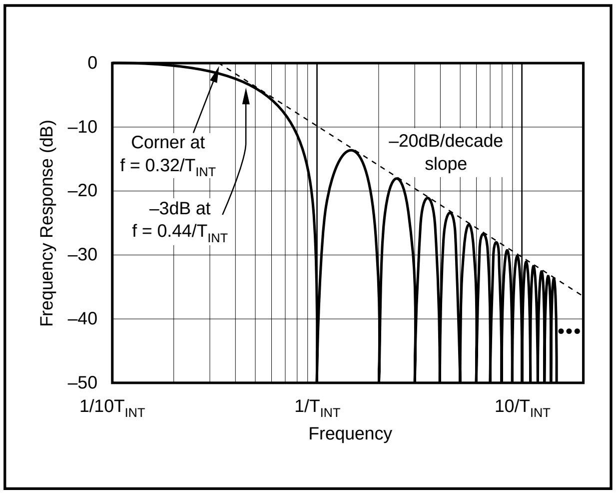


FIGURE 5. Frequency Response of Integrating Converter.

The input resistance seen at pin 2 includes an additional 1.5kΩ, the on-resistance of S_1. The total input resistance is the sum of the switch resistance and R_{IN}, or 2.5kΩ in this example.

Slew rate limit of the internal op amp is approximately 3V/µs. For most applications, the slew rate of V_{OUT} should be limited to 1V/µs or less. The rate of change is proportional to I_{IN} and inversely proportional to C_{INT}:

$$\text{Slew Rate} = \frac{I_{IN}}{C_{INT}}$$

This can be important in some applications since the slew-induced input voltage is applied to the sensor or signal source. The slew-induced input voltage can be reduced by increasing C_{INT}, which reduces the output slew rate.

NONLINEARITY

Careful nonlinearity measurements of the IVC102 yield typical results of approximately ±0.005% using the internal input capacitors (C_{INT} = 100pF). Nonlinearity will be degraded by using an external integrator capacitor with poor voltage coefficient. Performance with the internal capacitors is typically equal or better than the sensors it is used to measure. Actual application circuits with sensors such as a photodiode may have other sources of nonlinearity.