16-Channel LED Driver for LCD Panel Backlighting

1.0 Features

- 16-channel LED driver, 60V (max) per channel
- V_{IN}: 9V to 28V
- Fully-integrated current-sink FETs with minimum external components
- Two dynamic external boost or buck controller interfaces to optimize system power efficiency
- Patented BroadLED™ digital adaptive switch mode technology for high current matching at maximum efficiency
  - » Channel-to-channel matching accuracy ±2%
  - » Enables use of cheaper, loosely binned LED arrays for lower BOM cost
- High-speed PWM dimming via SPI interface
  - » High-bandwidth PWM-based dynamic local dimming
  - » PLL-locked VSYNC synchronized PWM
  - » Dimming range: 1% to 99.9%, 12-bit resolution
  - » Dimming frequency support for NTSC, PAL and 3D game modes with 5-bit programmability in normal mode (controlled by SPI dimming interface)
- Direct and unsynchronized dimming via external PWM
- Per-channel current
  - » Up to 150mA average
  - » Up to 240mA peak
- Comprehensive protection features:
  - » LED open and short-circuit fault protection
  - » Over-temperature shutdown
- 48-lead QFN-7m-48L package

2.0 Description

The iW7023 is a high efficiency driver for LEDs. It is designed for use with mid-size LCD panels that use arrays of LEDs as a backlight source. It is able to communicate with up to one external step-up or step-down PWM DC-DC converter to drive up to 16 separate strings of multiple series-connected LEDs.

The iW7023 features dynamic output voltage control, which automatically chooses the lowest active LED source voltage to adjust the feedback voltage of a step-up or step-down converter. Through this function, the iW7023 is able to dynamically adjust the output voltage of up to two external step-up or step-down converters to optimize the system power efficiency.

The iW7023 also provides 16 constant current sinks with maximum ±2% current matching. The LED PWM dimming can be adjusted dynamically through a high bandwidth SPI interface, which provides users flexibility to control the light intensity of LEDs. In addition, users can provide versatile configurations of the iW7023 through SPI interface registers.

The iW7023 can maintain very high efficiency even with the existence of LED channel total forward voltage mismatch, with the proprietary digital power management and patent pending adaptive switch mode LED current regulation technology.

The iW7023 has multiple features to protect the LED channels from fault conditions, and these protections are LED PWM cycle-by-cycle based to ensure system reliability and provide consistent operation.

3.0 Applications

- Direct & Segment-Edge LED Backlit LCD TV
- Edge Type global dimming LED backlit LCD TV
- Medical, Industrial Monitors and Public Displays

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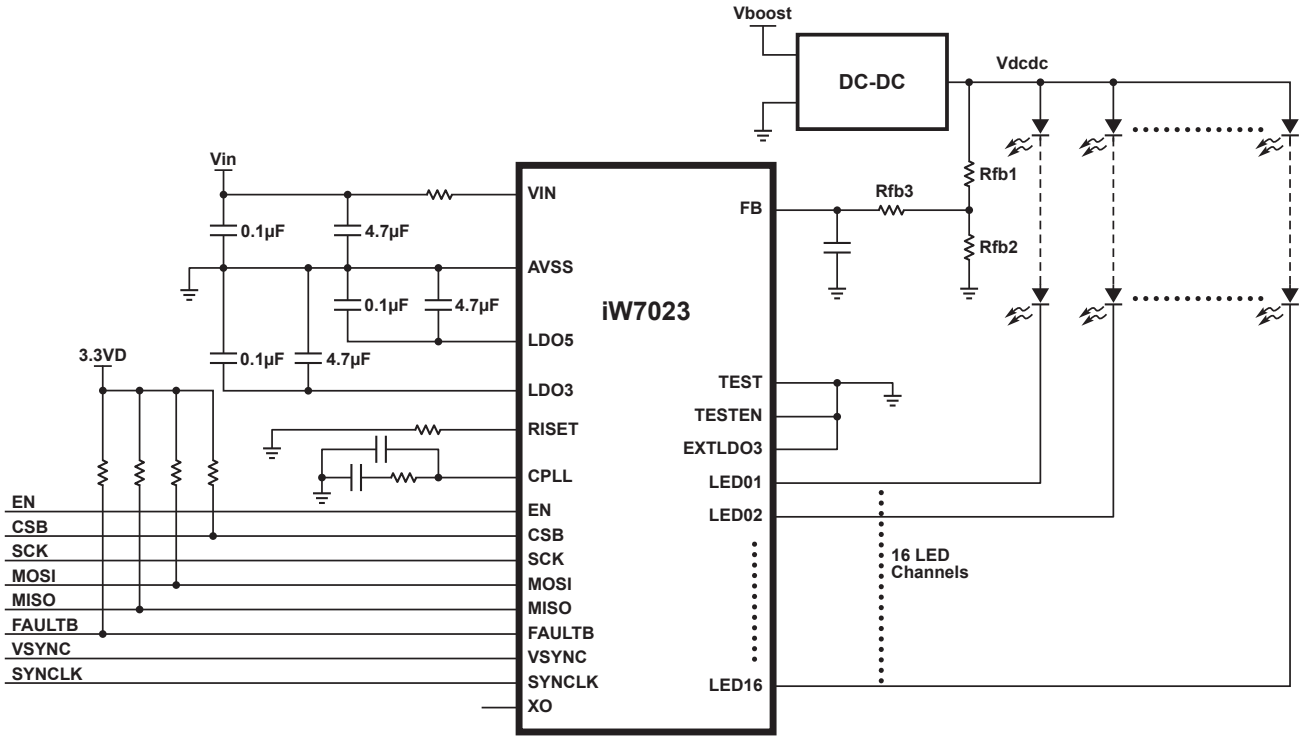

Figure 3.1: iW7023 Typical Application Schematic

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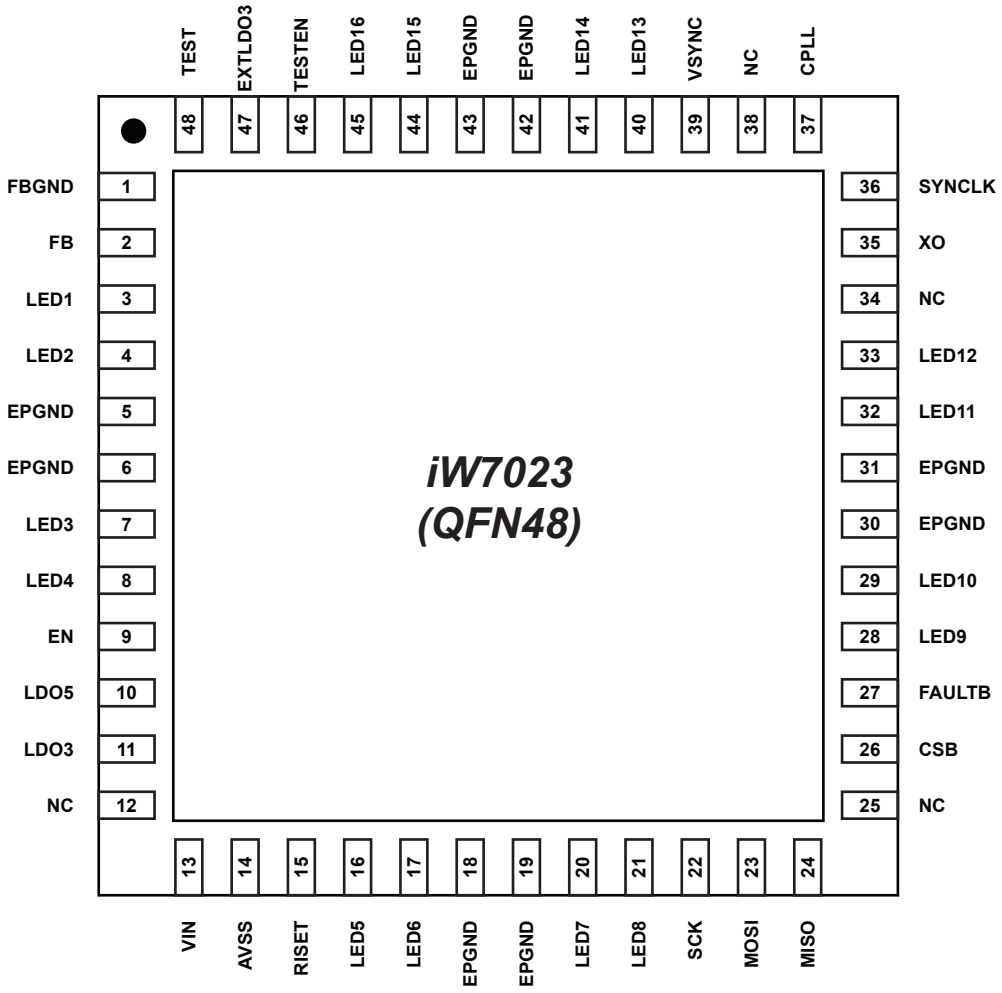
4.0 Pinout Description



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Pinout Description (cont.)

Pin #	Name	Type	Pin Description
1	FBGND	Ground	Signal ground for FB.
2	FB	Analog Output	Analog DAC output interface with external buck or boost converter for LED boost/buck group.
3	LED1	Analog Output	LED cathode connection for string 1.
4	LED2	Analog Output	LED cathode connection for string 2.
5	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
6	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
7	LED3	Analog Output	LED cathode connection for string 3.
8	LED4	Analog Output	LED cathode connection for string 4.
9	EN	Digital Input	Enabled Input. Logic high is defined as 3.3V.
10	LDO5	Analog Output	Internal +5V LDO output and analog power section supply.
11	LDO3	Analog Output	Internal +3.3V LDO output and digital power section supply.
12	NC	N/A	No connection.
13	VIN	Supply Input	Input voltage to the main supply rail.
14	AVSS	Ground	Analog ground return for LDO regulator.
15	RISET	Analog Output	External Iset setting resistor. Pull-down to AVSS with a120kΩ ±0.1% resistor. [Test Pin]
16	LED5	Analog Output	LED cathode connection for string 5.
17	LED6	Analog Output	LED cathode connection for string 6.
18	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
19	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
20	LED7	Analog Output	LED cathode connection for string 7.
21	LED8	Analog Output	LED cathode connection for string 8.
22	SCK	Digital Input	SCK, serial clock input for Serial Peripheral Interface (SPI). Logic high is defined as 3.3V.
23	MOSI	Digital Input	Master output, slave input for SPI. Logic high is defined as 3.3V.
24	MISO	Digital 3 State Output	Master input, slave output for SPI. Logic high is defined as 3.3V.
25	NC	N/A	No connection.
26	CSB	Digital Input	Slave select input for SPI (Chip Select Bar). Active LOW. Logic high is defined as 3.3V.

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Pinout Description (cont.)

Pin #	Name	Type	Pin Description
27	FAULTB	Analog Output	Fault status (Active Low) - Open drain. Pull-up to LDO3 with a100kΩ ±0.1% resistor.
28	LED9	Analog Output	LED cathode connection for string 9.
29	LED10	Analog Output	LED cathode connection for string 10.
30	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
31	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
32	LED11	Analog Output	LED cathode connection for string 11.
33	LED12	Analog Output	LED cathode connection for string 12.
34	NC	N/A	No connection.
35	XO	Analog Output	External crystal connection XO pin with SYNCLK acting as XI pin.
36	SYNCLK	Digital Input	External clock input for the multiple chip system solution. Logic high is defined as 3.3V.
37	CPLL	Analog Output	PLL compensation output.
38	NC	N/A	No connection.
39	VSYNC	Digital Input	Vertical SYNC input. [Optional direct PWM control] Logic high is defined as 3.3V.
40	LED13	Analog Output	LED cathode connection for string 13.
41	LED14	Analog Output	LED cathode connection for string 14.
42	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
43	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
44	LED15	Analog Output	LED cathode connection for string 15.
45	LED16	Analog Output	LED cathode connection for string 16.
46	TESTEN	Digital I/O	Digital test pin.
47	EXTLDO3	Analog Input	External LDO3 enable. Pull-up to LDO5 with a100kΩ pull-up resistor.
48	TEST	Analog Output	Analog test pin.

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5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 7.0.

Parameter	Symbol	Min	Units
DC supply voltage at V_{IN}	V_{IN}	-0.3 to 40	V
LDO3 output voltage	V_{LDO3}	-0.3 to 4	V
LDO5 output voltage	V_{LDO5}	-0.3 to 7	V
AGND/AVSS/GNDn to GND		-0.3 to 0.3	V
LEDn voltage	V_{LEDn}	-0.3 to 60	V
Logic I/O pins (SCK, MISO, MOSI, CSB, & VSYNC)		-0.3 to 4	V
Voltage on all other pins except for LEDn pins		-0.3 to 7	V
Power dissipation at $T_A \leq 25°C$	P_D	TBD	mW
Maximum operating junction temperature	T_{JMAX}	-40 to 150	°C
Storage temperature	T_{STG}	-40 to 150	°C
Latch-up current		>100	mA
ESD rating per JEDEC JESD22-A114 - HBM		±2,000	V

6.0 Recommended Operating conditions

Parameter	Min	Typ	Max	Units
V_{IN} supply voltage	9		28	V
Thermal resistance junction		31.63		°C/W
LEDn voltage	0.5		60	V
LEDn current - Local dimming mode	20		150	mA
LEDn current - Scanning mode	20		240	mA

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7.0 Electrical Characteristics

V_{in} = 24V, 0°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Pins SECTION						
LDO3 output voltage	V_{LDO3}	EN = 3.3 V, I_{LDO3} = 0 mA	3.0	3.3	3.6	V
LDO5 output voltage	V_{LDO5}	EN = 5 V, I_{LDO5} = 0 mA	5.0	5.5	6.5	V
Quiescent current	I_S	Standby mode, No LED current	2.5	4.5	6.5	mA
		Shutdown mode		120	200	µA
LDO3 undervoltage lockout upper threshold	$V_{3\_UVLO\_HIGH}$	Guaranteed by design		2.7	2.85	V
LDO3 undervoltage lockout lower threshold	$V_{3\_UVLO\_LOW}$	Guaranteed by design	2.25	2.5		V
LDO5 undervoltage lockout upper threshold	$V_{5\_UVLO\_HIGH}$	Guaranteed by design		4.6	4.75	V
LDO5 undervoltage lockout lower threshold	$V_{5\_UVLO\_LOW}$	Guaranteed by design	3.8	4.0		V
Internal reference voltage	V_{ref}		2.45	2.5	2.55	V
VIN undervoltage lockout upper threshold	$V_{IN\_UVLO\_HIGH}$			8.0	9.0	V
VIN undervoltage lockout lower threshold	$V_{IN\_UVLO\_LOW}$		6.0	7.5		V
Internal oscillator frequency	f_{osc}		2.33		2.58	MHz
Digital I/O SECTION						
High level logic threshold	$V_{T(HIGH)}$				2.0	V
Low level logic threshold	$V_{T(LOW)}$		0.4			V
LDO3 Linear Regulator SECTION						
Line regulation		9V ≤ V_{IN} ≤ 28V, I_{LDO3} = 20mA			50	mV
Load regulation		V_{IN} ≤ 24V, I_{LDO3} = 20mA			120	mV
Maximum output current		V_{LDO3} > $V_{IN\_UVLO\_ON}$		60	100	mA
LDO5 Linear Regulator SECTION						
Line regulation		9V ≤ V_{IN} ≤ 28V, I_{LDO5} = 5mA			50	mV
Load regulation		V_{IN} ≤ 24V, I_{LDO5} = 5mA			120	mV
Maximum output current		V_{LDO5} > $V_{IN\_UVLO\_ON}$		5	10	mA

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Electrical Characteristics (cont.)

V_{in} = 24V, 0°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Generation SECTION						
Current balance		Per channel ILED = 120mA	-2		2	%
LED current Range		Average	20		150	mA
LED current Range		Peak	20		240	mA
Current rise time		20% to 80% LED current, dependent on PCB and LED cable. Guaranteed by design		1		µs
Current fall time		80% to 20% LED current, dependent on PCB and LED cable. Guaranteed by design		1		µs
PWM linear dimming range		12-bit resolution	1		99	%
PWM dimming range		12-bit resolution	0			%
PWM resolution		Minimum resolution required to ensure smooth brightness transitions	12			bits
PWM dimming frequency (10-bit)		NTSC mode - Desirable to run at high frequency to avoid audible noise and banding/shimmering (waterfall) effects. Step = 120 Hz	120		2.4k	Hz
		PAL mode: Step = 100Hz	100		2.4k	Hz
		3D Game mode: Step = 96Hz	96		2.4k	Hz
PWM dimming frequency (12-bit)		NTSC mode - Desirable to run at high frequency to avoid audible noise and banding/shimmering (waterfall) effects. Step = 120Hz	120		480	Hz
		PAL mode: Step = 100Hz	100		480	Hz
		3D Game mode: Step = 96Hz	96		480	Hz

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Electrical Characteristics (cont.)

V_{in} = 24V, 0°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Generation SECTION (Continued)						
Junction Temperature		Normal operation temperature range	-40		150	°C
Storage Temperature		Storage temperature range	-40		150	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	Common air flow = 0 m/sec		TBD		°C/W
Thermo Shutdown SECTION						
Thermal shutdown threshold	T_{SHDN}	Thermal shutdown/Turn-off temperature		145		°C
Thermal shutdown hysteresis				30		°C
Feedback Pins SECTION						
FB, min		FB minimum voltage VDAC = 00, No loading	200	240	260	mV
FB, max		FB maximum voltage VDAC = FF, No loading	2.45	2.55	2.65	V
FB sink		When FB varies by 1% of its unloaded target value			100	µA
FB source		When FB varies by 1% of its unloaded target value			100	µA

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8.0 Functional Block Diagram

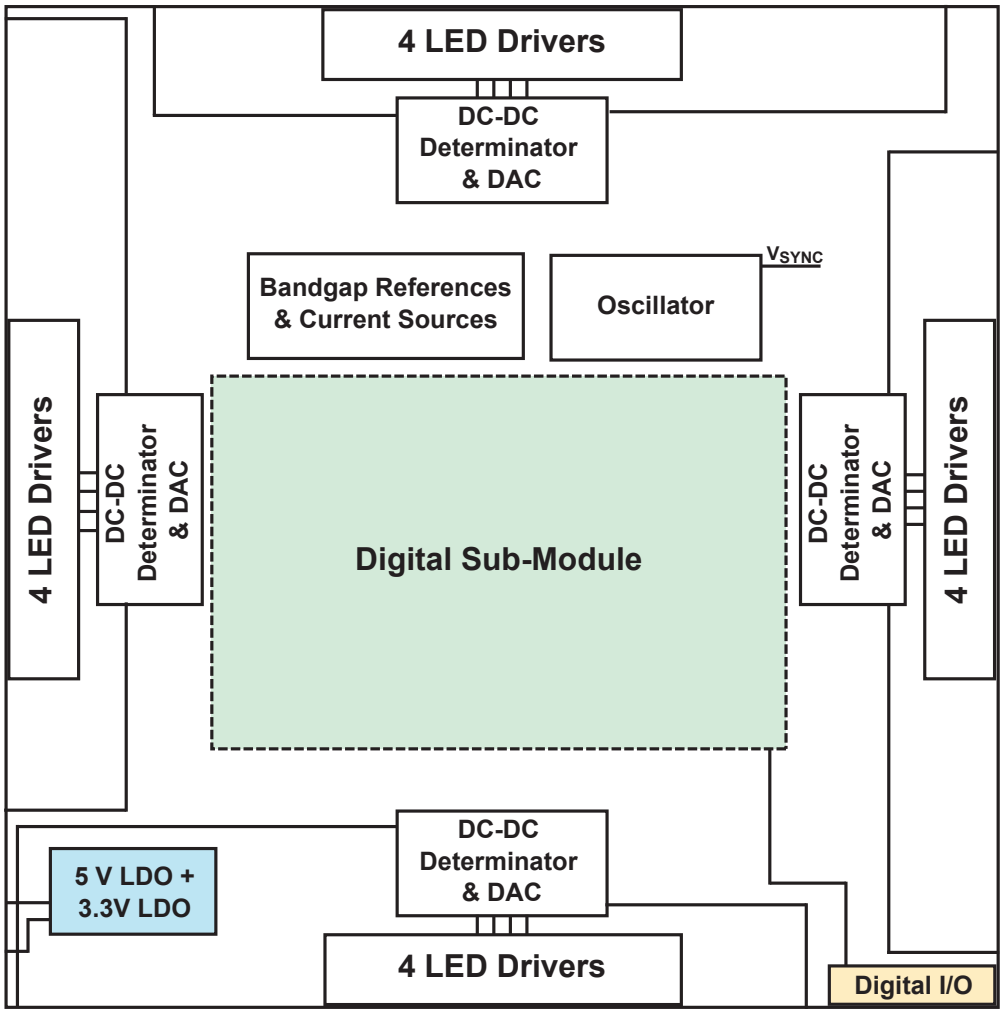

Figure 8.1: iW7023 Functional Block Diagram

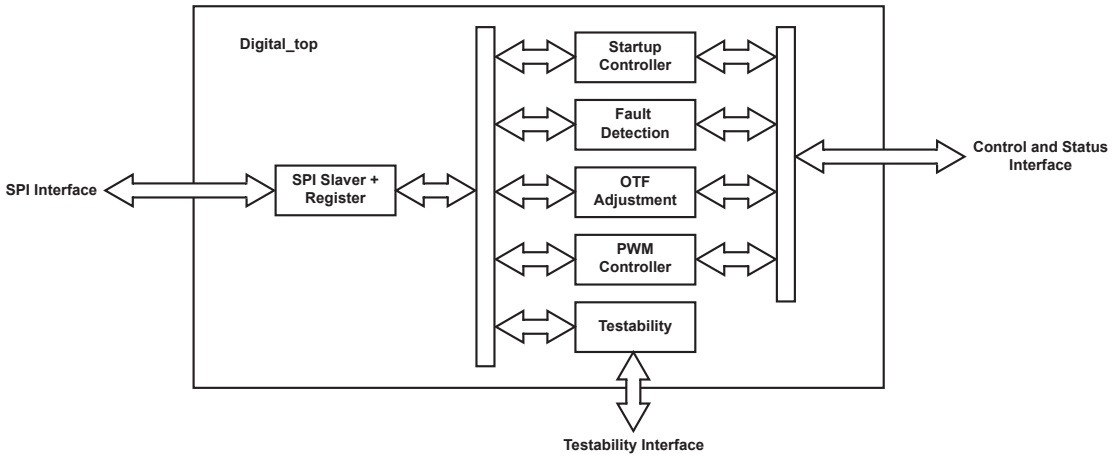

Figure 8.2: Digital Sub-Module Functional Block Diagram

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9.0 Operation Description

9.1 Adaptive Switching Algorithm

Adaptive switch mode current regulation improves the power efficiency by programmatically controlling the Low Drop Output (LDO) current regulation string in each channel to an optimum level which minimizes the differences in total voltage drop across each string (sharing the same LED power supply) while still minimizing the current differences in each string, thereby maintaining the reliability requirement for the LED component with peak current limit control. The adaptive switch mode also modifies the PWM duty cycle as necessary to automatically compensate for the allowed variances in the LDO current settings.

The following figure illustrates the power loss improvement that is obtained using the adaptive switch method.

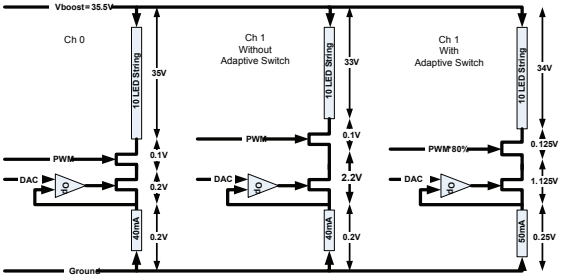


Figure 9.1: Power Loss Improvement Through Adaptive Switch Method

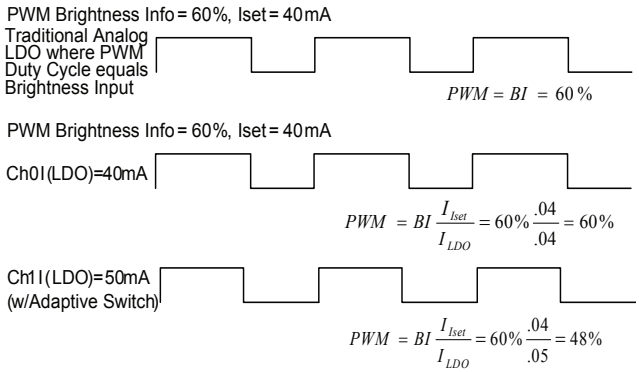
This is carried out by an adaptive channel balance algorithm performed during the power up sequence (referred to as calibration) where the LDO current setting of each channel is incremented while monitoring the multiple voltage potentials on the LDO regulation loop to determine when the loop is in the optimal operation point at the interface between the current regulation and non-regulation regions.

Each channel includes an LDO current regulator controlled by a 4-bit DAC which creates the reference voltage for its LDO. This 4-bit DAC is under control of the digital adaptive switch algorithm controller. The value of the LDO DAC can be observed in the register set where it is called “IDAC”.

This is initially performed during calibration. The optimal DAC settings are retained and updated as necessary by the digital controller. The operation point for each channel is monitored in real time for continued adaptive switch mode regulation for each LED string during normal operation.

This allows compensation for the total forward voltage drop differences such that the same current and on-time product can be maintained with different current and PWM dimming code settings as necessary to match the brightness of each string while minimizing the power dissipation within the LDO circuits.

The following illustration demonstrates the numerical PWM on time compensation that is provided to maintain constant peak current and PWM on time product proportional to the brightness input.



Wave Form and Timing Demonstration of PWM Duty Cycle Compensation for Variation In I(LDO) for each channel.

Figure 9.2: PWM Duty Cycle Compensation

In addition to maintaining a constant peak current and PWM on time product proportional to the desired brightness setting, the algorithm also provides luminance compensation and temperature compensation.

The following figure is a typical transfer function showing the relationship between optical luminance and forward current in an LED.

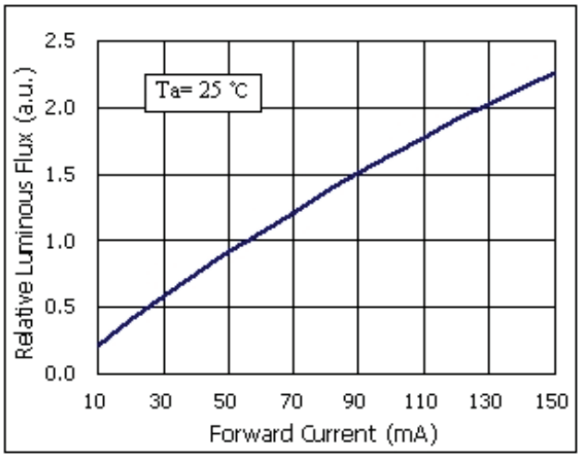


Figure 9.3: Optical Luminance vs. Forward Current in an LED

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This luminance can be fit reasonably well with the following function.

$$lum(x) = c_1 x + c_0 \quad (9.1)$$

To compensate for this luminous efficiency reduction in this application where brightness control is more important than current control, when the luminance compensation enable bit is set in the SPI interface register, the Luminance Control Module is modified to replace the following equation:

$$PWM\_out = PWM\_in \frac{I_{SET}}{I_n} \quad (9.2)$$

With the following one:

$$PWM\_out = PWM\_in \frac{lum(I_{SET})}{lum(I_n)} \quad (9.3)$$

To optimize the storage of information and maximize the accuracy, C_1, and C_0 must be multiplied by 2^{10} , and 2^0 respectively.

Based on the curve given for an LED of interest, scale the curve to occupy as close to, but not more than 2000 vertical units and as close to but no more than 1500 horizontal units.

Now take 2 x-y pairs of data, one from the far left side, and one from the far right side of the curve.

The following is a curve of a diode after it has been scaled as described above.

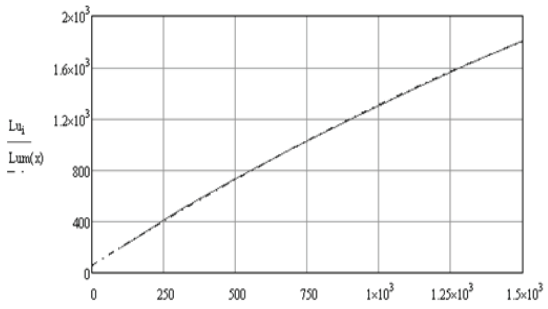

Figure 9.4: Scaled Diode Curve

From this graph, one might capture the following points:

I	Lu
100	191
1500	1809

Table 9.1

The coefficients are calculated as follows:

$$C_1 = \frac{Lu_2 - Lu_1}{I_1 - I_2} \quad (9.4)$$

$$C_0 = Lu_2 - C_1 I_2 \quad (9.5)$$

Using this technique, the results are calculated as follows:

$$Lum\_c1 = 2^{10} C_1 = 2^{10} (1.1557) = 1183 \quad (9.6)$$

$$Lum\_c0 = C_0 = 75 \quad (9.7)$$

The above numbers are decimal values that are directly used in Lum_c1 and Lum_c0.

Current luminance compensation is based on 1st order correction formula, and it might be upgraded into 2nd order transfer function in a future release.

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9.2 Calibration

In order to reduce the inrush current, calibration is based on 5% dimming ratio for Scanning Mode and 10% dimming ratio for Local Dimming Mode calibration by default. The calibration dimming ratio for Local Dimming can be adjusted by programming the brightness registers, and the calibration dimming ratio for Scanning Mode is always the half dimming ratio for Local Dimming. If the dimming ratio for Local Dimming is programmed less than 6.25%, then the IC internally clamps this ratio to be 6.25%. For scanning mode calibration, the minimum dimming ratio is 3.125%. In addition, the PWM frequency is based on software programmed value and LED string turning on sequence is following the dimming group setting and td_dg registers programmed delay.

Calibration is performed after the SPI initialization is complete and the Boost/Buck voltage has settled for 20 milliseconds allowing for the initial ramp up.

Figure 9.5 below describes the calibration sequence that is performed using VDAC, IDAC, and FORCE_ON.

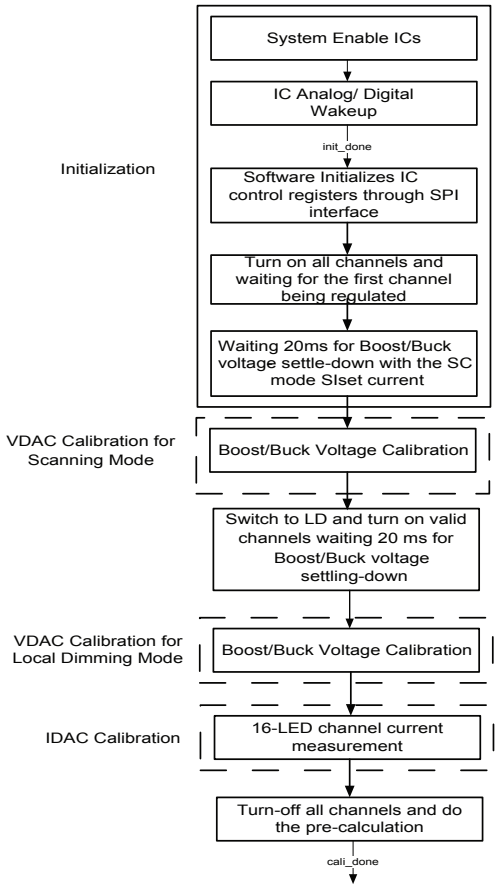

Figure 9.5: Calibration Sequence

Figure 9.6 below describes the sequence used by the firmware to bring up iW7023 to enable calibration.

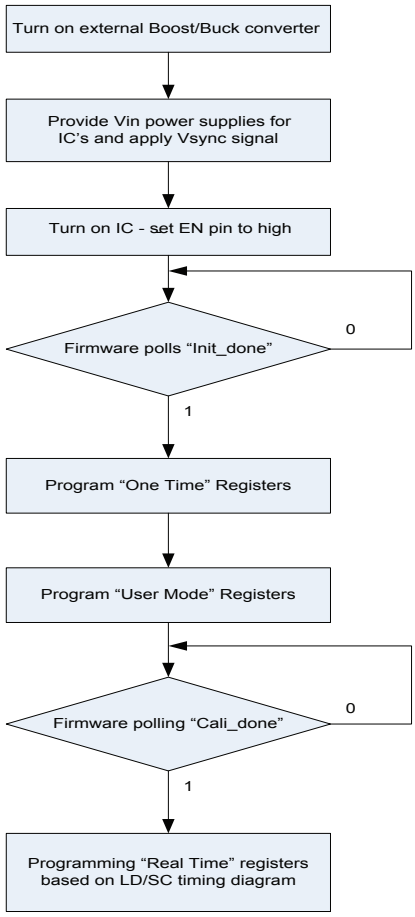

Figure 9.6: Firmware Sequence to Enable iW7023 Calibration

The function of the signals used in calibration are as follows.

VDAC is the digital value (8-bits) that drives the DAC which is used to affect the feedback input to the external Boost/Buck controller.

FORCE_ON is an internally generated digital signal from the LDO regulator that indicates whether or not the LDO is operating in the specified regulation. If it comes out of regulation, the FORCE_ON signal goes true.

An 8-bit DAC is used for adjustment of the Boost/Buck calibration.

The VDAC is in tri-state mode before the software initializes the IC control register through the SPI interface. Once the software completes initializing the IC, the VDAC setting is set to 0 by default which will cause the Boost/Buck regulator to settle at its highest possible setting to start out the calibration sequence.

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At this point, after the Boost/Buck voltage is ramped up, all the channels should indicate that they are in regulation through their individual LDOs FORCE_ON signal. There is a regulation detector on the LDO regulation loop that monitors multiple voltage potentials to ensure that the regulation is operating with enough loop gain for guaranteeing regulation and best efficiency. When the loop gain falls below the lower-bound limit threshold, this indicates that the channel is about to go out of regulation due to not having enough Boost/Buck voltage head room for that channel. With the Boost/Buck voltage at the maximum level, all channels should be in regulation, and therefore this regulation detector output called FORCE_ON should not be true.

The VDAC is increased by 4 LSB at a time at 2 millisecond intervals, by default, in a ramp decreasing the Boost/Buck voltage. This occurs until one channel within the Boost/Buck group indicates that it is coming out of regulation.

Then the VDAC output is decreased which increases the Boost/Buck voltage at 1 LSB per 2 millisecond interval, by default, until the FORCE_ON comparator output deactivates. The maximum time for this operation is just over 0.125 seconds, but will most often be shorter since the VDAC does not need to ramp the full distance. The above estimate is based on SISET being larger than or equal to ISET. If this is not true, the time can, under some circumstances, be a little longer.

After completing this function with the Scanning Mode ISET current setting, the whole process of VDAC calibration is repeated using the Local Dimming Mode current settings.

Once the VDAC calibration is completed, a similar function occurs with each IDAC. IDAC is the digital value (4-bits) that drives the DAC for each channel controlling the LDO current for the adaptive switching operation. This DAC is seen for each channel in figure 9.1. Initially all of the IDAC settings for the individual LDO's are set to 0, meaning that each channel is set up to operate at the current specified by the ISET bits in the SPI interface. Now that the Boost/Buck voltage is set to its ideal point where the weakest channel within the Boost/Buck group is in regulation. One-by-one, each channel will be adjusted within the Boost/Buck group by incrementing the IDAC value one bit at a time at 1 bit per 4.5 microseconds while again monitoring the FORCE_ON comparator output to determine when the LDO transistor moves deeper inside the triode region indicating that it is about to go out of regulation due to the current demand exceeding that which is feasible with the previously adjusted boost voltage. After the FORCE_ON comparator activates, then the IDAC value is reduced again by one step at a time until it deactivates again.

The calibration can be bypassed by setting cali_cfg to be HIGH. If calibration is bypassed, the internal VDAC for LD & SC are automatically loaded from VDAC_LD and VDAC_SC. The control flow to bypass calibration is shown below.

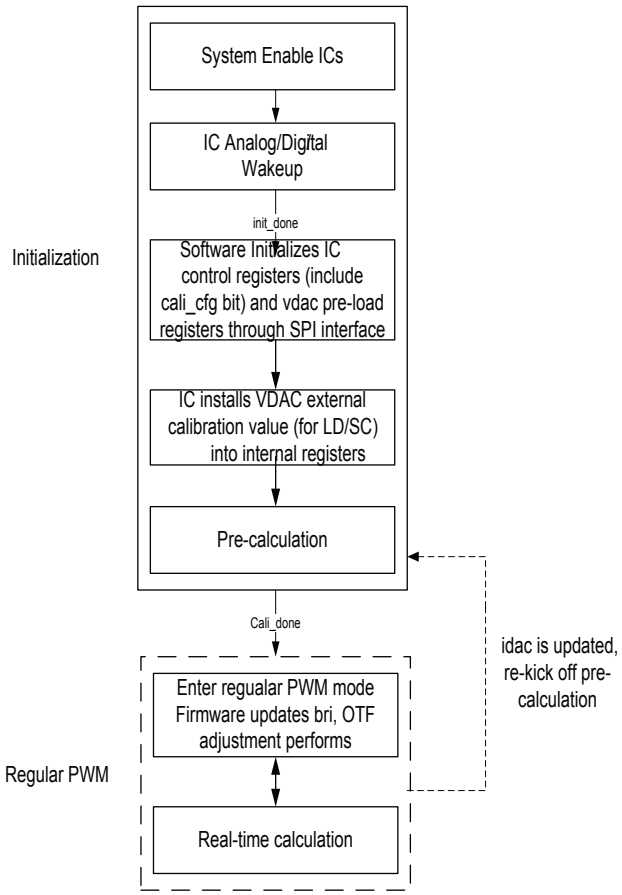

Figure 9.7: Control Flow to Bypass Calibration

9.3 Channel Grouping

Channel grouping allows multiple LED ports on the iW7023 IC to be connected together to one string of LED's at a higher current rating at the cost of a reduction in number of strings controlled by a single iW7023 IC. For example, if the LED string current is to operate at 240mA per string, the channel grouping can be set to 2 while the LDO Iset value is set to 120mA. By wiring the channels together in groups of two, the total output current per group will be 240 mA. However, the number of available strings will be 16/2 = 8 strings.

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16-Channel LED Driver for LCD Panel Backlighting

The iW7023 channels which are connected together to drive one string of LED's are called one channel group.

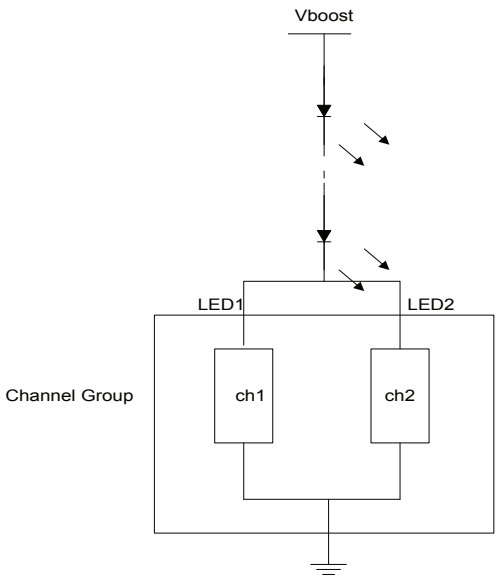

Figure 9.1 : Channel Group

In order to use this feature, it is still necessary to write the dimming value individually to every channel as it is to be updated from video frame-to-frame.

The iW7023 is notified of the channel group through the SPI register at address 0xa0 bits 10 as follows:

Bit[10] of REG_0a0

cg_cfg: ⇨ 0: 1 channel for one channel group (default)

⇨ 1: 2 channels for one channel group

9.4 On-the-Fly Automatic Operation

When the adaptive switch control register bit in REG_0a0 and the On-The-Fly (OTF) control register bit in REG_0a0 are enabled, internal VDAC and IDAC control values can be automatically adjusted based on the LED current regulation current and voltage adjustment head room for optimum thermal performance.

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10.0 Protection Description

The iW7023 monitors the behavior of each LED driver continuously. When fault conditions are observed, the iW7023 will turn off either the whole IC or the driver channel associated with the observed fault. There are two types of fault protection during startup – LED open and over-temperature, and three types continuous protection during normal operation – LED open, LED short, and over-temperature.

The three types of continuous protection are described in detail as follows:

1. LED_Open: While the iW7023 is operating, if a single LED string becomes open and its corresponding LED driver senses no current for eight consecutive vsync periods, the LED driver for this channel will be disabled causing the system to not request higher voltage from external DC-DC converter. In this state, the iW7023 will set bit 1 of SPI register 0x0c0. There is an automatic recovery feature from the LED_Open fault condition. When Auto-Recovery control register bit in REG_0a0 is enabled and the channel has been determined to be at fault, it can be enabled again within 0.5 secs once it meets Auto-Recovery criteria without the system being powered up again.
2. LED_Short (enough LEDs are shorted in an LED string): The iW7023 has accurate matching for each current source. However, the forward voltage of each LED string can vary significantly from channel to channel sharing the same Boost/Buck voltage power supply (within the same Boost/Buck group). The total voltage difference in each string results in additional power loss within the IC. For better efficiency, the voltage difference between lowest voltage string and highest voltage string is chosen to be less than 5.5V (or 8.0V programmable). If this condition is found to be false for eight consecutive vsync periods, the internal LED short protection circuit disables the string with the lowest forward biased voltage drop (which has the highest voltage at the pin). For example, when the iW7023 is started up, the LED pin voltage for the channel with the largest forward biased voltage drop should be about 0.6V. Therefore, if any LED pin has a voltage higher than 5.5V (or 8.0V), the corresponding LED string voltage is 4.9V (or 7.4V) lower than others. This means two or more LEDs in this LED string are shorted. The corresponding LED driver will then be turned off and the iW7023 will set bit 2 of the SPI register at 0x0c0. There is no automatic recovery from the LED_Short fault condition. Once a channel has been determined to be at fault, it is disabled until the system is powered up again.
3. OTP (Over-Temperature Protection): OTP is used to monitor if the die surface temperature is around 145°C. Once OTP is triggered, the LED drivers are disabled allowing the IC to cool down. Bit 0 of SPI register 0x0c0 is also set. After the temperature falls below around 115°C, the iW7023 resumes normal operation. This fault condition is not qualified for multiple vsync periods as the other two faults are. When this fault condition recovers, the iW7023 will re-perform calibration but does not require software re-initialization.

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11.0 Input and Output Equivalent Circuits

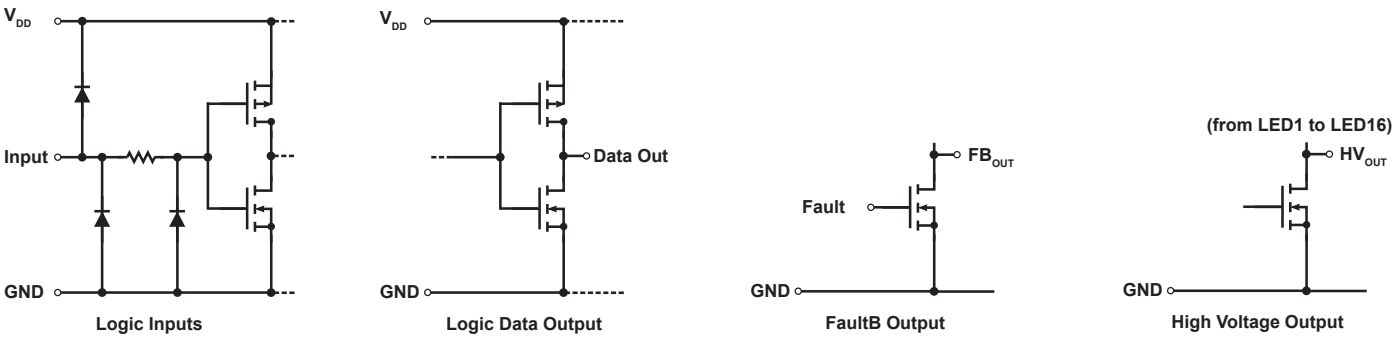

Figure 11.1: Logic Input and Output Equivalent Circuits

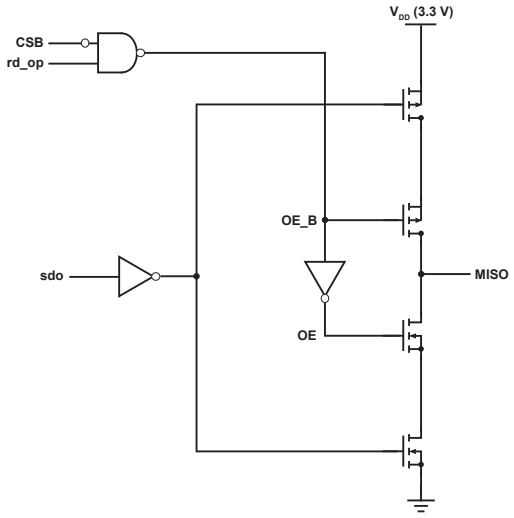

Figure 11.2: MISO Output Driving Circuit (tri-state)

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12.0 Control Register Table

The iW7023 is a high-efficiency driver for arrays of white LEDs. It contains several linear regulators, dimming control circuit, serial interface and 16 regulated current sources. The iW7023 provides a four-wire SPI compatible interface (MISO, MOSI, CSB and SCK), and several registers that are used to control and monitor the behavior of iW7023. The register map is shown as follows.

All the control registers are based on a 10-bit address and 16-bit data scheme.

The iW7023 on-chip master clock frequency is 2.4576MHz.

12.1 Control Register Mapping Table

Address	Access	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Real-Time Update Control Registers (Frame based)										
0x000	**R/W**	0x0000					temp_trk_ en	led_temp_ comp[2]	led_temp_ comp[1]	led_temp_ comp[0]
										dim_mode
0x001	**R/W**	0x0199	bri1[7]	bri1[6]	bri1[5]	bri1[4]	bri1[3]	bri1[2]	bri1[1]	bri1[0]
							bri1[11]	bri1[10]	bri1[9]	bri1[8]
:			:	:	:	:	:	:	:	:
:			:	:	:	:	:	:	:	:
0x010	**R/W**	0x0199	bri16[7]	bri16[6]	bri16[5]	bri16[4]	bri16[3]	bri16[2]	bri16[1]	bri16[0]
							bri16[11]	bri16[10]	bri16[9]	bri16[8]
Address 0x0011-0x004f (Reserved)										
Real-Time Update Control Registers (User Operation Mode based)										
0x050	**R/W**	0x0005	vsync_ cfg[1]	vsync_ cfg[0]		scan_ duty[4]	scan_ duty[3]	scan_ duty[2]	scan_ duty[1]	scan_ duty[0]
			tv_mode[1]	tv_mode[0]		pwm_ freq[4]	pwm_ freq[3]	pwm_ freq[2]	pwm_ freq[1]	pwm_ freq[0]
0x051	**R/W**	0x0010			pwm_bnk_ cfg[1]	pwm_bnk_ cfg[0]			sw_init_ byp	soft_rst
									dis_short_ prot	dis_open_ prot
0x052	**R/W**	0x0000	vdac_ld[7]	vdac_ld[6]	vdac_ld[5]	vdac_ld[4]	vdac_ld[3]	vdac_ld[2]	vdac_ld[1]	vdac_ld[0]
										ld_vdac-ld
0x053	**R/W**	0x0000	Vdac_sc[7]	Vdac_sc[6]	Vdac_sc[5]	Vdac_sc[4]	Vdac_sc[3]	vdac_sc[2]	vdac_sc[1]	vdac_sc[0]
										ld_vdac_sc
0x054	**R/W**	0x0000	td0[7]	td0[6]	td0[5]	td0[4]	td0[3]	td0[2]	td0[1]	td0[0]
							td0[11]	td0[10]	td0[9]	td0[8]
0x055	**R/W**	0x0000	td_dg1[7]	td_dg1[6]	td_dg1[5]	td_dg1[4]	td_dg1[3]	td_dg1[2]	td_dg1[1]	td_dg1[0]
							td_dg1[11]	td_dg1[10]	td_dg1[9]	td_dg1[8]
0x056	**R/W**	0x0000	td_dg2[7]	td_dg2[6]	td_dg2[5]	td_dg2[4]	td_dg2[3]	td_dg2[2]	td_dg2[1]	td_dg2[0]
							td_dg2[11]	td_dg2[10]	td_dg2[9]	td_dg2[8]
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
0x064	**R/W**	0x0000	td_dg16[7]	td_dg16[6]	td_dg16[5]	td_d16[4]	td_dg16[3]	td_dg16[2]	td_dg16[1]	td_dg16[0]
							td_ dg16[11]	td_ dg16[10]	td_dg16[9]	td_dg16[8]
Address 0x065-0x09f (Reserved)										

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12.1 Control Register Mapping Table (cont.)

Address	Access	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Initial One-Time Update Control Registers - *These functions can be changed on the fly, but it is not recommended unless some reduced picture quality and performance can be tolerated for up to 4 frames.*										
0x0a0	**R/W**	0x0000	apt_sw_en	otf_apt_en	lum_trk_en	vled_short	clk_sel[1]	clk_sel[0]	cali_cfg	cali_time_ step
			auto_rcv_ en	ldac_hf_en	apt_sw_ cfg[1]	apt_sw_ cfg[0]	vdac_rvs_ en	cg_cfg	pwm_mdl_ cfg[1]	pwm_mdl_ cfg[0]
0x0a1	**R/W**	0x7444	iset[7]	iset[6]	iset[5]	iset[4]	iset[3]	iset[2]	iset[1]	iset[0]
			slset[7]	slset[6]	slset[5]	slset[4]	slset[3]	slset[2]	slset[1]	slset[0]
0x0a2	**R/W**	0x05b5	lu_c1[7]	lu_c1[6]	lu_c1[5]	lu_c1[4]	lu_c1[3]	lu_c1[2]	lu_c1[1]	lu_c1[0]
			direct_pwm	mis_ vsync_sd_ en	iset_2mA_ en		lu_c1[11]	lu_c1[10]	lu_c1[9]	lu_c1[8]
0x0a3	**R/W**	0x1039	lu_c0[7]	lu_c0[6]	lu_c0[5]	lu_c0[4]	lu_c0[3]	lu_c0[2]	lu_c0[1]	lu_c0[0]
			fault_ dglch_ cfg[1]	fault_ dglch_ cfg[0[					lu_c0[9]	lu_c0[8]
Address 0x0A6-0x0ff (Reserved)										
Interrupt Registers										
0x0c0	R/W	0x0000					mis_ vsync_int_ msk	led_short_ int_msk	led_open_ int_msk	ot_int_msk
0x0c1	R/W	0x0000					mis_ vsync_int_ src	led_short_ int_src	led_open_ int_src	ot_int_src
Status Registers										
0x100	**R**	0x0000			cali_done	Init_done				OT
			led_open_ idx[3]	led_open_ idx[2]	led_open_ idx[1]	led_open_ idx[0]	led_short_ idx[3]	led_short_ idx[2]	led_short_ idx[1]	led_short_ idx[0]
0x101	R/W	0x0000	ch_en[7]	ch_en[6]	ch_en[5]	ch_en[4]	ch_en[3]	ch_en[2]	ch_en[1]	ch_en[0]
			ch_en[15]	ch_en[14]	ch_en[13]	ch_en[12]	ch_en[11]	ch_en[10]	ch_en[9]	ch_en[8]
0x102	**R**	0x0000	ldac2[3]	ldac2[2]	ldac2[1]	ldac2[0]	ldac1[3]	ldac1[2]	ldac1[1]	ldac1[0]
			ldac4[3]	ldac4[2]	ldac4[1]	ldac4[0]	ldac3[3]	ldac3[2]	ldac3[1]	ldac3[0]
0x103	**R**	0x0000	ldac6[3]	ldac6[2]	ldac6[1]	ldac6[0]	ldac5[3]	ldac5[2]	ldac5[1]	ldac5[0]
			ldac8[3]	ldac8[2]	ldac8[1]	ldac8[0]	ldac7[3]	ldac7[2]	ldac7[1]	ldac7[0]
0x104	**R**	0x0000	ldac10[3]	ldac10[2]	ldac10[1]	ldac10[0]	ldac9[3]	ldac9[2]	ldac9[1]	ldac9[0]
			ldac12[3]	ldac12[2]	ldac12[1]	ldac12[0]	ldac11[3]	ldac11[2]	ldac11[1]	ldac11[0]
0x105	**R**	0x0000	ldac14[3]	ldac14[2]	ldac14[1]	ldac14[0]	ldac13[3]	ldac13[2]	ldac13[1]	ldac13[0]
			ldac16[3]	ldac16[2]	ldac16[1]	ldac16[0]	ldac15[3]	ldac15[2]	ldac15[1]	ldac15[0]
0x106	**R**	0x0000	vdac[7]	vdac[6]	vdac[5]	vdac[4]	vdac[3]	vdac[2]	vdac[1]	vdac[0]

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12.2 Control Register Bit Field Definitions

Definition	Access	Description
Real-Time Update Control Registers (Frame Based)		
dim_mode	R/W	0: local dimming (default) 1: scanning mode
temp_trk_en	R/W	0: disable temperature-current compensation (default) 1: enable temperature-current compensation
led_temp_comp[2:0]	R/W	LED junction temperature vs. derating of Luminous Flux Density compensation factor (Ct). The equation for LED junction temperature compensation is “PWM_ out = PWM_in / Ct”. This compensation factor is defined as follows: 0: Ct = 1(default); 1: Ct = (1+1/32); 2: Ct = (1+2/32); 3: Ct = (1+3/32); 4: Ct = (1+4/32); 5: Ct = (1+5/32); 6: Ct =(1+6/32); 7: Ct = (1+7/32)
bri1[11:0] to bri16[11:0]	R/W	12-bit brightness setting for each of the 16 LED channels, adjusting brightness in 4096 steps. Please refer to “The Brightness Register vs. On Duty Table” to get the exact mapping information. Default value is 0x199.
Definition	**Access**	**Description**
Real-Time Update Control Registers (User Operation Mode Based)		
tv_model[1:0]	R/W	0: NTSC mode, vsync frequency is 120Hz, 240Hz or 480Hz (default) 1: PAL mode, vsync frequency is 100Hz, 200Hz or 400Hz 2: 3D Game mode, vsync frequency is 96Hz, 192Hz or 384Hz 3: NTSC mode
vsync_cfg[1:0]	R/W	*If TV is in NTSC mode:* 0: VSYNC = 120Hz (default) 1: VSYNC = 240Hz 2: VSYNC = 480Hz 3: the same as 2’b00 *If TV is in PAL mode:* 0: VSYNC = 100Hz (default) 1: VSYNC = 200Hz 2: VSYNC = 400Hz (scanning mode) 3: the same as 2’b00 *If TV is in 3D Game mode:* 0: VSYNC = 96Hz (default) 1: VSYNC = 192Hz 2: VSYNC = 384Hz 3: the same as 2’b00 PWM frequency needs to be programmed to be equal or faster than VSYNC frequency.

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12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Real-Time Update Control Registers (User Operation Mode Based) (cont.)		
scan_duty[4:0]	R/W	0: 20% 1: 24% ….. 5: 40% (default) ….. 20: 100% (Any number greater than this results in 100%) This Scanning Mode dimming ratio may be slightly adjusted by the IC internally in order to meet the requirement of Tsc being the integer number of the dimming period (please refer to the Scanning mode timing diagram). Please note that for thermal reasons, it is not recommended in most cases to use more than 50% scan duty unless the scan duty SISET value is not set higher than the Local Dimming (LD) current setting.
pwm_freq[4:0]	R/W	*If TV is in NTSC mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 20 steps 0 - 19: 120Hz to 2.4kHz with 120Hz per step for 10-bit PWM resolution 0 - 3: 120Hz to 480Hz with 120Hz per step for 12-bit PWM resolution *If TV is in PAL mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 24 steps 0 - 23: 100Hz to 2.4kHz with 100Hz per step for 10-bit PWM resolution 0 - 3: 100Hz to 480Hz with 100Hz per step for 12-bit PWM resolution *In TV is in 3D game mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 25 steps 0 - 24: 96Hz to 2.4kHz with 96Hz per step for 10-bit PWM resolution 0 - 3: 96Hz to 480Hz with 96Hz per step for 12-bit PWM resolution The default value is 0
soft_rst	R/W	0: no action (default) 1: perform soft reset, - all the IC internal registers in synclk clock domain are reset; - all the IC internal registers in sck clock domain remain in the same configuration
sw_init_byp	R/W	0: software needs to initialize the One Time registers and User mode before IC start to calibration (default) 1: bypass software initialization step
pwm_bnk_cfg[1:0]	R/W	0: PWM sampling blank time is 8 clock cycles from the rising edge of PWM 1: PWM sampling blank time is 32 clock cycles from the rising edge of PWM (default) 2: PWM sampling blank time is 128 clock cycles from the rising edge of PWM 3: PWM sampling blank time is 254 clock cycles from the rising edge of PWM
dis_open_prot	R/W	0: enable OPEN protection (default) 1: disable OPEN protection

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12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Real-Time Update Control Registers (User Operation Mode Based) (cont.)		
dis_short_prot	R/W	0: enable SHORT protection (default) 1: disable SHORT protection
vdac_ld[7:0] ld_vdac_ld	R/W	Load 8-bit Boost/Buck voltage DAC value for LD mode ld_vdac_ld: 0: IC internal vdac for LD mode is adjusted On-the-Fly (default) 1: load 8-set vdac value from vdac_ld for LD mode Note: When this bit is left as a 1, the value of VDAC is frozen at the value that was written to it when it was set to 1. When writing to this bit set to 0, the VDAC becomes read only, and if free to adjust by normal on the fly operations.
vdac_sc[7:0] ld_vdac_sc	R/W	Load 8-bit Boost/Buck voltage DAC value for SC mode ld_vdac_sc: 0: IC internal vdac for SC mode is adjusted On-the-Fly (default) 1: load 8-set vdac value from vdac_sc for SC mode Note: When this bit is left as a 1, the value of VDAC is frozen at the value that was written to it when it was set to 1. When writing to this bit set to 0, the VDAC becomes read only, and if free to adjust by normal on the fly operations.
td0[11:0] (tsd0[11:0])	R/W	The timing delay from vsync rising edge to the first scan line updating the brightness on TV. The timing delay is in 8 synclk cycles as the time unit. In local dimming mode, it should be programmed as td0; in scanning mode, it should be programmed as tsd0. The default value is 0
td_dg1[11:0] to td_dg16[11:0] (tsd_dg1[11:0] to tsd_dg16[11:0])	R/W	The timing delay from vsync rising edge to the dimming ratio updating for each dimming group. The timing delay is in 8 synclk cycles as the time unit. In local dimming mode, this set of registers should be programmed as td_dg1[11:0] ~ td_dg16[11:0]; in scanning mode, it should be programmed as tsd_dg1[11:0] ~ tsd_dg16[11:0]. td0 is always equal to or less than td_dg1 The default value is 0
Initial One-Time Update Control Registers - *These features are most often set or changed before calibration; however, they can also be changed on-the-fly, but their response times are not guaranteed within one frame. Picture quality and thermal performance could be slightly degraded for a few frames just after these items are changed on-the-fly.*		
apt_sw_en	R/W	0: disable adaptive switch mode (default) 1: enable adaptive switch mode
apt_sw_cfg[1:0]	R/W	0: 24% adaptive switch range in 4% steps (default) 1: 48% adaptive switch range in 4% steps 2, 3: 60% adaptive switch range in 4% steps
otf_apt_en	R/W	0: disable on-the-fly power monitoring and adjustment (default) 1: enable on-the-fly power monitoring and adjustment

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12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Initial One-Time Update Control Registers (cont.)		
lum_trk_en	R/W	0: disable luminance-current compensation (default) 1: enable luminance-current compensation
direct_pwm	R/W	0: each channel pwm dimming is controlled by individual bri register setting (default) 1: all channel pwm signals are coming from vsync pin directly
mis_vsync_sd_en	R/W	0: no IC shutdown if vsync pulse is missing for 100ms (default) 1: IC shutdown if vsync pulse is missing for 100ms
auto_rcv_en	R/W	0: disable auto-recovery for OPEN fault detection (default) 1: enable auto-recovery for OPEN fault detection
cali_cfg	R/W	0: normal IC calibration (default) 1: bypass IC calibration, firmware uploads vdac values through vdac_ld and vdac_sc registers
cali_time_step	R/W	0: 2ms per vdac calibration time step (default) 1: 10ms per vdac calibration time step Note: During initiate calibration, if pwm_frequency is programmed to be faster than 500Hz, program this bit to be set to 0; otherwise, program this bit of register to be set to 1
iset[7:0]	R/W	8-bit control to set the nominal DC current of the LED drivers in local dimming mode If iset_2mA_en is set to 0 0 -150: for 0mA to 150mA current with 1mA step Default = 68 for 68mA Note: Can be set to 240mA peak current so long as system ensures that average current does not exceed 150mA. If iset_2mA_en is set to 1 0 - 75: for 0mA to 150mA current with 2mA step Default = 68 for 136mA Note: Can be set to 240mA peak current so long as system ensures that average current does not exceed 150mA.
siset[7:0]	R/W	8-bit control to set the nominal DC current of the LED drivers in scanning and 3D game modes If iset_2mA_en is set to 0 0 - 240: for 0mA to 240mA current with 1mA step Default = 116 for 116mA Note: Can be set to 240mA peak current so long as system ensures that average current does not exceed 150mA. If iset_2mA_en is set to 1 0 - 120: for 0mA to 240mA current with 2mA step Default = 116 for 232mA Note: Can be set to 240mA peak current so long as system ensures that average current does not exceed 150mA.

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12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Initial One-Time Update Control Registers (cont.)		
vled_short	R/W	0: LED short detection threshold = 8.0V (default) 1: LED short detection threshold = 5.5V
clk_sel[1:0]	R/W	0: using IC internal ring oscillator as master clock (default) 1: using external system clock (synclk) as master clock 2: using external crystal (synclk, XO) as master clock 3: using IC internal PLL as master clock
vdac_rvs_en	R/W	0: vdac output is same as digital control valve (default) 1: vdac output is bitwise negative from digital control value
pwm_mdl_cfg[1:0]	R/W	0: modulate PWM “Head Shift Lighting” based on dimming programming (default) 1: modulate PWM “Tail Shift Lighting” based on dimming programming 2,3: modulate PWM with “Center Shift Lighting” based on dimming programming
idac_hf_en	R/W	0: idac resolution is 4% of iset/siset current (default) 1: idac resolution is 2% of iset/siset current
iset_2mA_en	R/W	0: iset/siset resolution is 1mA (default) 1: iset/siset resolution is 2mA
fault_dglch_cfg[1:0]		0: 16 synclk cycle deglitch circuit following open/short detect signal 1: 32 synclk cycle deglitch circuit following open/short detect signal (default) 2: 64 synclk cycle deglitch circuit following open/short detect signal 3: 128 synclk cycle deglitch circuit following open/short detect signal
cg_cfg	R/W	Defines channel sharing group configuration 0: 1 channel for one channel group (default) 1: 2 channels for one channel group
lu_c0[9:0] lu_c1[11:0]	R/W	The 2nd order LED current to luminance nonlinear transfer function coefficient. The transfer function is: $Lum\_Flux(I_f) = C_1 I_f + C_0$ lu_c0 default: 57; lu_c1 default: 1461

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12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Interrupt Registers		
ot_int_msk	R/W	0: enable OT fault interrupt generation (default) 1: disable OT fault interrupt generation
led_open_int_msk	R/W	0: enable LED open fault interrupt generation (default) 1: disable LED open fault interrupt generation
led_short_int_msk	R/W	0: enable LED short fault interrupt generation (default) 1: disable LED short fault interrupt generation
mis_vsync_int_msk	R/W	0: enable missing vsync pulse interrupt generation (default) 1: disable missing vsync pulse interrupt generation
ot_int_src	R/W	0: no “OT fault” event happens (default) 1: “OT fault” event happens Writing “1” to this bit clears this bit register
led_open_int_src	R/W	0: no “LED open fault” event happens (default) 1: “LED open fault” event happens, read led_open_idx to further identify which channel is shorted Writing “1” to this bit clears this bit register
led_short_int_src	R/W	0: no “LED short fault” event happens (default) 1: “LED short fault” event happens, read led_open_idx to further identify which channel is shorted Writing “1” to this bit clears this bit register
mis_vsync_int_src	R/W	0: no “missing vsync pulse within 100ms” event happens (default) 1: “missing vsync pulse within 100ms” event happens Writing “1” to this bit clears this bit register
Status Registers		
led_short_idx[3:0]	R	The latest shorted LED channel index
led_open_idx[3:0]	R	The latest open LED channel index
ot	R	Status bit if over temperature fault happens
init_done	R	Status bit for IC initialization is done; software starts to program the initial one-time control registers to configure the IC
cali_done	R	Status bit for IC calibration is done; software starts to program the 17 real-time registers
ch_en[15:0]	R/W	Status bit for each of the 16 LED channels. It is used to flag if any LED channel is either enabled (1) or disabled (0) from fault detections
Idac1[3:0] : Idac16[3:0]	R	4-bit current DAC value for each LED channels
vdac[7:0]	R	8-bit voltage DAC value for the external Boost/Buck converter

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12.3 Brightness Control Register (R/W) vs. PWM Turn-on Duty Table

Brightness (Bin)	Brightness (Dec)	Bright (Hex)	Duty of Driver Turn-ON Time (%)
0000_0000_0000*	0	0	0.00%
0000_0000_0001*	1	1	0.02%
……..	…….	……..	……..
0000_0010_1000*	40	28	0.98%
……..	……..	……..	……..
0011_1111_1101	1021	3FD	24.93%
0011_1111_1110	1022	3FE	24.95%
0011_1111_1111	1023	3FF	24.98%
……..	……..	……..	……..
0111-1111-1101	2045	7FD	49.93%
0111-1111-1110	2046	7FE	49.95%
0111-1111-1111	2047	7FF	49.98%
……..	……..	……..	……..
1111_1111_1101	4093	FFD	99.93%
1111_1111_1110	4094	FFE	99.95%
1111_1111_1111	4095	FFF	99.98%

* Linearity not guaranteed within the shaded area.

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13.0 SPI Interface

13.1 SPI Interface Definitions

A Serial Peripheral Interface (SPI) system consists of one master device and one or more slave devices. The master is defined as a microcontroller providing the SPI clock and the slave as any IC receiving the SPI clock from the master. The iW7023 always operates as a slave device in master-slave operation mode.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with a LOW active Chip Select wire (CSB). Data is transmitted with a 3-wire interface consisting of wires for serial data input MOSI (refer to SDI in figures), serial data output MISO (refer to SDO in figures) and serial clock (SCK).

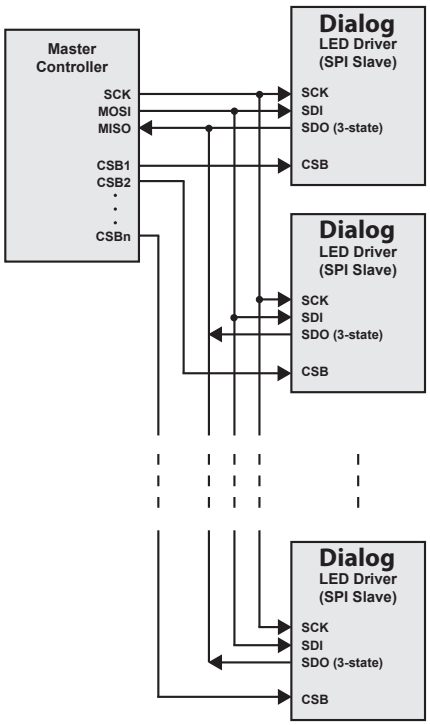

Figure 13.1 : Parallel Configuration of Multiple 16-Channel Drivers

The SPI interface in the iW7023 is designed to support any master controller that uses SPI bus. Communication can be carried out by software. The SPI interface is used for IC initialization, the real-time control and monitor purposes. The data transfer uses the following 4-wire interface:

MOSI	Master out slave in	Master controller ⇨ IC
MISO	Master in slave out	IC ⇨ master controller
SCK	Serial clock	Master controller ⇨ IC
CSB	Chip select (low active)	Master controller ⇨ IC

The word width of the SPI interface is defined as 16-bit. Each transaction is defined as the two phases - command address phase and data phase. These two phases are sequentially presented in the SPI interface during each transaction.

Command Address Phase	Data Phase

The Command Address Phase is composed of a 2-bit command transmission and a 10-bit register address transmission; the Data Phase is composed of the integer number of 16-bit word transmission.

The SPI transaction Command Word is defined as follows:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
N/A	N/A	I/R	R/W	Adr9	Adr8	Adr7	Adr6
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Adr5	Adr4	Adr3	Adr2	Adr1	Adr0	N/A	N/A

Bit 12	0: Read; 1: Write
Bit 13	0: Address Incremental Burst Access; 1: Address Repetitive Burst Access
Bit2 : Bit11	10-bit SPI Register Address

The difference between Incremental Burst vs. Repetitive Burst is if the address is incremental by 1 following each word data access. For Incremental Burst, the register address increments by 1 internally by the iW7023 for each word access; while for Repetitive Burst, the same address register is accessed repeatedly. The Repetitive Burst can be used for IC status register polling by software.

Each transmission starts with a falling edge of CSB and ends with the rising edge. During transmission, commands, address and data are controlled by SCK and CSB according to the following rules:

- Commands, address and data are shifted: MSB first, LSB last
- Output data bits are shifted out on the falling edge of SCK (MISO line)
- Input bits are sampled on the rising edge of SCK (MOSI line)
- After the device is selected with the falling edge of CSB, a 16-bit command and address is received. The command defines the operations to be preformed
- The address defines the register address to be accessed

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- Data transfer to MOSI continues immediately after receiving the address in all cases when data is to be written to IC internal registers
- Data transfer out from MISO starts with the falling edge of SCK immediately after the last bit of the SPI command is sampled in on the rising edge of SCK
- Maximum SPI clock frequency is 16 MHz
- Maximum data transfer speed for real time register access is 2.496 Mbps for up to 8 IC system configuration

13.2 SPI Interface Timing Diagrams

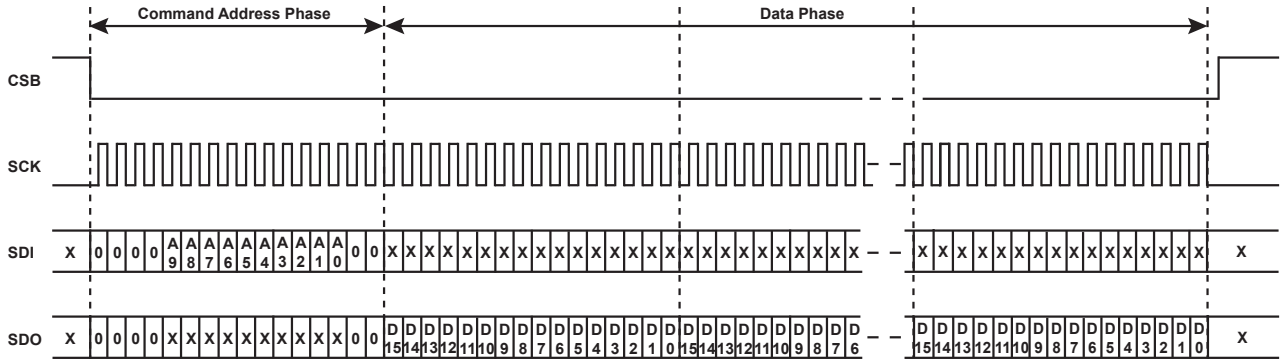
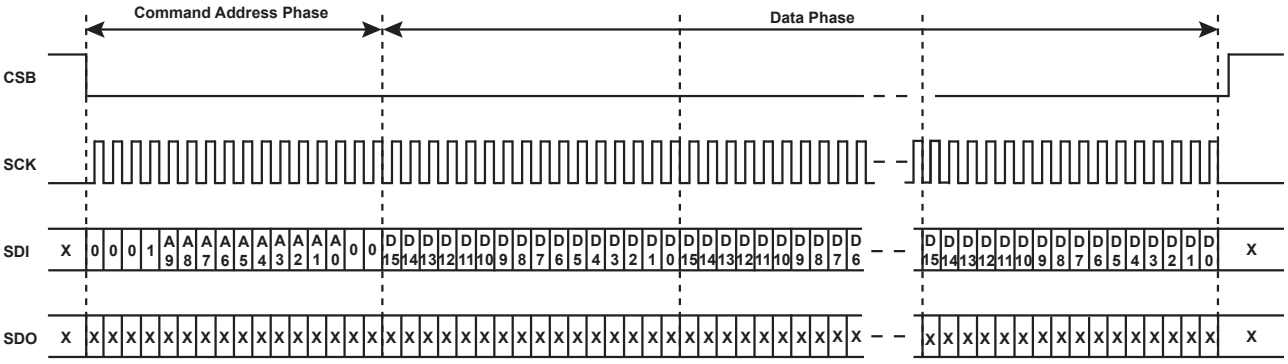


Figure 13.4 : Read Mode Transaction Timing Diagram



Software controls how many words to write by stopping to toggle SCK and disable chip select pin.

Figure 13.2 : Write Mode Transaction Timing Diagram

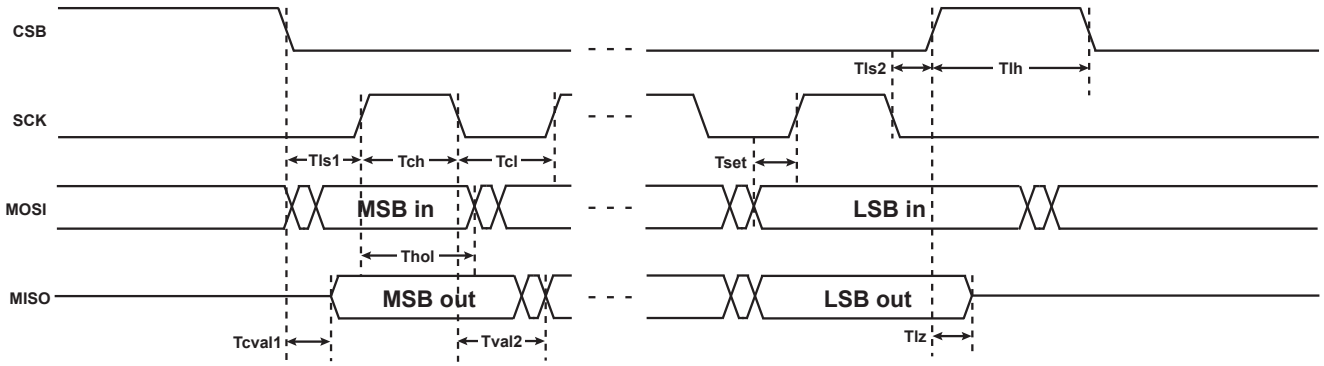


Figure 13.3 : SPI Bus Timing Diagram

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13.3 AC Parameters of the SPI Interface

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TERMINAL CSB, SCK						
Time from CSB (10%) to SCK (90%)	t_{LS1}		25			ns
Time from SCK (10%) to CSB (90%)	t_{LS2}		25			ns
SCK low time	t_{CL}	MISO Load capacitance < 100pF	30			ns
SCK high time	t_{CH}	MISO Load capacitance < 100pF	30			ns
TERMINAL MOSL, SCK						
Time from changing MOSI (10%, 90%) to SCK (90%) Data setup time	t_{SET}		12.5			ns
Time from SCK (90%) to changing MOSI (10%, 90%) Data hold time	t_{HOL}		12.5			ns
TERMINAL MISO, CSB						
Time from CSB (10%) to stable MISO (10%, 90%)	t_{VAL1}	MISO load capacitance < 150pF	17.5			ns
Time from CSB (90%) to high impedance state of MISO	t_{LZ}	MISO load capacitance < 150pF	17.5			ns
TERMINAL MISO, SCK						
Time from SCK (10%) to stable MISO (10%, 90%)	t_{VAL2}	MISO load capacitance < 150pF			25	ns
TERMINAL CSB						
Time between SPI cycles, CSB at high level (90%)	t_{LH}		250			ns

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14.0 Dimming Mode Control and Timing

The iW7023 supports two real-time dimming control modes – Local Dimming Mode and Scanning Mode.

Local Dimming Mode enables the LED backlight to be turned off in dark image areas, increasing the dynamic contrast ratio. Scanning Mode eliminates the flicker and ghosting problems (motion blur) associated with large-screen LCD TVs.

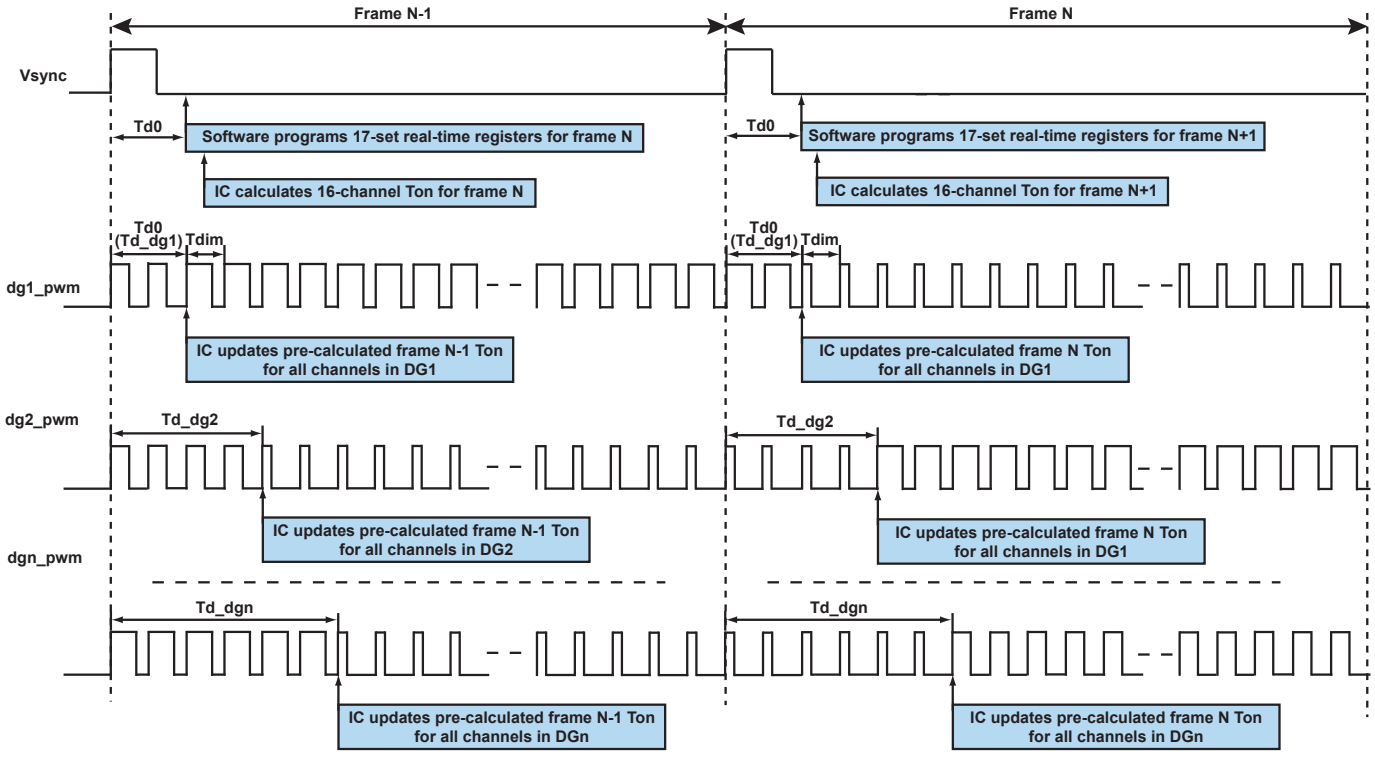

Figure 14.1 : Local Dimming Mode Timing Diagram

Td0: Delay time for DG1 updated after VSYNC. It is a control register which is programmed by software. For the multiple iW7023 chip solution for a TV system, Td0 is equal to the td_dg1 for the first iW7023 chip programming.

Td_dgn: Delay time for DGn update after Vsync. It is one pair of the td_dg1 ~ td_dg16 registers setting.

Tdim: It is the dimming period, which can be calculated by the configuration register pwm_freq[4:0]. Ton calculation by the iW7023 is pipelined by programming the dimming register. When the first channel dimming register is updated, the iW7023 initiates the calculation for this channel's Ton immediately. This allows the dimming register programming and Ton calculation to be overlapped in time, saving both the SPI and calculation bandwidth.

For single IC system solutions, software needs to program 17-set real time registers for the N+1 frame at td0 delay of N frame. The IC manages all 16-channel Ton calculations, pre-calculated Ton buffering, and Ton updating at the right timing.

For multiple IC system solutions, software needs to program 17-set real time registers sequentially for all ICs for the N+1 frame at td0 delay of N frames. Each IC starts the Ton calculation when the first dimming register belonging to this IC is updated.

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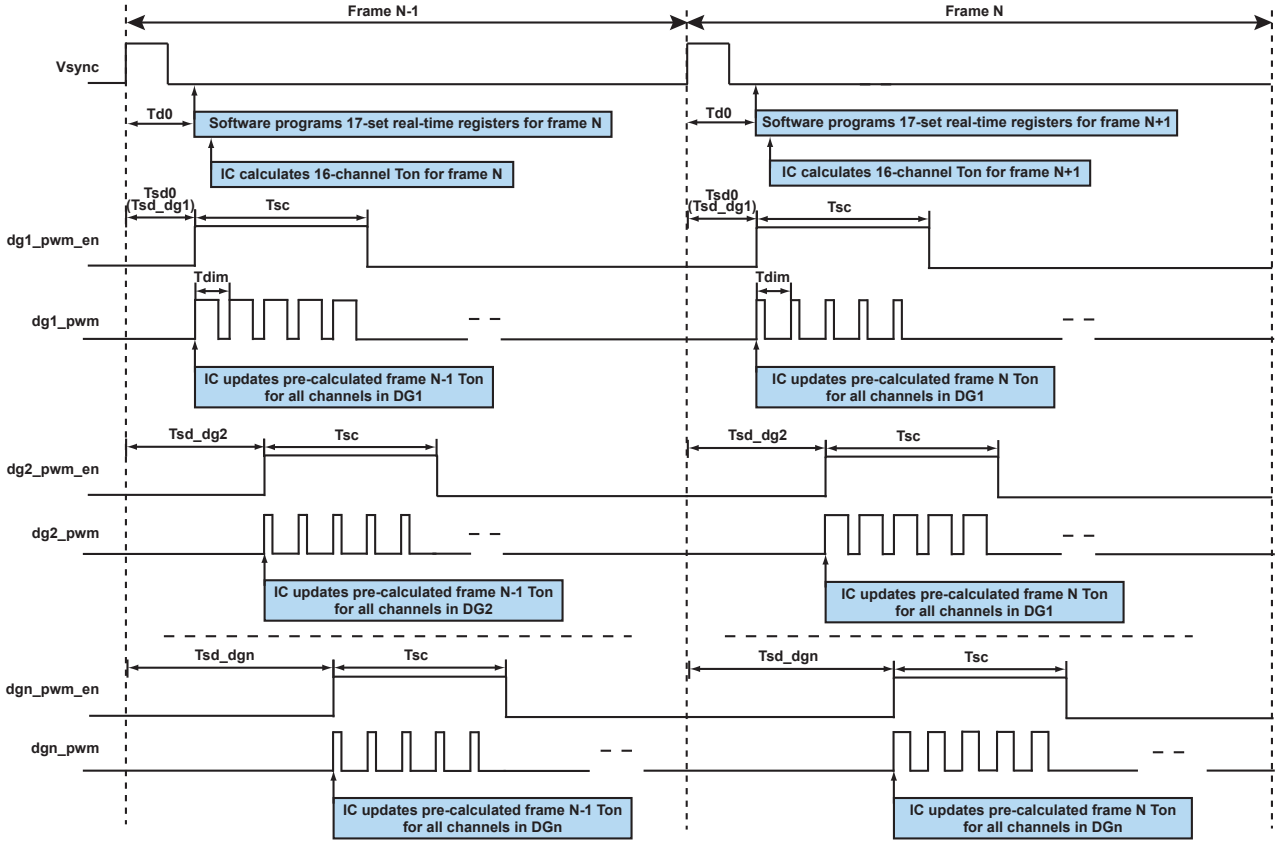

Figure 14.2 : Scanning Mode Timing Diagram

Tsd0: Delay time for DG1 updated after VSYNC. This is a control register which is programmed by the system software. For the multiple iW7023 chip solution for a TV system, Tsd0 is equal to the tsd_dg1 for the first iW7023 chip programming.

Tsd_dgn: Delay time for DGn update after VSYNC. This is one pair of the tsd_dg1 ~ tsd_dg16 registers setting

Tdim: This is the dimming period, which can be calculated by the configuration register pwm_freq[4:0].

Tsc: This is the scanning mode first-order dimming period. The iW7023 supports scan duty configurations by 5-bits which range from 20% to 100% scan duty in 4% steps. The scan duty cycle is a percentage of the vsync cycle time. In order to meet “Tsc = n•Tdim, n is an integer”. Tsc is adjusted slightly internally by the iW7023 to meet n•Tdim requirement. For example, if SVSYNC is 240Hz, and this first-order dimming is set to be 32%, and Tdim is programmed to be 2.4kHz, from the calculation, Tsc/Tdim = (0.32/240)/(1/2400) = 3.2. In this example, design will round this ratio to be the nearest integer, that is 3, and the real dimming ratio will be 30% instead of 32%.

Ton calculation by the iW7023 is pipelined with dimming register programming. When the first channel dimming register is updated, the IC initiates the calculation for this channel’s Ton immediately. This allows the dimming register programming and Ton calculation to be overlapped in time to save both SPI and the calculation bandwidth.

For a single IC system solution, the software is required to program 17-set real time registers for the N+1 frame at tsd0 delay of N frame. The IC manages all 16-channel Ton calculations, pre-calculated Ton buffering, and Ton updating at the right timing.

For multiple IC system solutions, the software is required to program 17-set real time registers sequentially for all ICs for the N+1 frame at tsd0 delay of N frame. Each IC starts the Ton calculation when the first dimming register belonging to this IC is updated.

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15.0 PWM Modulation Timing

The iW7023 offers three modes of PWM modulation. They are controlled by the PWM_mdl_cfg bits within the SPI register map, and work as described in the following timing diagram. The example given is for a 25% dimming duty cycle with a delay set at 30 percent of a VSYNC cycle.

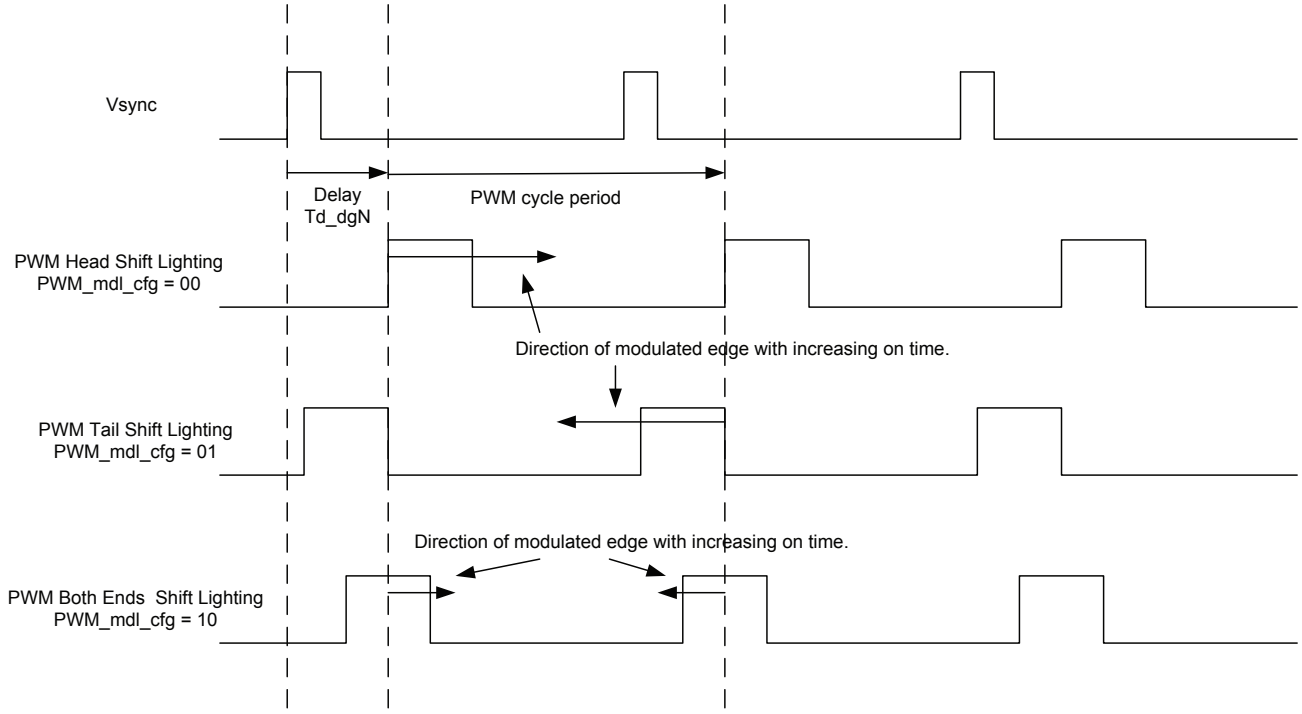
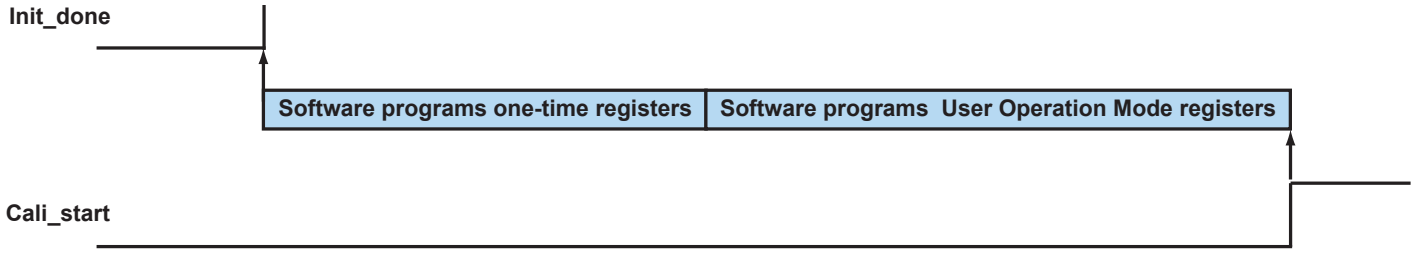


Figure 15.1: PWM Modulation Timing Diagram

16.0 Software Initialization Timing



After “init_done” is asserted, software needs to program the control registers in order to initiate the calibration.

Figure 16.1: Software Initialization Timing

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17.0 User Operation Mode Register Update Timing

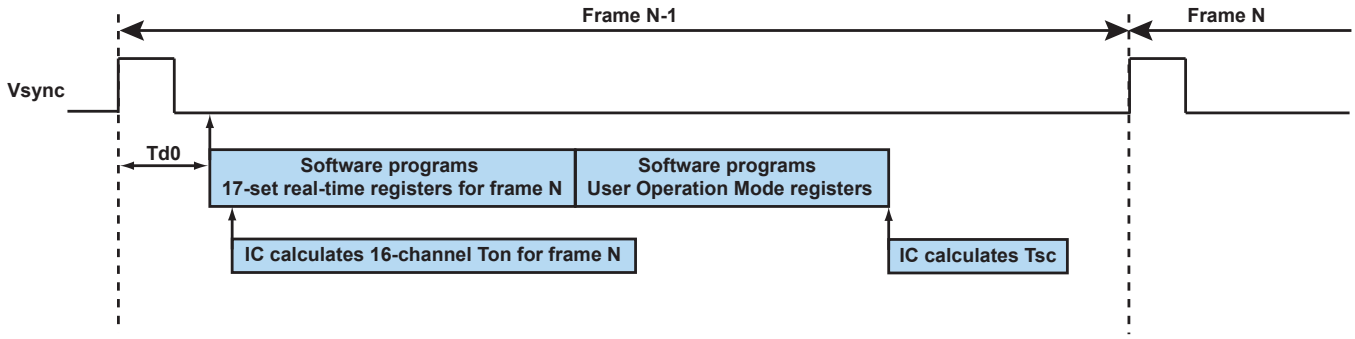

Figure 17.1: User Operation Mode Register Update Timing

18.0 Total Power Dissipation and Thermal Considerations

The input resistance into LEDx (for x = 1 to 16) of the iW7023 is around 2.5Ω for each of 16 LED pins. Suppose the maximum LED current is 150mA. Then the maximum continuous total power dissipation, under the condition that all of the LED strings have perfectly matched forward voltages, is:

$$16 \times 150mA \times 150mA \times 2.5\Omega = 0.9W \qquad (18.1)$$

However, in reality, LEDs are manufactured with varying forward voltages. Suppose the varying range of the forward voltage of each LED is around 0.1V. If each LED channel includes 10 LEDs in series, the variance of the total forward voltage of the 16 LED channels is around 0.1V•0.5•10 (LEDs) = 0.5V on the average. Since all of the 16 LED strings need to flow with the same currents, this disparity in forward voltages will contribute to the additional thermal dissipation at the 16 LED pins.

Therefore, the average continuous total power dissipation is around:

$$0.9W + 15 \times 150mA \times 0.5V = 0.9W + 1.125W = 2.025W \qquad (18.2)$$

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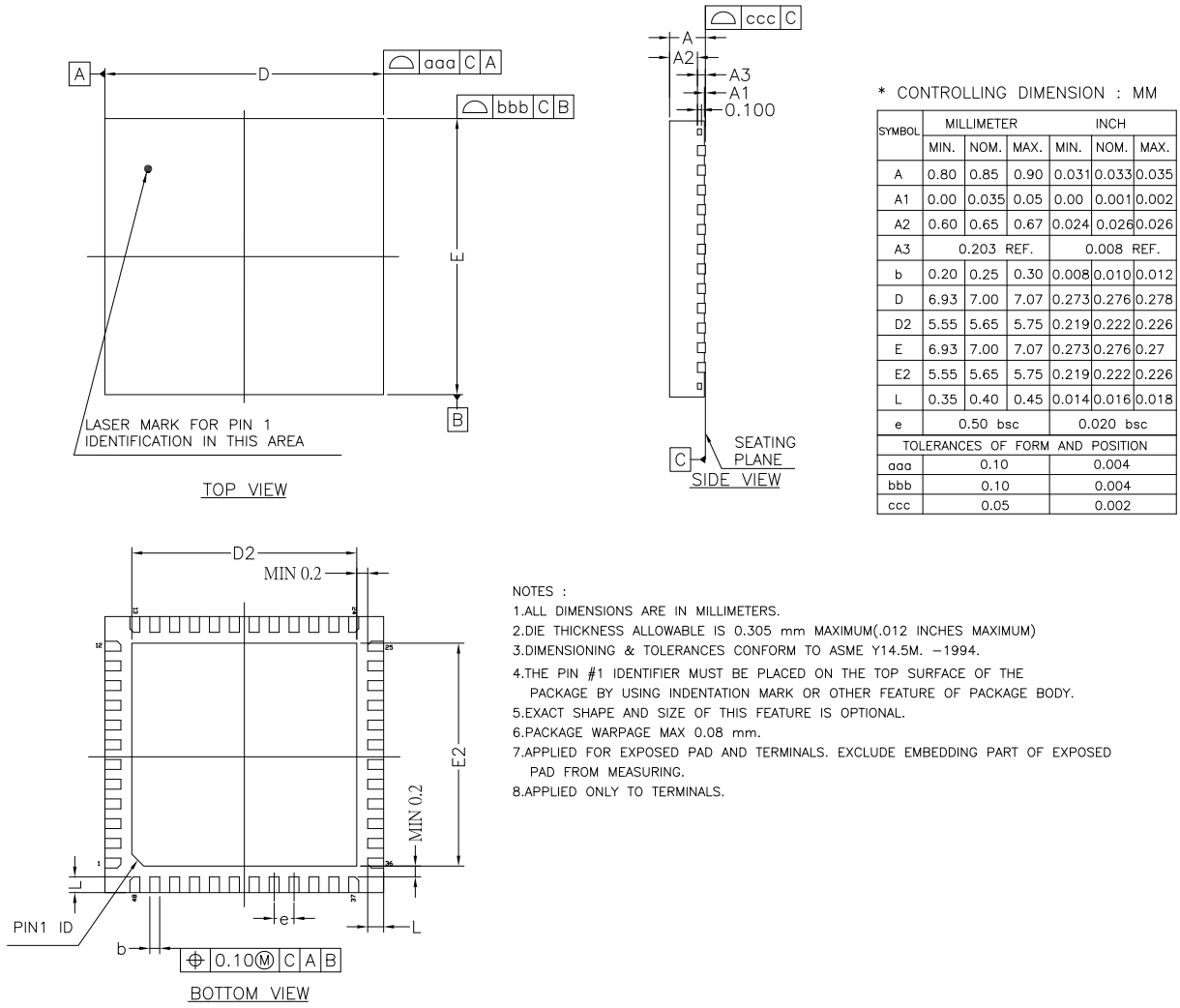
19.0 Physical Dimensions



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	0.60	0.65	0.67	0.024	0.026	0.026
A3	0.203 REF.			0.008 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	6.93	7.00	7.07	0.273	0.276	0.278
D2	5.55	5.65	5.75	0.219	0.222	0.226
E	6.93	7.00	7.07	0.273	0.276	0.27
E2	5.55	5.65	5.75	0.219	0.222	0.226
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. −1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Figure 19.1: Physical Dimensions, QFN-48 Package

20.0 Ordering Information

Part Number	Package	Description
iW7023-00-QFN4	QFN-7m-48L	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 4,000/reel. Minimum ordering quantity is 4,000.

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Contacting Dialog Semiconductor

United Kingdom
Dialog Semiconductor (UK) Ltd
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 88 22

Email
info_pcbg@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Singapore
Dialog Semiconductor Singapore
Phone: +65 648 499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China
Dialog Semiconductor (Shenzhen)
Phone: +86 755 2981 3669

Dialog Semiconductor (Shanghai)
Phone: +86 21 5424 9058

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