iW7032

32-Channel LED Driver for LCD Panel Backlighting

1.0 Features

- Fully integrated power FET with minimum external components
- Proprietary digital power management and patented adaptive switch mode LED driver
- 32-channel output each at 56 V with 9 V to 28 V input supply voltage range
- Dynamic external Boost or Buck controller interface to optimize system power efficiency
- Serial Peripheral Interface (SPI) compatible for high bandwidth PWM-based dynamic local dimming
- Per channel current up to 120 mA average current, with non-adaptive-switch peak current of 120 mA for local dimming and 192 mA for scanning mode, and with adaptive-switch peak current up to 60% higher.
- LED failure (open and short-circuit) detection
- LED brightness local dimming, scanning, and 3D game mode controlled by SPI interface
- PWM dimming range from 1% to 99.9% with 10-bit resolution
- Vsync synchronized PWM
- PWM dimming frequency from 120Hz to 2.4 kHz in NTSC; 100Hz to 2.4kHz in PAL; and 96Hz to 2.4kHz in 3D game mode with 5-bit programmability in normal mode.
- Over-temperature protection
- UVLO protection
- Green & Pb-free (RoHS compliant) BOM

2.0 Description

The iW7032 is a high efficiency driver for LEDs. It is designed for use with mid- to large size LCD panels that use arrays of LEDs as a backlight source. It is able to communicate with up to two external step-up or step-down PWM DC-DC converters to drive up to 32 separate strings of multiple series-connected LEDs.

The iW7032 features dynamic output voltage control, which automatically chooses the lowest active LED source voltage to regulate the feedback voltage of a step-up or step-down converter. Through this function, the iW7032 is able to dynamically adjust the output voltage of up to two external step-up or step-down converters to optimize the system power efficiency.

The iW7032 also provides 32 constant current sinks with maximum ±2% current matching. The LED PWM dimming can be adjusted dynamically through a high bandwidth SPI interface, which provides users flexibility to control the light intensity of LEDs. In addition, users can provide versatile configurations of the iW7032 through SPI interface registers.

The iW7032 can maintain very high efficiency even with the existence of LED channel total forward voltage mismatch, with the proprietary digital power management and patent pending adaptive switch mode LED current regulation technology.

The iW7032 has multiple features to protect the LED channels from fault conditions, and these protections are LED PWM cycle-by-cycle based to ensure system reliability and provide consistent operation.

iW7032 is available in a low-profile, space-saving thermally enhanced 10mm x 10mm TQFP-EP package.

3.0 Applications

- Edgelit Local Dimming for LED TV Backlit
- Direct & Segment-Edge LED Backlit LCDTV
- LCD Public Information Displays

4.0 Pinout Description

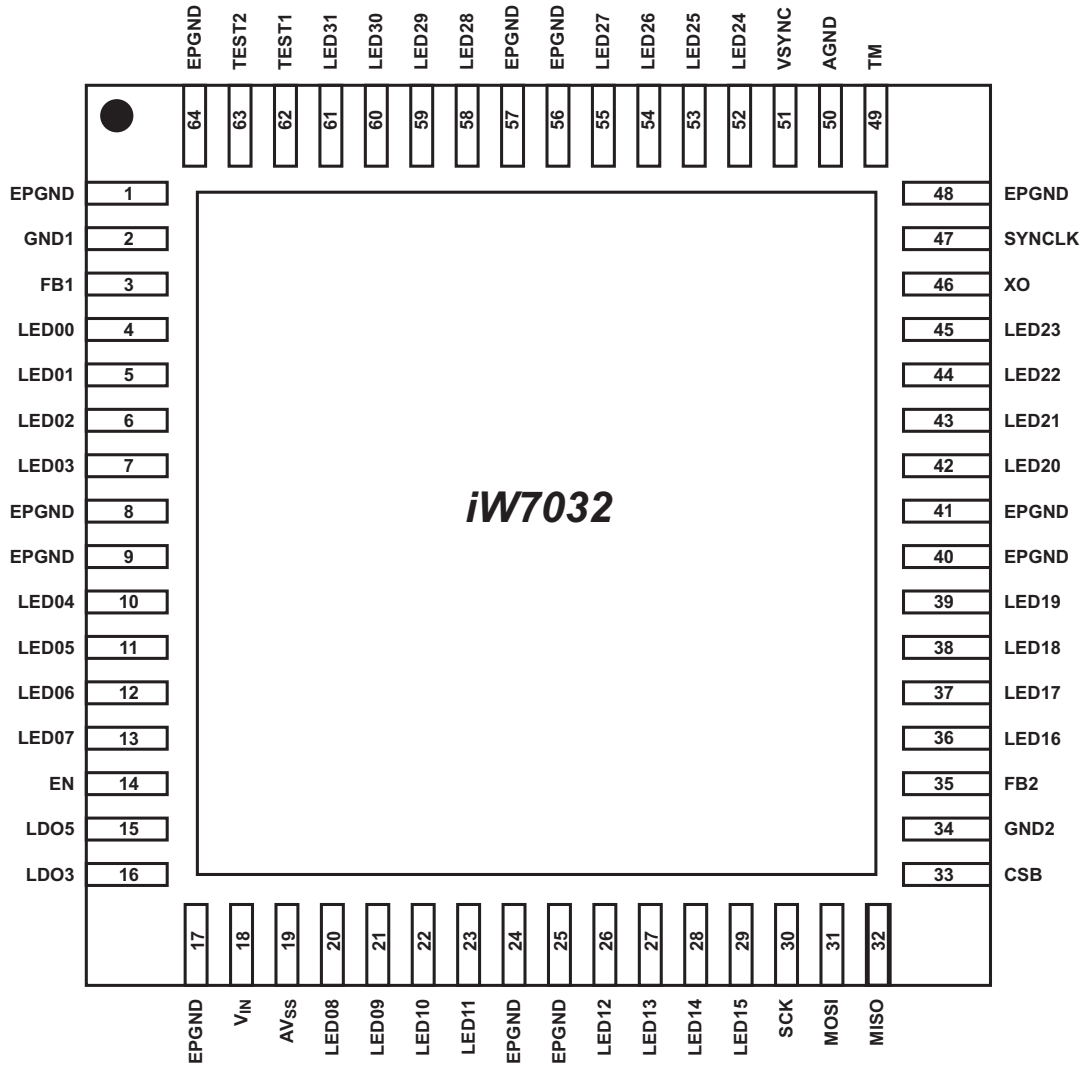


Figure 4.1. iW7032 Pin Configuration

Pin #	Name	Type	Pin Description
1	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
2	GND1	Ground	Signal ground for FB1.
3	FB1	Analog Output	Analog DAC output interface with external Buck or Boost converter for LED Boost/Buck group 1.
4, 5, 6, 7, 10, 11, 12, 13	LED00 - LED07	Analog Output	LED cathode connection for string 0 to string 7.
8, 9	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
14	EN	Digital Input	Enable Input. Logic high is defined as 3.3V.
15	LDO5	Analog Output	Internal +5V LDO output and analog power section supply.
16	LDO3	Analog Output	Internal +3.3V LDO output and digital power section supply.
17	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
18	VIN	Supply Input	Input voltage to the main supply rail.
19	AVSS	Ground	Analog ground return for LDO regulator.
20, 21, 22, 23, 26, 27, 28, 29	LED08 - LED15	Analog Output	LED cathode connection for string 8 to string 15.
24, 25	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
30	SCK	Digital Input	SCK, serial clock input for Serial Peripheral Interface (SPI). Logic high is defined as 3.3V.
31	MOSI	Digital Input	Master output, slave input for SPI. Logic high is defined as 3.3V.
32	MISO	Digital 3 State Output	Master input, slave output for SPI. Logic high is defined as 3.3V.
33	CSB	Digital Input	Slave select input for SPI (Chip Select Bar). Active LOW. Logic high is defined as 3.3V.
34	GND2	Ground	Signal ground for FB2.
35	FB2	Analog Output	Analog DAC output interface with external Buck or Boost converter for LED Boost/Buck group 2.
36, 37, 38, 39, 42, 43, 44, 45	LED16-LED23	Analog Output	LED cathode connection for string 16 to string 23.
40, 41	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
46	XO	Analog Output	External crystal connection XO pin with SYNCLK acting as XI pin.
47	SYNCLK	Digital Input	External clock input for the multiple chip system solution. Logic high is defined as 3.3V.
48	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.

Pin #	Name	Type	Pin Description
49	TM	Digital I/O	Dedicated digital test mode pin where logic high is 5.5V and logic low is 0V. Logic high enables ditigal test mode. Connect to logic low.
50	AGND	Ground	Analog ground return for internal circuits.
51	VSYNC	Digital Input	Vertical SYNC input. Logic high is defined as 3.3V.
52, 53, 54, 55, 58, 59, 60, 61	LED24-LED31	Analog Output	LED cathode connection for string 24 to string 31.
56, 57	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
62	TEST1	Digital I/O	Reserved test pin.
63	TEST2	Digital I/O	Reserved test pin.
64	EPGND	Ground	Exposed bottom pad used as the high current LED return current path.
	Exposed Bottom PAD	Ground	Exposed bottom PAD for high current ground

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 7.0.

Parameter	Symbol	Value	Units
V_{IN} supply voltage	V_{IN}	-0.3 to 40	V
LDO3 output voltage	V_{LDO3}	-0.3 to 4	V
LDO5 output voltage	V_{LDO5}	-0.3 to 7	V
AGND / AV_{SS} / GNDn to GND		-0.3 to 0.3	V
LEDn voltage	V_{LEDn}	-0.3 to 56	V
Logic I/O pins (SCK, MISO, MOSI, CSB, & VSYNC)		-0.3 to 4	V
Voltage on all other pins except for LEDn pins		-0.3 to 7	V
Power dissipation at $T_A \leq 25°C$	P_D	TBD	mW
Maximum operating junction temperature	$T_{J\ MAX}$	-40 to 150	°C
Storage temperature	T_{STG}	-40 to 150	°C
Lead temperature during IR reflow for ≤ 15 seconds	T_{LEAD}	TBD	°C
ESD rating per JEDEC JESD22-A114 - HBM		±2,000	V
ESD rating per JEDEC JESD22-A114 - CDM		±500	V

6.0 Recommended Operating Conditions

Parameter	Min	Max	Units
V_{IN} supply voltage	9	28	V
LEDn voltage	0.5	56	V
LEDn current - Local dimming mode	32	120	mA
LEDn current - Scanning mode	32	192	mA

7.0 Electrical Characteristics

V_{IN} = 24 V, 0°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY PINS						
LDO3 output voltage	V_{LDO3}	EN = 3.3 V, I_{LDO3} = 0 mA	3.0	3.3	3.6	V
LDO5 output voltage	V_{LDO5}	EN = 5 V, I_{LDO5} = 0 mA	5.0	5.5	6.5	V
Quiescent current	I_S	Standby mode, No LED current	4	8	12	mA
		Shutdown mode		120	200	µA
LDO3 undervoltage lockout upper threshold	$V_{3\ UVLO\ HIGH}$	Guaranteed by design		2.7	2.85	V
LDO3 undervoltage lockout lower threshold	$V_{3\ UVLO\ LOW}$	Guaranteed by design	2.25	2.5		V
LDO5 undervoltage lockout upper threshold	$V_{5\ UVLO\ HIGH}$	Guaranteed by design		4.6	4.75	V
LDO5 undervoltage lockout lower threshold	$V_{5\ UVLO\ LOW}$	Guaranteed by design	3.8	4.0		V
Internal reference voltage	V_{ref}		1.225	1.25	1.275	V
V_{IN} undervoltage lockout upper threshold	$V_{IN\ UVLO\ HIGH}$			8.4	8.5	V
V_{IN} undervoltage lockout lower threshold	$V_{IN\ UVLO\ LOW}$		6.6	7.2		V
Internal oscillator frequency	f_{osc}		2.33	2.4576	2.58	MHz
DIGITAL I/O						
High level logic threshold	$V_{T(HIGH)}$				2.0	V
Low level logic threshold	$V_{T(LOW)}$		0.4			V

7.0 Electrical Characteristics (cont.)

V_{IN} = 24 V, 0°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LDO3 LINEAR REGULATOR						
Line regulation		9 V ≤ V_{IN} ≤ 28 V, I_{LDO3} = 20 mA			165	mV
Load regulation		V_{IN} ≤ 24 V, I_{LDO3} = 20 mA		165	300	mV
Maximum output current		V_{LDO3} > $V_{IN\ UVLO,ON}$		60	100	mA
LDO5 LINEAR REGULATOR						
Line regulation		9 V ≤ V_{IN} ≤ 28 V, I_{LDO5} = 5 mA			250	mV
Load regulation		V_{IN} ≤ 24 V, I_{LDO5} = 5 mA		480	1150	mV
Maximum output current		V_{LDO5} > $V_{IN\ UVLO,ON}$		5	10	mA
CURRENT GENERATION SECTION						
Current balance		Per channel ILED = 120mA	-2		2	%
LED channel current range, local dimming (High side is adaptive switch adjustable range)		$I_{PEAK,\ SINK}$	32		192	mA
LED channel current range, scanning mode (High side is adaptive switch adjustable range)		$I_{PEAK,\ SINK}$	32		308	mA
Current rise time		20% to 80% LED current, dependent on PCB and LED cable. Guaranteed by design		100		ns
Current fall time		80% to 20% LED current, dependent on PCB and LED cable. Guaranteed by design		100		ns
PWM linear dimming range		10-bit resolution	1		99	%
PWM dimming range		10-bit resolution	0		99.9	%
PWM resolution		Minimum resolution required to ensure smooth brightness transitions	10			bits
Number of strings		Desirable to run at high frequency to avoid audible noise and banding/shimmering (waterfall) effects			32	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM dimming frequency		NTSC mode - Desirable to run at high frequency to avoid audible noise and banding/shimmering (waterfall) effects. Step = 120 Hz	120		2.4k	Hz
		PAL mode: Step = 100Hz	100		2.4k	Hz
		3D Game mode: Step = 96Hz	96		2.4k	Hz
Junction Temperature		Normal operation temperature range	-40		150	°C
Storage Temperature		Storage temperature range	-40		150	°C
Thermal Resistance Junction-to-Ambient	θ_{JA}	Common Air Flow Speed = 0 m/sec			50	°C/W
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_{SHDN}	Thermal shutdown/Turn-off temperature		145		°C
Thermal shutdown hysteresis				30		°C
Feedback Pins						
FBx, min		FBx minimum voltage VDAC = 00, No loading	200	240	260	mV
FBx, max		FBx maximum voltage VFAC = FF, No loading	2.45	2.55	2.65	V
FBx Sink		When FBx varies by 1% of its unloaded target value			100	µA
FBx Source		When FBx varies by 1% of its unloaded target value			100	µA

8.0 Functional Block Diagram

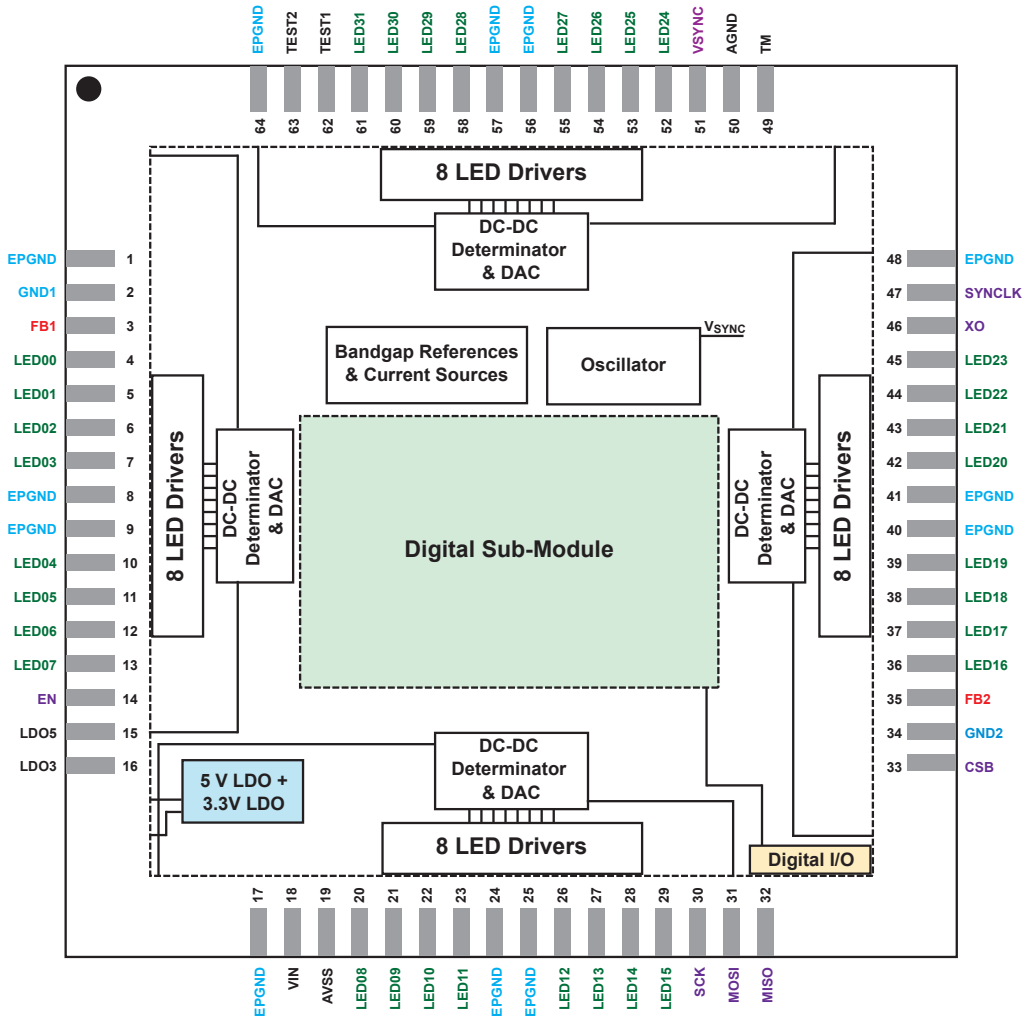


Figure 8.1. iW7032 Functional Block Diagram

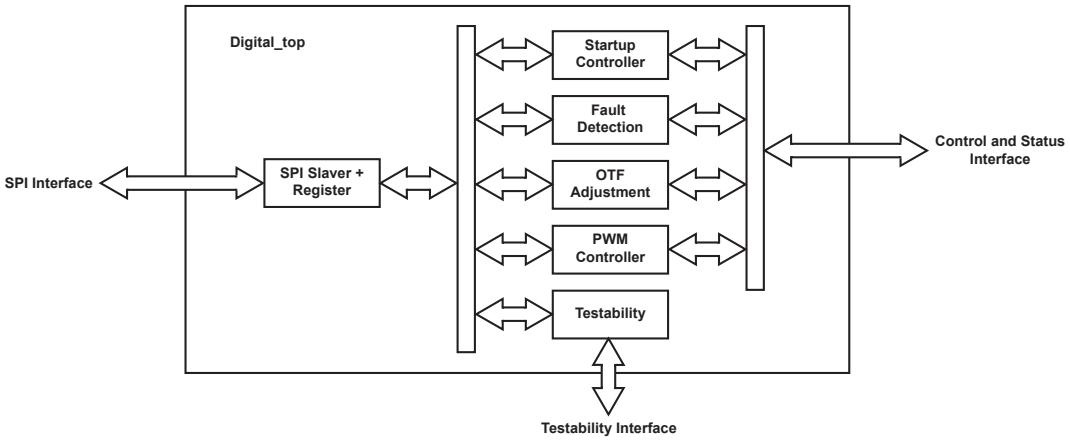


Figure 8.2. Digital Sub-module Functional Block Diagram

9.0 Operation Description

9.1 Adaptive Switching Algorithm

Adaptive switch mode current regulation improves the power efficiency by programmatically controlling the Low Drop Output (LDO) current regulation string in each channel to an optimum level which minimizes the differences in total voltage drop across each string (sharing the same LED power supply) while still minimizing the current differences in each string, thereby maintaining the reliability requirement for the LED component with peak current limit control. The adaptive switch mode also modifies the PWM duty cycle as necessary to automatically compensate for the allowed variances in the LDO current settings.

The following figure illustrates the power loss improvement that is obtained using the adaptive switch method.

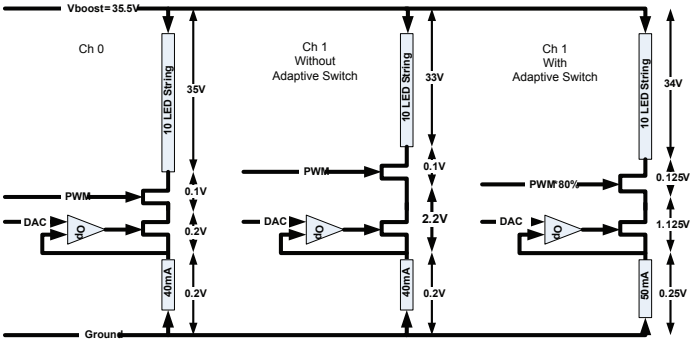


Figure 9.1. Power Loss Improvement Through Adaptive Switch Method

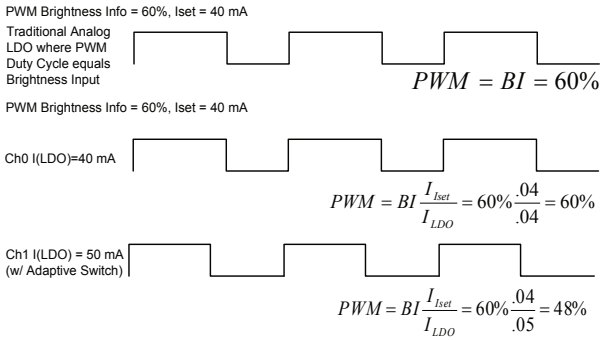
This is carried out by an adaptive channel balance algorithm performed during the power up sequence (referred to as calibration) where the LDO current setting of each channel is incremented while monitoring the multiple voltage potentials on the LDO regulation loop to determine when the loop is in the optimal operation point at the interface between the current regulation and non-regulation regions.

Each channel includes an LDO current regulator controlled by a 4-bit DAC which creates the reference voltage for its LDO. This 4-bit DAC is under control of the digital adaptive switch algorithm controller. The value of the LDO DAC can be observed in the register set where it is called “IDAC”.

This is initially performed during calibration. The optimal DAC settings are retained and updated as necessary by the digital controller. The operation point for each channel is monitored in real time for continued adaptive switch mode regulation for each LED string during normal operation.

This allows compensation for the total forward voltage drop differences such that the same current and on-time product can be maintained with different current and PWM dimming code settings as necessary to match the brightness of each string while minimizing the power dissipation within the LDO circuits.

The following illustration demonstrates the numerical PWM on time compensation that is provided to maintain constant peak current and PWM on time product proportional to the brightness input.



Wave Form and Timing Demonstration of PWM Duty Cycle Compensation for Variation In I(LDO) for each channel.

Figure 9.2. PWM Duty Cycle Compensation

In addition to maintaining a constant peak current and PWM on time product proportional to the desired brightness setting, the algorithm also provides luminance compensation and temperature compensation.

The following figure is a typical transfer function showing the relationship between optical luminance and forward current in an LED.

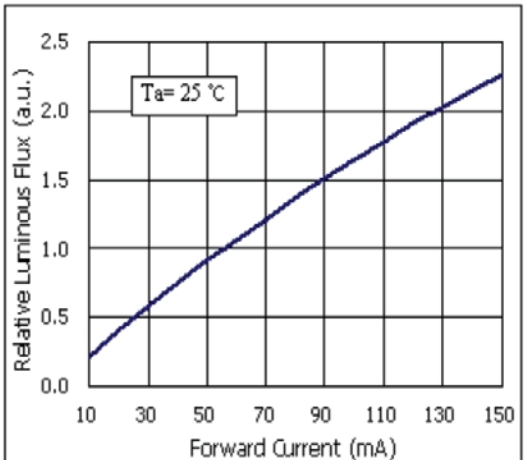


Figure 9.3. Optical Luminance vs. Forward Current in an LED

This luminance can be fit reasonably well with the following function.

$$lum(x) = c_1 x + c_0 \qquad \textit{(eq 9.1)}$$

To compensate for this luminous efficiency reduction in this application where brightness control is more important than current control, when the luminance compensation enable bit is set in the SPI interface register, the Luminance Control Module is modified to replace the following equation:

$$PWM\_out = PWM\_in \frac{I_{SET}}{I_n} \qquad \textit{(eq 9.2)}$$

With the following one:

$$PWM\_out = PWM\_in \frac{lum(I_{SET})}{lum(I_n)} \qquad \text{(eq 9.3)}$$

To optimize the storage of information and maximize the accuracy, C_1, and C_0 must be multiplied by 2^{10} , and 2^0 respectively.

Based on the curve given for an LED of interest, scale the curve to occupy as close to, but not more than 2000 vertical units and as close to but no more than 1500 horizontal units.

Now take 2 x-y pairs of data, one from the far left side, and one from the far right side of the curve.

The following is a curve of a diode after it has been scaled as described above.

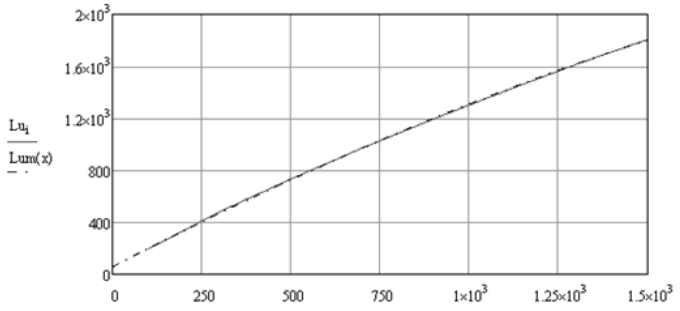


Figure 9.4. Scaled Diode Curve

From this graph, one might capture the following points:

I	*Lu*
100	191
1500	1809

Table 9.1

The coefficients are calculated as follows:

$$C_1 = \frac{Lu_2 - Lu_1}{I_1 - I_2} \qquad \text{(eq 9.4)}$$

$$C_0 = Lu_2 - C_1 I_2 \qquad \text{(eq 9.5)}$$

Using this technique, the results are calculated as follows:

$$Lum\_c1 = 2^{10} C_1 = 2^{10}(1.1557) = 1183 \qquad \text{(eq 9.6)}$$

$$Lum\_c0 = C_0 = 75 \qquad \text{(eq 9.7)}$$

The above numbers are decimal values that are directly used in Lum_c1 and Lum_c0.

Current luminance compensation is based on 1st order correction formula, and it might be upgraded into 2nd order transfer function in a future release.

9.2 Calibration

In order to reduce the in rush current, calibration is based on 5% dimming ratio for scanning mode and 10% dimming ratio for local dimming mode calibration by default. The calibration dimming ratio for local dimming can be adjusted by programming the brightness registers, and the calibration dimming ratio for scanning mode is always the half dimming ratio for local dimming. If the dimming ratio for local dimming is programmed less than 6.25%, then the IC internally clamps this ratio to be 6.25%. For scanning mode calibration, the minimum dimming ratio is 3.125%. In addition, the PWM frequency is based on software programmed value and LED string turning on sequence is following the dimming group setting and td_dg registers programmed delay.

Calibration is performed after the SPI initialization is complete and the Boost/Buck voltage has settled for 20 milliseconds allowing for the initial ramp up.

Figure 9.5 below describes the calibration sequence that is performed using VDAC, IDAC, and FORCE_ON.

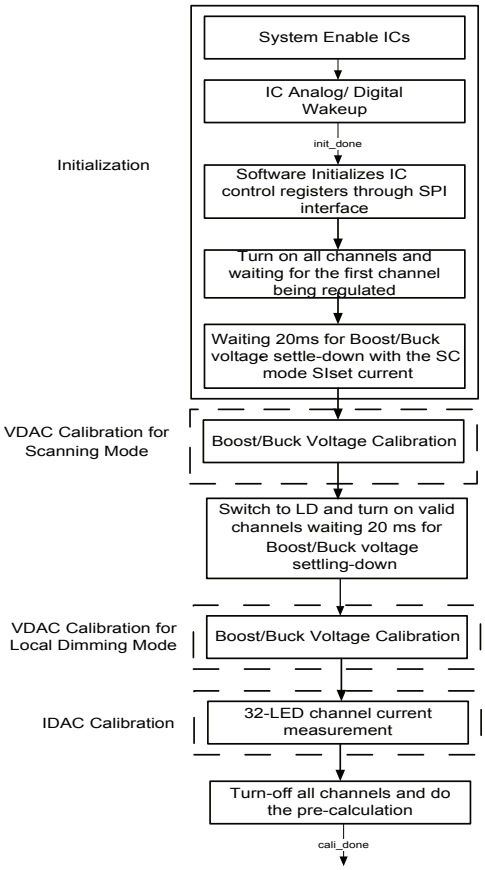


Figure 9.5. Calibration Sequence

Figure 9.6 below describes the sequence used by the firmware to bring up iW7032 to enable calibration.

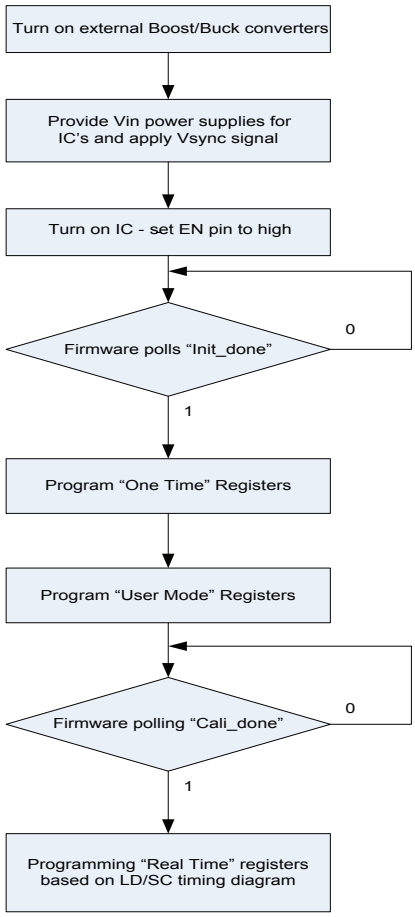


Figure 9.6. Firmware Sequence to Enable iW7032 Calibration

The function of the signals used in calibration are as follows.

VDAC is the digital value (8-bits) that drives the DAC which is used to affect the feedback input to the external Boost/Buck controller.

FORCE_ON is an internally generated digital signal from the LDO regulator that indicates whether or not the LDO is operating in the specified regulation. If it comes out of regulation, the FORCE_ON signal goes true.

There are two 8-bit DAC's used for adjustment of the Boost/Buck calibration; one for each of the two possible Boost/Buck groups. The following sequence is performed for each Boost/Buck group, one group at a time.

The VDAC is in tri-state mode before the software initializes the IC control register through the SPI interface. Once the software completes initializing the IC, the VDAC setting is set to 0 by default which will cause the Boost/Buck regulator

to settle at its highest possible setting to start out the calibration sequence.

At this point, after the Boost/Buck voltage is ramped up, all the channels should indicate that they are in regulation through their individual LDOs FORCE_ON signal. There is a regulation detector on the LDO regulation loop that monitors multiple voltage potentials to ensure that the regulation is operating with enough loop gain for guaranteeing regulation and best efficiency. When the loop gain falls below the lower-bound limit threshold, this indicates that the channel is about to go out of regulation due to not having enough Boost/Buck voltage head room for that channel. With the Boost/Buck voltage at the maximum level, all channels should be in regulation, and therefore this regulation detector output called FORCE_ON should not be true.

For each group, the VDAC is increased 4 LSB at a time at 2 millisecond intervals by default, in a ramp decreasing the Boost/Buck voltage. This occurs until one channel within the Boost/Buck group indicates that it is coming out of regulation. This is sequentially done for every Boost/Buck group.

Then the VDAC output is decreased which increases the Boost/Buck voltage at 1 LSB per 2 millisecond interval, by default, until the FORCE_ON comparator output deactivates. This is also accomplished for each Boost/Buck group. With 2 Boost/Buck groups and 256 possible steps for each one, the maximum time for this operation is just over 0.25 seconds, but will most often be shorter since each VDAC does not need to ramp the full distance. The above estimate is based on SISET being larger than or equal to ISET. If this is not true, the time can, under some circumstances, be a little longer.

After completing this function with the Scanning Mode ISET current setting, the whole process of VDAC calibration is repeated using the Local Dimming Mode current settings.

Once the VDAC calibration is completed, a similar function occurs with each IDAC. IDAC is the digital value (4-bits) that drives the DAC for each channel controlling the LDO current for the adaptive switching operation. This DAC is seen for each channel in figure 9.1. Initially all of the IDAC settings for the individual LDO's are set to 0, meaning that each channel is set up to operate at the current specified by the ISET bits in the SPI interface. Now that the Boost/Buck voltage is set to its ideal point where the weakest channel within the Boost/Buck group is in regulation. One-by-one, each channel will be adjusted within the Boost/Buck group by incrementing the IDAC value one bit at a time at 1 bit per 4.5 microseconds while again monitoring the FORCE_ON comparator output to determine when the LDO transistor moves deeper inside the triode region indicating that it is about to go out of regulation due to the current demand exceeding that which is feasible with the previously adjusted boost voltage. After the FORCE_ON comparator activates, then the IDAC value is reduced again by one step at a time until it deactivates again.

The calibration can be bypassed by setting cali_cfg to be HIGH. If calibration is bypassed, 2-set internal VDACs for LD & SC are automatically loaded from VDAC_LD and VDAC_SC. The control flow to bypass calibration is shown below.

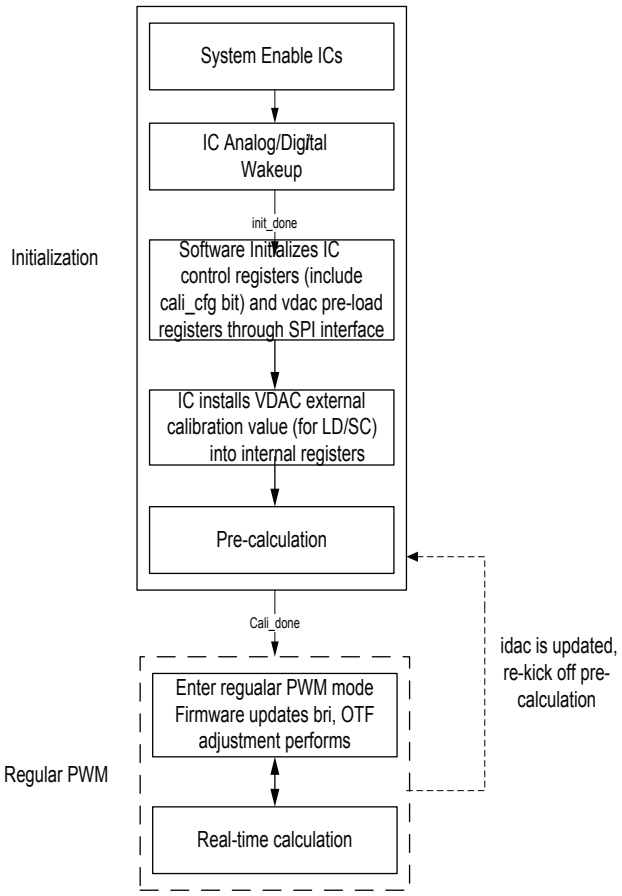


Figure 9.7. Control Flow to Bypass Calibration

9.3 Channel Grouping

Channel grouping allows multiple LED ports on the iW7032 IC to be connected together to one string of LED's at a higher current rating at the cost of a reduction in number of strings controlled by a single iW7032 IC. For example, if the LED string current is to operate at 240 mA per string, the channel grouping can be set to 2 while the LDO Iset

value is set to 120mA. By wiring the channels together in groups of two, the total output current per group will be 240 mA. However, the number of available strings will be 32/2 = 16 strings.

The iW7032 channels which are connected together to drive one string of LED's are called one channel group.

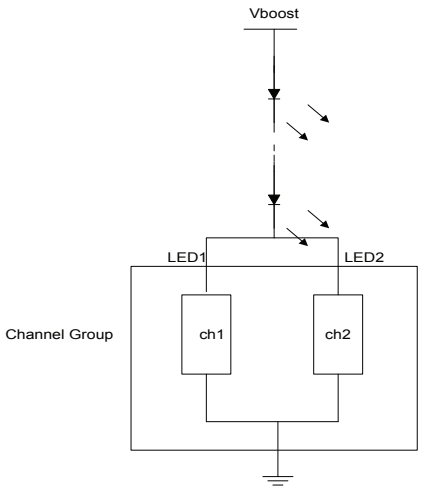


Figure 9.8. Channel Group

In order to use this feature, it is still necessary to write the dimming value individually to every channel as it is to be updated from video frame-to-frame.

It is necessary that the channel group must be set such that an integer number of them occur in both the dimming group size and the Boost/Buck group size. The iW7032 is notified of the channel group through the SPI register at address 0xa2 bits 8 as follows:

Bit[8] of REG_0a2

Cg_cfg: ⇨ 0: 1channel for one channel group (default)

⇨ 1: 2 channels for one channel group

When the channel grouping is configured to be 2 channels per string, initial adaptive switch calibration is fully functional.

9.4 Boost/Buck Grouping

The channels of iW7032 that are connected to the same external Boost/Buck converter belong to one Boost/Buck group. The iW7032 supports up to two Boost/Buck groups. The number of channels belonging to one Boost/Buck group can be programmed by bg_cfg bit in bit [0] of REG_0a3. Two types of Boost/Buck groups are provided in iW7032, and they are 16, and 32 channels per Boost/Buck group for settings 0 and 1, respectively.

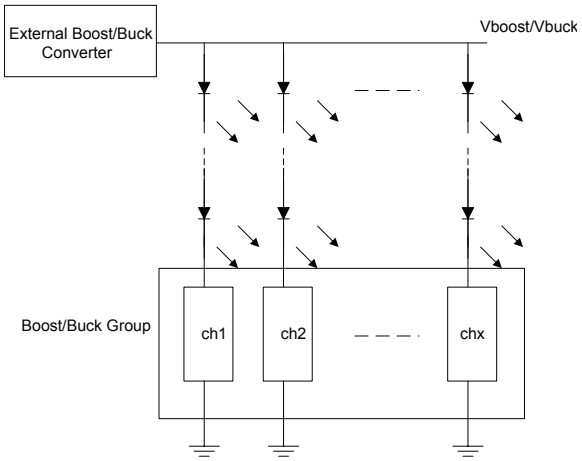


Figure 9.9. iW7032 Boost/Buck Groups

9.5 On-the-Fly Automatic Operation

When the adaptive switch control register bit REG_0a0 and the on-the-fly (OTF) control register bit in REG_0a0 are enabled, internal VDAC and IDAC control values can be automatically adjusted based on the LED current regulation current and voltage adjustment head room for optimum thermal performance.

10.0 Protection Description

The iW7032 monitors the behavior of each LED driver continuously. When fault conditions are observed, the iW7032 will turn off either the whole IC or the driver channel associated with the observed fault. There are two types of fault protection during startup – LED open and over-temperature, and three types continuous protection during normal operation – LED open, LED short, and over-temperature.

The three types of continuous protection are described in detail as follows:

1. LED_Open: While the iW7032 is operating, if a single LED string becomes open and its corresponding LED driver senses no current for eight consecutive vsync periods, the LED driver for this channel will be disabled causing the system to not request higher voltage from external DC-DC converter. In this state, the iW7032 will set bit 1 of SPI register 0x100. There is an automatic recovery feature from the LED_Open fault condition. When auto-recovery control register bit in REG_0a3 is enabled and the channel has been determined to be at fault, it can be enabled again within 0.5 secs once it meets Auto-Recovery criteria without the system being powered up again.
2. LED_Short (enough LEDs are shorted in an LED string): The iW7032 has accurate matching for each current source. However, the forward voltage of each LED string can vary significantly from channel to channel sharing the same Boost/Buck voltage power supply (within the same Boost/Buck group). The total voltage difference in each string results in additional power loss within the IC. For better efficiency, the voltage difference between lowest voltage string and highest voltage string is chosen to be less than 5.5 V (or 8.0 V programmable). If this condition is found to be false for eight consecutive vsync periods, the internal LED short protection circuit disables the string with the lowest forward biased voltage drop (which has the highest voltage at the pin). For example, when the iW7032 is started up, the LED pin voltage for the channel with the largest forward biased voltage drop should be about 0.6V. Therefore, if any LED pin has a voltage higher than 5.5V (or 8.0V), the corresponding LED string voltage is 4.9V (or 7.4V) lower than others. This means two or more LEDs in this LED string are shorted. The corresponding LED driver will then be turned off and the iW7032 will set bit 2 of the SPI register at 0x100. There is no automatic recovery from the LED_Short fault condition. Once a channel has been determined to be at fault, it is disabled until the system is powered up again.
3. OT (Over-Temperature Protection): OT is used to monitor if the die surface temperature is around 145°C. Once OT is triggered, the LED drivers are disabled allowing the part to cool down. Bit 0 of SPI register 0x100 is also set. After the temperature falls below around 115°C, the iW7032 resumes normal operation. This fault condition is not qualified for multiple vsync periods as the other two faults are. When this fault condition recovers, the iW7032 will re-perform calibration but does not require software re-initialization.

11.0 Input and Output Equivalent Circuits

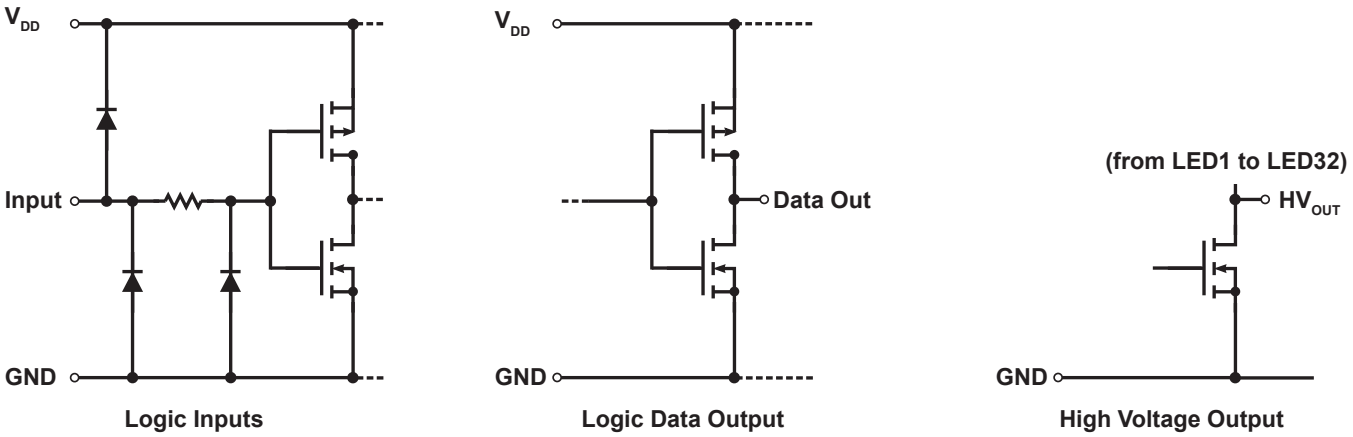


Figure 11.1. Input and Output Equivalent Circuits

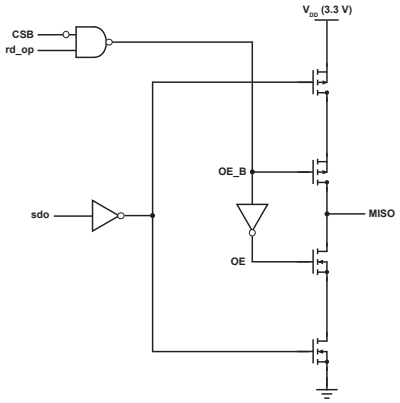


Figure 11.2. MISO Output Driving Circuit (tri-state)

12.0 Control Register Table

Due to the PWM resolution of the 10 bits, all the control registers are based on a 10-bit address and data scheme.

12.1 Control Register Mapping Table

Address	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Real-Time Update Control Registers (Frame based)										
0x000		Dim_mode					Temp_trk_en	Led_temp_comp[2]	Led_temp_comp[1]	Led_temp_comp[0]
0x001	Bri1[9]	Bri1[8]	Bri1[7]	Bri1[6]	Bri1[5]	Bri1[4]	Bri1[3]	Bri1[2]	Bri1[1]	Bri1[0]
0x002	Bri2[9]	Bri2[8]	Bri2[7]	Bri2[6]	Bri2[5]	Bri2[4]	Bri2[3]	Bri2[2]	Bri2[1]	Bri2[0]
:			:	:	:	:	:	:	:	:
0x01f	Bri31[9]	Bri31[8]	Bri31[7]	Bri31[6]	Bri31[5]	Bri31[4]	Bri31[3]	Bri31[2]	Bri31[1]	Bri31[0]
0x020	Bri32[9]	Bri32[8]	Bri32[7]	Bri32[6]	Bri32[5]	Bri32[4]	Bri32[3]	Bri32[2]	Bri32[1]	Bri32[0]
Address 0x041-0x04f (Reserved)										
Real-Time Update Control Registers (User Operation Mode based)										
0x050	Tv_mode[1]	Tv_mode[0]		Scan_duty[4]	Scan_duty[3]	Scan_duty[2]	Scan_duty[1]	Scan_duty[0]	SVsync_cfg[1]	SVsync_cfg[0]
0x051						Pwm_freq[4]	Pwm_freq[3]	Pwm_freq[2]	Pwm_freq[1]	Pwm_freq[0]
0x052	Td0[9]	Td0[8]	Td0[7]	Td0[6]	Td0[5]	Td0[4]	Td0[3]	Td0[2]	Td0[1]	Td0[0]
0x053							Td0[13]	Td0[12]	Td0[11]	Td0[10]
0x054	Td_dg1[9]	Td_dg1[8]	Td_dg1[7]	Td_dg1[6]	Td_dg1[5]	Td_dg1[4]	Td_dg1[3]	Td_dg1[2]	Td_dg1[1]	Td_dg1[0]
0x055						Td_dg1[14]	Td_dg1[13]	Td_dg1[12]	Td_dg1[11]	Td_dg1[10]
0x056	Td_dg2[9]	Td_dg2[8]	Td_dg2[7]	Td_dg2[6]	Td_dg2[5]	Td_dg2[4]	Td_dg2[3]	Td_dg2[2]	Td_dg2[1]	Td_dg2[0]
0x057						Td_dg2[14]	Td_dg2[13]	Td_dg2[12]	Td_dg2[11]	Td_dg2[10]
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
0x092	Td_dg32[9]	Td_dg32[8]	Td_dg32[7]	Td_dg32[6]	Td_dg32[5]	Td_dg32[4]	Td_dg32[3]	Td_dg32[2]	Td_dg32[1]	Td_dg32[0]
0x093						Td_dg32[14]	Td_dg32[13]	Td_dg32[12]	Td_dg32[11]	Td_dg32[10]
:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:
0x129		Ld_vdac_ld	Vdac_ld[7]	Vdac_ld[6]	Vdac_ld[5]	Vdac_ld[4]	Vdac_ld[3]	Vdac_ld[2]	Vdac_ld[1]	Vdac_ld[0]
0x12a		Ld_vdac_sc	Vdac_sc[7]	Vdac_sc[6]	Vdac_sc[5]	Vdac_sc[4]	Vdac_sc[3]	Vdac_sc[2]	Vdac_sc[1]	Vdac_sc[0]
Address 0x093-0x09f (Reserved)										

12.1 Control Register Mapping Table (cont.)

Address	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Initial One-Time Update Control Registers - *These functions can be changed on the fly, but it is not recommended unless some reduced picture quality and performance can be tolerated for up to 4 frames.*										
0x0A0	Apt_sw_en	Otf_apt_en	Lum_trk_en							
0x0A1	ext_clk_en	Vled_short	Call_cfg	Call_time_step	Iset[5]	Iset[4]	Iset[3]	Iset[2]	Iset[1]	Iset[0]
0x0A2		Cg_cfg			SIset[5]	SIset[4]	SIset[3]	SIset[2]	SIset[1]	SIset[0]
0x0A3	Lu_c1[1]	Lu_c1[0]	Auto_rcv_en		Apt_sw_cfg[1]	Apt_sw_cfg[0]	Pwm_mdl_cfg[1]	Pwm_mdl_cfg[0]		Bg_cfg
0x0A4	Lu_c1[11]	Lu_c1[10]	Lu_c1[9]	Lu_c1[8]	Lu_c1[7]	Lu_c1[6]	Lu_c1[5]	Lu_c1[4]	Lu_c1[3]	Lu_c1[2]
0x0A5	Lu_c0[9]	Lu_c0[8]	Lu_c0[7]	Lu_c0[6]	Lu_c0[5]	Lu_c0[4]	Lu_c0[3]	Lu_c0[2]	Lu_c0[1]	Lu_c0[0]
Address 0x0A6-0x0ff (Reserved)										

Status Registers										
0x100					cali_done	Init_done		Led_short	Led_open	OT
0x101	ch_en[9]	ch_en[8]	ch_en[7]	ch_en[6]	ch_en[5]	ch_en[4]	ch_en[3]	ch_en[2]	ch_en[1]	ch_en[0]
0x102	ch_en[19]	ch_en[18]	ch_en[17]	ch_en[16]	ch_en[15]	ch_en[14]	ch_en[13]	ch_en[12]	ch_en[11]	ch_en[10]
0x103	ch_en[29]	ch_en[28]	ch_en[27]	ch_en[26]	ch_en[25]	ch_en[24]	ch_en[23]	ch_en[22]	ch_en[21]	ch_en[20]
0x104		Led_short_idx[4]	Led_short_idx[3]	Led_short_idx[2]	Led_short_idx[1]	Led_short_idx[0]			ch_en[31]	ch_en[30]
0x105			Idac2[3]	Idac2[2]	Idac2[1]	Idac2[0]	Idac1[3]	Idac1[2]	Idac1[1]	Idac1[0]
:			:	:	:	:	:	:	:	:
0x114			Idac32[3]	Idac32[2]	Idac32[1]	Idac32[0]	Idac31[3]	Idac31[2]	Idac31[1]	Idac31[0]
0x115						Led_open_idx[4]	Led_open_idx[3]	Led_open_idx[2]	Led_open_idx[1]	Led_open_idx[0]
0x116			Vdac1[7]	Vdac1[6]	Vdac1[5]	Vdac1[4]	Vdac1[3]	Vdac1[2]	Vdac1[1]	Vdac1[0]
0x117			Vdac2[7]	Vdac2[6]	Vdac2[5]	Vdac2[4]	Vdac2[3]	Vdac2[2]	Vdac2[1]	Vdac2[0]

12.2 Control Register Bit Field Definitions

Definition	Access	Description
Real-Time Update Control Registers (Frame Based)		
dim_mode	R/W	0: local dimming (default) 1: scanning mode
temp_trk_en	R/W	0: disable temperature-current compensation (default) 1: enable temperature-current compensation
led_temp_comp[2:0]	R/W	LED junction temperature vs. derating of Luminous Flux Density compensation factor (Ct). The equation for LED junction temperature compensation is “PWM_out = PWM_in / Ct”. This compensation factor is defined as follows: 0: Ct = 0.79; 1: Ct = 0.82; 2: Ct = 0.85; 3: Ct = 0.88; 4: Ct = 0.91; 5: Ct = 0.94; 6: Ct = 0.97; 7: Ct = 1.00 (default)
bri1[9:0] to bri32[9:0]	R/W	10-bit brightness setting for each of the 32 LED channels, adjusting brightness in 1024 steps. Please refer to “The Brightness Register vs. On Duty Table” to get the exact mapping information. Default value is 0x066.

12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Real-Time Update Control Registers (User Operation Mode Based)		
tv_mode[1:0]	R/W	0: NTSC mode, vsync frequency is 120Hz, 240Hz or 480Hz (default) 1: PAL mode, vsync frequency is 100Hz, 200Hz or 400Hz 2: 3D game mode, vsync frequency is 96Hz, 192Hz or 384Hz 3: NTSC mode
vsync_cfg[1:0]	R/W	*If TV is in NTSC mode:* 0: VSYNC = 120Hz (default) 1: VSYNC = 240Hz 2: VSYNC = 480Hz 3: the same as 0 *If TV is in PAL mode:* 0: VSYNC = 100Hz (default) 1: VSYNC = 200Hz 2: VSYNC = 400Hz (scanning mode) 3: the same as 0 *If TV is in 3D Game mode:* 0: VSYNC = 96Hz (default) 1: VSYNC = 192Hz 2: VSYNC = 384Hz 3: the same as 0 PWM frequency needs to be programmed to be equal or slower than svsync frequency The default value is 0
scan_duty[4:0]	R/W	0: 20% 1: 24% ….. 5: 40% (default) ….. 20: 100% (Any number greater than this results in 100%) This Scanning Mode dimming ratio may be slightly adjusted by the IC internally in order to meet the requirement of Tsc being the integer number of the dimming period (please refer to the Scanning mode timing diagram). Please note that for thermal reasons, it is not recommended in most cases to use more than 50% scan duty unless the scan duty SISET value is not set higher than the local dimming (LD) current setting.

12.2 Control Register Bit Field Definitions (cont.)

Definition	Access	Description
Real-Time Update Control Registers (User Operation Mode Based) (cont.)		
pwm_freq[4:0]	R/W	*If TV is in NTSC mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 20 steps. 0 - 120Hz to 19 - 2.4kHz with 120Hz per step *If TV is in PAL mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 24 steps. 0 - 100Hz to 23 - 2.4kHz with 100Hz per step *In TV is in 3D game mode:* 5-bit PWM dimming frequency setting, adjusting frequency in 25 steps. 0 - 96Hz to 24 - 2.4kHz with 96Hz per step The default value is 0
td0[13:0] (tsd0[13:0])	R/W	The timing delay from vsync rising edge to the first scan line updating the brightness on TV. In local dimming mode, it should be programmed as td0; in scanning mode, it should be programmed as tsd0. The default value is 0
td_dg1[14:0] to td_ dg32[14:0] (tsd_dg1[14:0] to tsd_ dg32[14:0])	R/W	The timing delay from vsync rising edge to the dimming ratio updating for each channel. The default values are 0. In local dimming mode, this set of registers should be programmed as td_ dg1[14:0] ~ td_dg32[14:0]; in scanning mode, it should be programmed as tsd_dg1[14:0] ~ tsd_dg32[14:0]. td0 is always equal to or less than td_dg1
ld_vdac_ld	R/W	ld_vdac_ld: (Allows for writing of vdac values) 1: load both vdac values from vdac1 for LD mode 0: vdac1 is read only, and reflects the value of vdac1 Note: When this bit is left as a 1, the value of VDAC is frozen at the value that was written to it when it was set to 1. When writing to this bit with a 0, the VDAC becomes read only, and if free to adjust by normal on the fly operations.
ld_vdac_sc	R/W	ld_vdac_sc: 1: load both vdac values from vdac2 for SC mode 0: vdac2 is read only, and reflects the value of vdac2 Note: When this bit is left as a 1, the value of VDAC is frozen at the value that was written to it when it was set to 1. When writing to this bit with a 0, the VDAC becomes read only, and if free to adjust by normal on the fly operations.
vdac_ld[7:0]	W	If ld_vdac_ lc is **HIGH**, it is the value loaded into vdac1 and vdac2 for local dimming mode. The default value is 0.
vdac_sc[7:0]	W	If ld_vdac_ sc is **HIGH**, it is the value loaded into vdac1 and vdac2 for scanning control mode. The default value is 0.

Definition	Access	Description
Initial One-Time Update Control Registers - *These features are most often set or changed before calibration; however, they can also be changed on the fly, but their response times are not guaranteed within one frame. Picture quality and thermal performance could be slightly degraded for a few frames just after these items are changed on the fly.*		
apt_sw_en	R/W	0: disable adaptive switch mode (default) 1: enable adaptive switch mode
apt_sw_cfg[1:0]	R/W	0: 24% adaptive switch range in 4% steps (default) 1: 48% adaptive switch range in 4% steps 2, 3: 60% adaptive switch range in 4% steps
otf_apt_en	R/W	0: disable on-the-fly power monitoring and adjustment (default) 1: enable on-the-fly power monitoring and adjustment
lum_trk_en	R/W	0: disable luminance-current compensation (default) 1: enable luminance-current compensation
auto_rcv_en	R/W	0: disable auto-recovery for OPEN fault detection (default) 1: enable auto-recovery for OPEN fault detection
cali_cfg	R/W	0: normal IC calibration (default) 1: bypass IC calibration, firmware uploads vdac values through vdac_ld and vdac_sc registers
cali_time_step	R/W	0: 2ms per vdac calibration time step (default) 1: 10ms per vdac calibration time step Notes: During initiate calibration, if pwm_frequency is programmed to be faster than 500Hz, program this bit to 0; otherwise, program this bit of register to be 1
iset[5:0]	R/W	6-bit control to set the nominal DC current of the LED drivers in local dimming mode 000011 to 011011 for 24 mA with 4 mA steps to 120 mA current Default = 010001 for 80 mA (12 + 17x4 = 80) Note: Can be set to 192mA so long as system ensures that average current does not exceed 120mA.
siset[5:0]	R/W	6-bit control to set the nominal DC current of the LED drivers in scanning mode 000011 to 101101 for 24 mA with 4 mA steps to 192 mA current Default = 011101 for 128 mA (12 + 29x4 = 128)
vled_short	R/W	0: LED short detection threshold = 8.0V (default) 1: LED short detection threshold = 5.5V
ext_clk__en	R/W	0: using internal clock generated clock as the master clock (default) 1: using external system provided clock as the master clock
pwm_mdl_cfg[1:0]	R/W	0: modulate PWM “head shift lighting” based on dimming programming (default) 1: modulate PWM “tail shift lighting” based on dimming programming 2: modulate PWM with “both ends shift lighting” based on dimming programming. In this mode, the PWM cycle is centered around the corresponding delay (td_dgx) 3: the same as “0”
vdac_rvs_en	R/W	0: vdac output is same as digital control valve (default) 1: vdac output is bitwise negative from digital control value
cg_cfg	R/W	Defines channel sharing group configuration 0: 1 channel for one channel group (default) 1: 2 channels for one channel group

Definition	Access	Description
Initial One-Time Update Control Registers (cont'd)		
bg_cfg	R/W	The number of LED channels in one Boost/Buck Group 0: 16 LED channels in one Boost/Buck Group (default) 1: 17 - 32 LED channels in one Boost/Buck Group
lu_c0[9:0] lu_c1[11:0]	R/W	The 1st (2 term) order LED current to luminance nonlinear transfer function coefficient. The transfer function is: $Lum\_Flux(I_f) = C_1 I_f + C_0$ lu_c0 default: 57; lu_c1 default: 1461
Status Registers		
led_short	R	Status bit for the 32 LED channels. If any LED pin has a voltage higher than 5.5v, this means two or more LEDs in this LED string have been shorted together. The *led_short* bit will be set and the corresponding LED driver will then be disabled.
led_short_idx[4:0]	R	The latest shorted LED channel index
led_open	R	Status bit for the 32 LED channels. While iW7032 is working, if some LED string is suddenly open and its corresponding LED driver senses no current at all, the *led_open* bit will be set and the LED driver will be disabled instead of requesting higher voltage from Boost/Buck.
led_open_idx[4:0]	R	The latest open LED channel index
ot	R	Status bit if over temperature fault happens.
init_done	R	Status bit for IC initialization is done; software starts to program the initial one-time control registers to configure the IC.
cali_done	R	Status bit for IC calibration is done; software starts to program the 32-channel real-time registers
ch_en[31:0]	R	Status bit for each of the 32 LED channels. It is used to flag if any LED channel is either enabled (1) or disabled (0) from fault detections.
Idac1[3:0] : Idac32[3:0]	R	4-bit current DAC value for each LED channels
vdac1[7:0]	R	8-bit Boost/Buck voltage DAC value for the first external Boost/Buck converter
vdac2[7:0]	R	8-bit Boost/Buck voltage DAC value for the second external Boost/Buck converter

12.3 Brightness Control Register (R/W) vs. PWM Turn-on Duty Table

Brightness (Bin)	Brightness (Dec)	Bright (Hex)	Duty of Driver Turn-ON Time (%)
00_0000_0000*	0	0	0.00%
00_0000_0001*	1	1	0.10%
……..	…….	……..	……..
00_0000_1001*	9	9	0.88%
00_0000_1010	10	A	0.98%
00_0000_1011	11	B	1.07%
00_0000_1100	12	C	1.17%
00_0000_1101	13	D	1.27%
00_0000_1110	14	E	1.37%
00_0000_1111	15	F	1.46%
……..	…….	……..	……..
01_1111_1111	511	1FF	49.90%
10_0000_0000	512	200	50.00%
10_0000_0001	513	201	50.10%
……..	……..	……..	……..
11_1111_1101	1021	3FD	99.71%
11_1111_1110	1022	3FE	99.80%
11_1111_1111	1023	3FF	99.90%

* Linearity not guaranteed within the shaded area.

13.0 SPI Interface

13.1 SPI Interface Definitions

A Serial Peripheral Interface (SPI) system consists of one master device and one or more slave devices. The master is defined as a microcontroller providing the SPI clock and the slave as any IC receiving the SPI clock from the master. The iW7032 always operates as a slave device in master-slave operation mode.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled with a LOW active Chip Select wire (CSB). Data is transmitted with a 3-wire interface consisting of wires for serial data input MOSI (refer to SDI in figures), serial data output MISO (refer to SDO in figures) and serial clock (SCK).

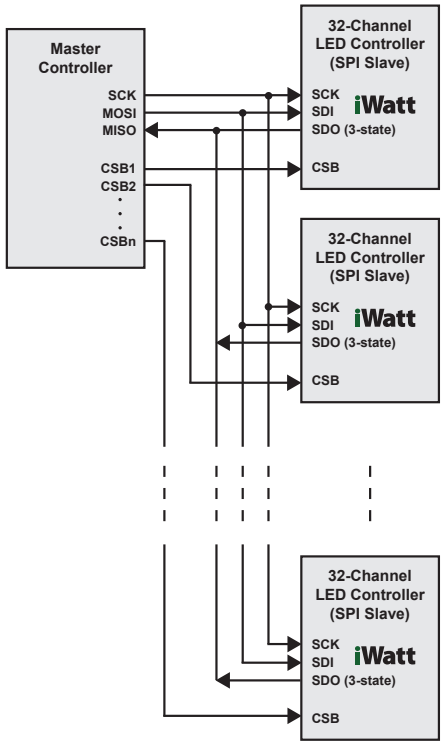


Figure 13.1. Parallel Configuration of Multiple 32-Channel Controllers

The SPI interface in the iW7032 is designed to support any master controller that uses SPI bus. Communication can be carried out by software. The SPI interface is used for IC initialization, the real-time control and monitor purposes. The data transfer uses the following 4-wire interface:

MOSI	Master out slave in	Master controller ⇨ IC
MISO	Master in slave out	IC ⇨ master controller
SCK	Serial clock	Master controller ⇨ IC
CSB	Chip select (low active)	Master controller ⇨ IC

The word width of the SPI interface is defined as 10-bit to facilitate the 10-bit dimming register real-time updating. Each transaction is defined as the three phases - command phase, address phase and data phase. These three phases are sequentially presented in the SPI interface during each transaction.

Command Phase	Address Phase	Data Phase

The Command Phase is composed of 10-bit command transmission; the Address Phase is composed of 10-bit register address transmission; the Data Phase is composed of the integer number of 10-bit word transmission.

The SPI transaction Command Word is defined as follows:

Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	I/R	R/W
Bit 0		0: Read; 1: Write							
Bit 1		0: Address Incremental Burst Access; 1: Address Repetitive Burst Access							

The difference between Incremental Burst vs. Repetitive Burst is if the address is incremental by 1 following each word data access. For Incremental Burst, the register address increments by 1 internally by the iW7032 for each word access; while for Repetitive Burst, the same address register is accessed repeatedly. The Repetitive Burst can be used for IC status register polling by software.

Each transmission starts with a falling edge of CSB and ends with the rising edge. During transmission, commands, address and data are controlled by SCK and CSB according to the following rules:

- Commands, address and data are shifted: MSB first, LSB last.
- Output data bits are shifted out on the falling edge of SCK (MISO line).
- Input bits are sampled on the rising edge of SCK (MOSI line).
- After the device is selected with the falling edge of CSB, a 10-bit command is received. The command defines the operations to be preformed.
- After the 10-bit command is received, a 10-bit register address is received. The address defines the register address to be accessed.

- Data transfer to MOSI continues immediately after receiving the address in all cases when data is to be written to IC internal registers.
- Data transfer out from MISO starts with the falling edge of SCK immediately after the last bit of the SPI command is sampled in on the rising edge of SCK.
- Maximum SPI clock frequency is 16 MHz
- Maximum data transfer speed for real time register access is 2.496 Mbps for up to 8 IC system configuration

13.2 SPI Interface Timing Diagrams

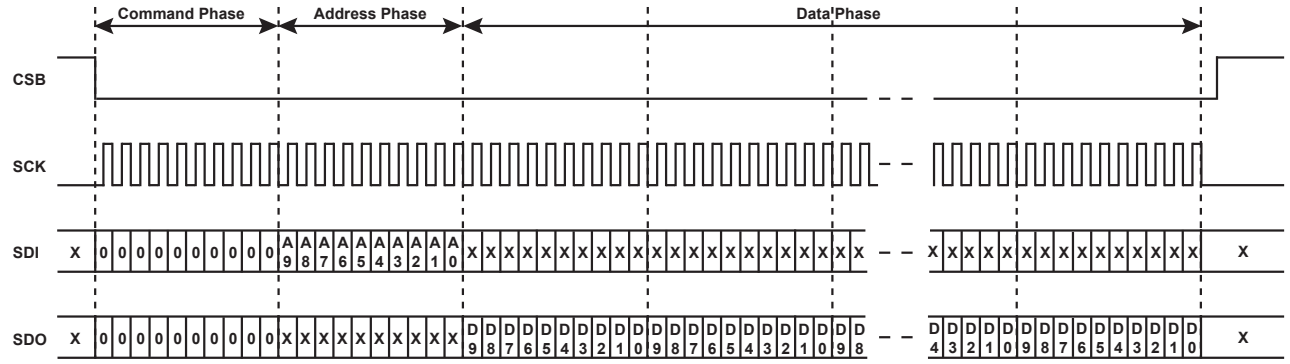
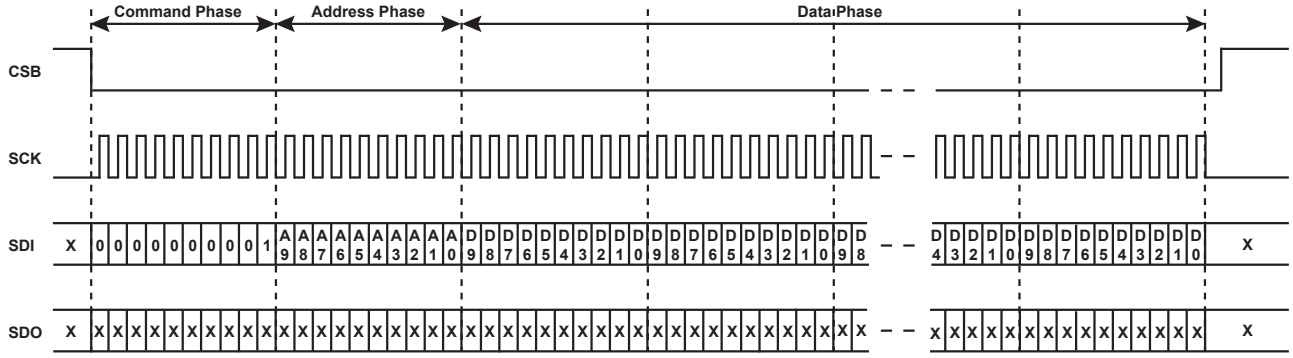


Figure 13.2. Read Mode Transaction Timing Diagram



Software controls how many words to write by stopping to toggle SCK and disable chip select pin.

Figure 13.3. Write Mode Transaction Timing Diagram

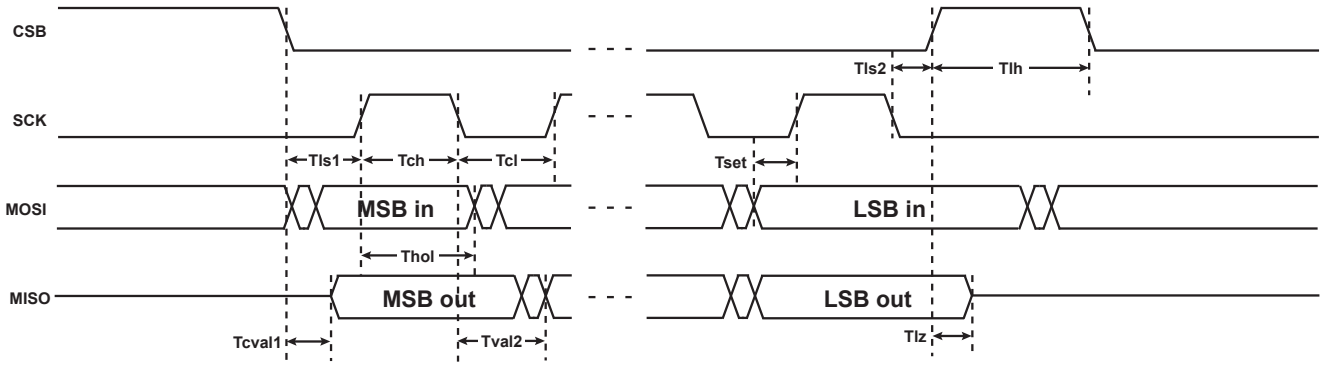


Figure 13.4. SPI Bus Timing Diagram

13.3 AC Parameters of the SPI Interface

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TERMINAL CSB, SCK						
Time from CSB (10%) to SCK (90%)	t_{LS1}		25			ns
Time from SCK (10%) to CSB (90%)	t_{LS2}		25			ns
SCK low time	t_{CL}	MISO Load capacitance < 100 pF	30			ns
SCK high time	t_{CH}	MISO Load capacitance < 100 pF	30			ns
TERMINAL MOSL, SCK						
Time from changing MOSI (10%, 90%) to SCK (90%) Data setup time	t_{SET}		12.5			ns
Time from SCK (90%) to changing MOSI (10%, 90%) Data hold time	t_{HOL}		12.5			ns
TERMINAL MISO, CSB						
Time from CSB (10%) to stable MISO (10%, 90%)	t_{VAL1}	MISO load capacitance < 150 pF	17.5			ns
Time from CSB (90%) to high impedance state of MISO	t_{LZ}	MISO load capacitance < 150 pF	17.5			ns
TERMINAL MISO, SCK						
Time from SCK (10%) to stable MISO (10%, 90%)	t_{VAL2}	MISO load capacitance < 150 pF			25	ns
TERMINAL CSB						
Time between SPI cycles, CSB at high level (90%)	t_{LH}		250			ns

14.0 Dimming Mode Control and Timing

The iW7032 supports two real-time dimming control modes – Local Dimming Mode and Scanning Mode.

Local Dimming Mode enables the LED backlight to be turned off in dark image areas, increasing the dynamic contrast ratio. Scanning Mode eliminates the flicker and ghosting problems (motion blur) associated with large-screen LCD TVs.

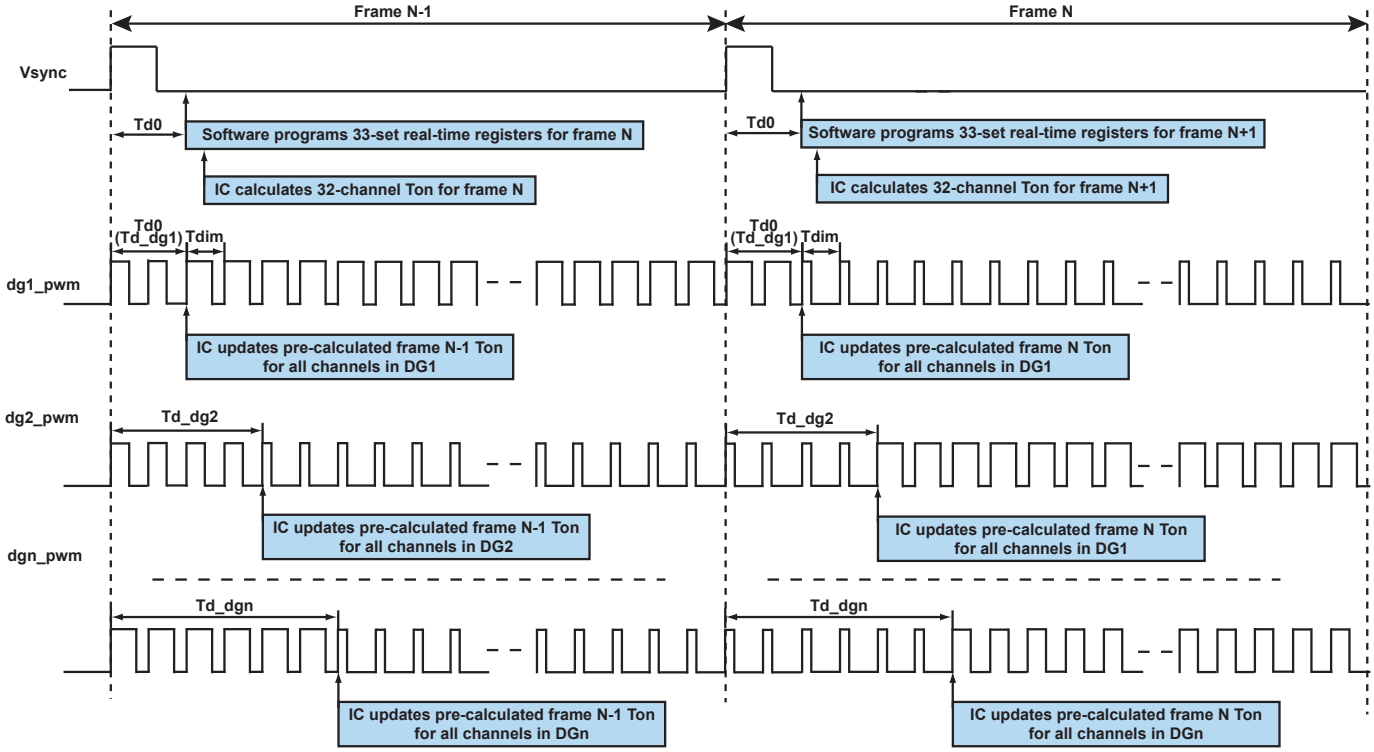


Figure 14.1. Local Dimming Mode Timing Diagram

Td0: Delay time for DG1 updated after Vsync. It is a control register which is programmed by software. For the multiple iW7032 chip solution for a TV system, Td0 is equal to the td_dg1 for the first iW7032 chip programming.

Td_dgn: Delay time for DGn update after Vsync. It is one of the td_dg1 ~ td_dg32 registers setting.

Tdim: it is the dimming period, which can be calculated by the configuration register pwm_freq[4:0]. Ton calculation by the iW7032 is pipelined by programming the dimming register. When the first channel dimming register is updated, the iW7032 initiates the calculation for this channel's Ton immediately. This allows the dimming register programming and Ton calculation to be overlapped in time, saving both the SPI and calculation bandwidth.

For single IC system solutions, software needs to program 33-set real time registers for the N+1 frame at td0 delay of N frame. The IC manages all 32-channel Ton calculations, pre-calculated Ton buffering, and Ton updating at the right timing.

For multiple IC system solutions, software needs to program 33-set real time registers sequentially for all ICs for the N+1 frame at td0 delay of N frames. Each IC starts the Ton calculation when the first dimming register belonging to this IC is updated.

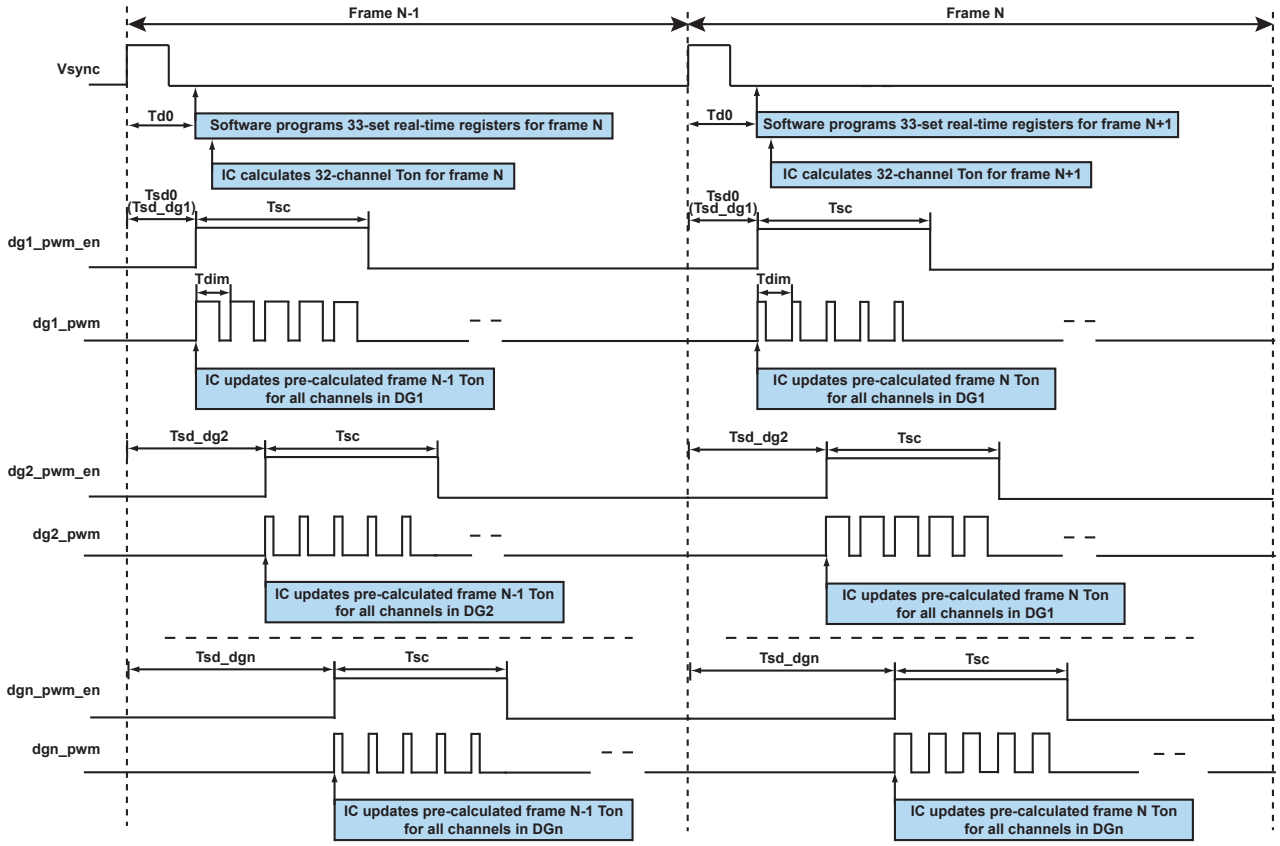


Figure 14.2. Scanning Mode Timing Diagram

Tsd0: Delay time for DG1 updated after SVsync. This is a control register which is programmed by the system software. For the multiple iW7032 chip solution for a TV system, Tsd0 is equal to the tsd_dg1 for the first iW7032 chip programming.

Tsd_dgn: Delay time for DGn update after SVsync. This is one of the tsd_dg1 ~ tsd_dg32 registers setting

Tdim: This is the dimming period, which can be calculated by the configuration register pwm_freq[4:0].

Tsc: This is the scanning mode first-order dimming period. The iW7032 supports scan duty configurations by 5-bits which range from 20% to 100% scan duty in 4% steps. The scan duty cycle is a percentage of the vsync cycle time. In order to meet “Tsc = n•Tdim, n is an integer”. Tsc is adjusted slightly internally by the iW7032 to meet n•Tdim requirement. For example, if SVsync is 240 Hz, and this first-order dimming is set to be 32%, and Tdim is programmed to be 2.4 kHz, from the calculation, Tsc/Tdim = (0.32/240)/(1/2400) = 3.2. In this example, design will round this ratio to be the nearest integer, that is 3, and the real dimming ratio will be 30% instead of 32%.

Ton calculation by the iW7032 is pipelined with dimming register programming. When the first channel dimming register is updated, the IC initiates the calculation for this channel’s Ton immediately. This allows the dimming register programming and Ton calculation to be overlapped in time to save both SPI and the calculation bandwidth.

For a single IC system solution, the software is required to program 33-set real time registers for the N+1 frame at tsd0 delay of N frame. The IC manages all 32-channel Ton calculations, pre-calculated Ton buffering, and Ton updating at the right timing.

For multiple IC system solutions, the software is required to program 33-set real time registers sequentially for all ICs for the N+1 frame at tsd0 delay of N frame. Each IC starts the Ton calculation when the first dimming register belonging to this IC is updated.

15.0 PWM Modulation Timing

The iW7032 offers three modes of PWM modulation. They are controlled by the PWM_mdl_cfg bits within the SPI register map, and work as described in the following timing diagram. The example given is for a 25% dimming duty cycle with a delay set at 30 percent of a vsync cycle.

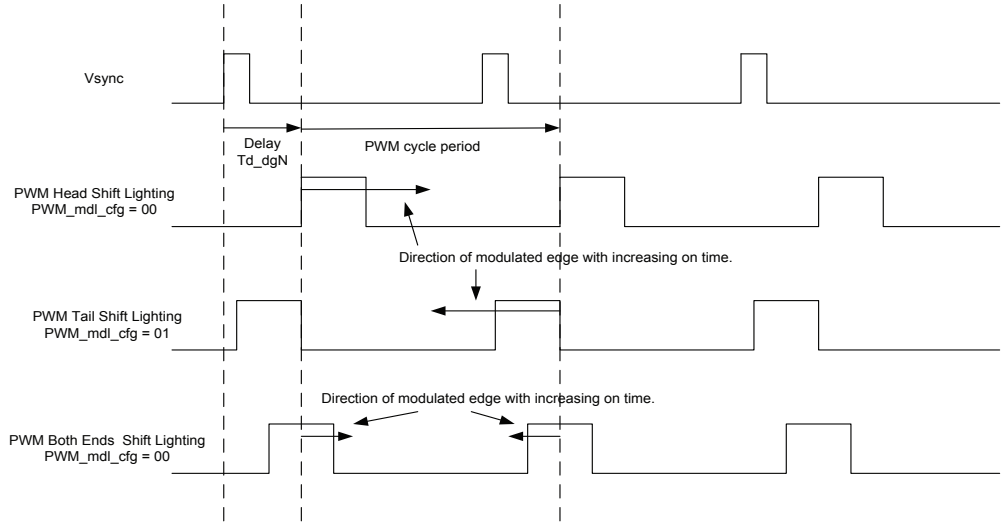
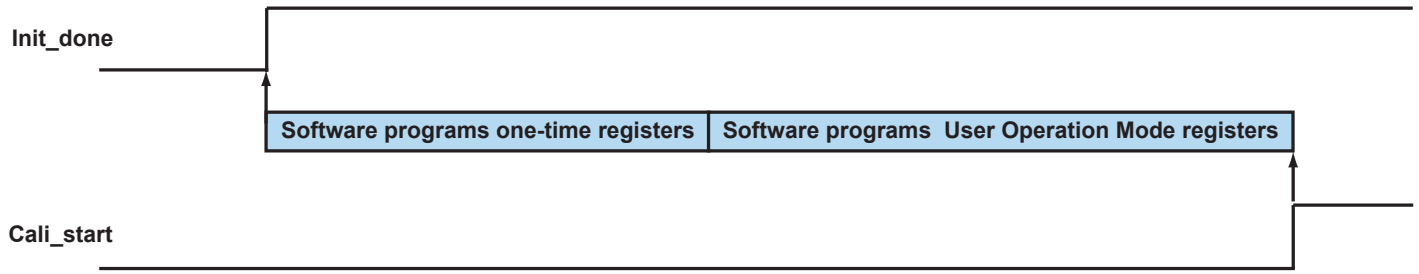


Figure 15.1. PWM Modulation Timing Diagram

16.0 Software Initialization Timing



After “init_done” is asserted, software needs to program the control registers in order to initiate the calibration.

Figure 16.1. Software Initialization Timing

17.0 User Operation Mode Register Update Timing

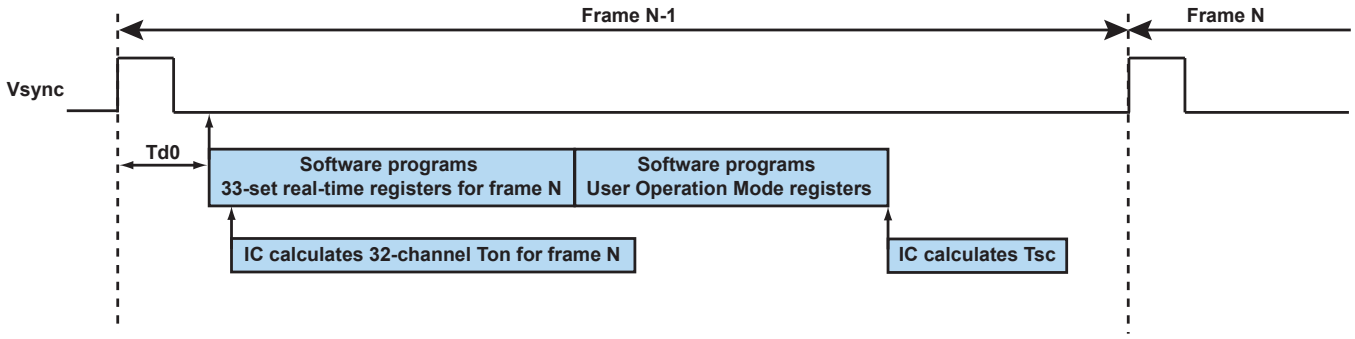


Figure 17.1. User Operation Mode Register Update Timing

18.0 Continuous Total Power Dissipation

The input resistance into LEDx (for x = 1 to 32) of the iW7032 is around 5 Ω for each of 32 LED pins. Suppose the maximum LED current is 120 mA. Then the maximum continuous total power dissipation, under the condition that all of the LED strings have perfectly matched forward voltages, is:

$$32 \times 120mA \times 120mA \times 5\Omega = 2.3\ W \qquad (eq\ 18.1)$$

However, in reality, LEDs are manufactured with varying forward voltages. Suppose the varying range of the forward voltage of each LED is around 0.1 V. If each LED channel includes 10 LEDs in series, the variance of the total forward voltage of the 32 LED channels is around 0.1V•0.5•10 (LEDs) = 0.5 V on the average. Since all of the 32 LED strings need to flow with the same currents, this disparity in forward voltages will contribute to the additional thermal dissipation at the 32 LED pins.

Therefore, the average continuous total power dissipation is around:

$$2.3W + 31 \times 120mA \times 0.5V = 2.3W + 1.86W = 4.16W \qquad (eq\ 18.2)$$

If the thermal resistance of the QFP64 package for iW7032 is 15 °C/W and T_A = 60°C:

$$T_J = 60 + 15 \bullet 4.16 = 122.4°C \qquad (eq\ 18.3)$$

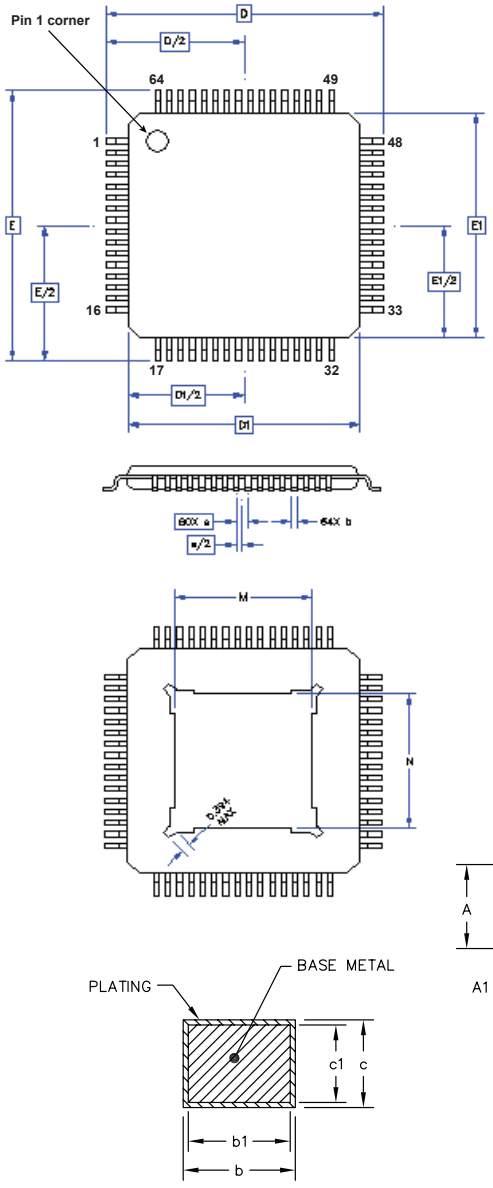
That is, the temperature increase is around 62 °C.

Note: A heat sink is needed to achieve the value of θ_{JA} = 15 °C/W

19.0 Physical Dimensions

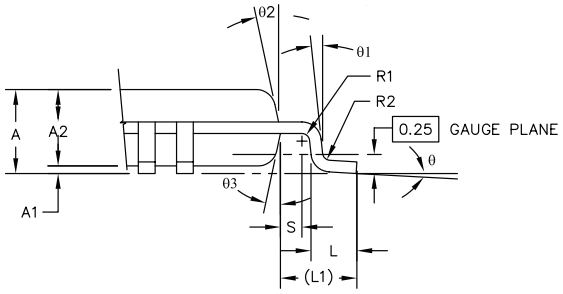
10 x 10mm TQFP-EP 64 Lead Package Package

IPC/JEDEC J-STD-20D Moisture Sensitivity Level 3



	MIN	Typ	MAX
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09		0.20
c1	0.09		0.16
D		12 BSC	
D1		10 BSC	
e		0.5 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.6	0.75
L1		1.00 Ref.	
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
M	5.85		6.05
N'	5.85		6.05

Unit in mm



Soldering Temperature Resistance:

[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 3

[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270°C

20.0 Ordering Information

Part Number	Description	Minimum Order Requirement
iW7032-00-TQ1	TQFP-64-EP	1,600 pcs

Trademark Information

Contact Information

Web: http://www.iwatt.com

E-mail: info@iwatt.com

Phone: +1 (408) 374-4200

Fax: +1 (408) 341-0455

iWatt Inc.
675 Campbell Technology Parkway, Suite 150
Campbell, CA 95008

Disclaimer

iWatt reserves the right to make changes to its products and to discontinue products without notice. The applications information, schematic diagrams, and other reference information included herein is provided as a design aid only and are therefore provided as-is. iWatt makes no warranties with respect to this information and disclaims any implied warranties of merchantability or non-infringement of third-party intellectual property rights.

iWatt cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in an iWatt product. No circuit patent licenses are implied.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

iWATT SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR OTHER CRITICAL APPLICATIONS.

Inclusion of iWatt products in critical applications is understood to be fully at the risk of the customer. Questions concerning potential risk applications should be directed to iWatt Inc.

iWatt semiconductors are typically used in power supplies in which high voltages are present during operation. High-voltage safety precautions should be observed in design and operation to minimize the chance of injury.