IXYS Power MOSFET Datasheet Parameters Definition

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IXAN0065

IXYS provides datasheets with parameters that are essential and useful for selecting the appropriate device as well as for predetecting its performance in an application. The graphs included in the datasheet represent typical performance characteristic and can be used to extrapolate from one set of operating conditions to another. Power MOSFET generally contains a body diode, which provides "free wheeling" operation in the inductive load switching. Figure 1 shows the equivalent circuit for an N-Channel and a P-Channel Power MOSFET.

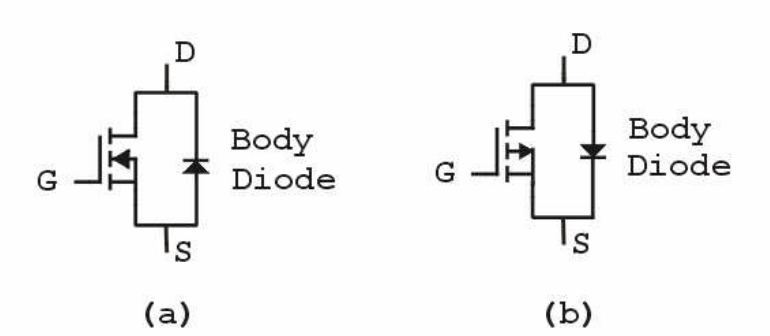

Figure 1: (a) an N-Channel (b) a P-Channel Enhancement-Mode Power MOSFET[1]

Essential Ratings and Characteristics

1. Maximum Ratings

The ratings are limiting values for a device and valid for the whole range of operating conditions[3].

1.1 Temperature

1.1.1 **Junction Temperature T_J and T_{JM}**

The junction temperature (T_J) range is -55 ~ 150°C in most cases and it is the device's permissible temperature range within which the device may be operated continuously. The maximum junction temperature (T_{JM}) is 150°C unless otherwise specified (in some cases 175°C). Junction temperature varies electrical parameters of Power MOSFET, for example, at very low temperature (< -55°C), the device can loss its functionality and at very high temperature, the device's threshold voltage becomes very low and leakage current becomes very high. It also can cause thermal run away within the device at very high value.

1.1.2 **Storage Temperature T_{Stg}**

It is the range of temperature for storage or transportation of the dev ice and it must be between -55 ~ 150°C.

1.1.3 **Lead Temperature T_L**

It is the maximum lead temperature during soldering and it must not exceed 300 ℃ for 10 seconds at 1/8" from the case.

1.2 Power Dissipation P_D

The power dissipation is the maximum calculated power that the device can dissipate and is function of both on the maximum junction temperature and the thermal resistance at a case temperature T_C 25°C.

$$P_D = [T_{JM} - T_C]/R_{thJC} \quad (1)$$

1.3 Current

1.3.1 **Continuous On-state Drain Current I_{D25}**

This is the maximum current rating for the device at a case temperature (T_C) 25°C. It is calculated based on maximum power dissipation, maximum on-resistance and temperature dependence of on-resistance. It can be limited by the current handling capacity of leads.

1.3.2 **Maximum Lead Current I_{DRMS}**

This is the maximum current rating of the device's lead at a case temperature 25°C.

1.3.3 **Maximum Peak On-state Drain Current I_{DM}**

It is the peak current the device can flow above I_{D25} specification under the maximum junction temperature. It varies with current pulse widths, duty cycle and heat dissipation conditions.

1.3.4 **Diode Forward Current I_S**

It's the maximum DC current the diode can flow in the forward direction at specified case temperature.

1.3.5 **Maximum Diode Forward Current I_{SM}**

It's the peak current the diode can flow above I_S specification under the maximum junction temperature.

1.4 Voltage

1.4.1 **Maximum Drain-Source Voltage V_{DSS}**

This is defined as the maximum drain-source voltage without causing avalanche breakdown with gate-source short-circuited ($V_{GS} = 0$) and the device is at 25°C. The avalanche breakdown voltage is temperature dependent and could be less than the BV_{DSS}, rating.

1.4.2 Maximum Gate-Source Voltage $\pm V_{GS}$

This is the maximum voltage that can be introduced between gate and source. It depends on the thickness and characteristics of the gate oxide layer. The actual gate oxide withstand voltage is typically much higher than this but varies due to manufacturing processes, so staying within this rating ensures application reliability.

1.4.3 **Maximum Rate of Rise of Off-state Voltage (dv/dt)**

This is defined as the maximum permissible rate of rise of off-state voltage across the device.

1.5 Avalanche Energy (for avalanche devices)[3]

1.5.1 **Avalanche Drain Current, Repetitive I_{AR}**

For power MOSFETs, the propensity for current crowding in the die area during avalanche mandates a limit in avalanche current. It represents the avalanche energy specification for the device and the true capability of a device.

1.5.2 **Maximum repetitive Avalanche Energy, Single Pulse E_{AR}**
The maximum permissible reverse-voltage breakdown energy in continuous operation while observing the maximum permissible chip temperature. The heat dissipation limits the avalanche energy.

1.5.3 **Maximum non-repetitive Avalanche Energy, E_{AS}**
The maximum permissible reverse-voltage breakdown energy in continuous operation while observing the maximum permissible chip temperature. The heat dissipation limits the avalanche energy.

1.6 Mechanical Data

1.6.1 **Mechanical Drawings**
This provides the mechanical size of the device with package information.

1.6.2 **Weight**
This provides the weight information of the device with package.

1.6.3 **Mounting Torque M_d**
This provides the maximum permissible torque that can be applied on the device for mounting[3].

2. Characteristics

According to IEC 60747-8:2004, the characteristics of Power MOSFETs are given at $25^{o}C$ and at one specified higher operating temperature[3].

2.1 Current

2.1.1 **Gate-Source Leakage Current I_{GSS}**
It is the maximum gate-source leakage current with the drain and the source shorted and with the introduction of rated gate-source voltage.

2.1.2 **Zero Gate Voltage Drain Current I_{DSS}**
It is the maximum drain-source leakage current with the gate and the source shorted and with the introduction of rated drain-source voltage.

2.2 Voltage

2.2.1 **Break Down Voltage BV_{DSS}**
The breakdown voltage BV_{DSS} is the minimum blocking voltage between the drain and the source at given drain current and when the gate is shorted to the source. The break down voltage has a positive temperature coefficient.

2.2.2 **Gate Threshold Voltage $V_{GS\ (th)}$**
It is the gate-source voltage at which the drain current starts to flow and the device is considered at ON-State. It has negative temperature coefficient.

2.2.3 **Gate-Source on-state voltage V_{GSM}**

This is a gate-source maximum voltage in the on-state.

2.3 On-state Resistance $R_{DS\ (on)}$

The specific on-resistance for a power MOSFET is defined by

$$R_{DS\ (on)} = R_{SOURCE} + R_{CH} + R_A + R_D + R_J + R_{sub} + R_{wcml,} \quad (2)$$

Where,
R_{SOURCE} = Source diffusion resistance
R_{CH} = Channel resistance
R_A = Accumulation resistance
R_J = JFET component resistance
R_D = Drift region resistance
R_{sub} = Substrate resistance
R_{wcml} = Bond wire resistance

2.4 Transconductance g_{fs}

It is defined as the change in drain current divided by the change in gate voltage for a constant drain voltage. A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response.

2.5 Capacitances and Gate Charges[3]

2.5.1 **Input Capacitance C_{iss}**

The input capacitance is measured between the gate and source terminals with the drain shorted to the source terminal. The C_{iss} is made up of the gate-to-drain capacitance C_{DG} in parallel with the gate-to-source capacitance $C_{GS.}$

$$C_{iss} = C_{GS} + C_{DG} \quad (3)$$

2.5.2 **Reverse Transfer Capacitance C_{rss}**

The reverse transfer capacitance is measured between the drain and gate terminals with the source connected to ground. The reverse transfer capacitance is the same as the gate-to-drain capacitance $C_{DG.}$

$$C_{rss} = C_{DG} \quad (4)$$

2.5.3 **Output Capacitance C_{oss}**

The output capacitance is measured between the drain and source with the gate shorted to the source terminal. The C_{oss} is equal to the drain-to-source capacitance C_{DS}, in parallel with the gate to drain capacitance $C_{DG.}$

$$C_{oss} = C_{DS} + C_{DG} \quad (5)$$

2.5.4 **Gate Charges**

It's the total gate charge that's required to raise the gate-source voltage to 15V in most cases to fully turn-on the device. It's measured at a specified drain current,

drain-source voltage and gate-source voltage. The gate charge reflects the charge stored on the inter-terminal capacitances described earlier and is used in designing the gate drive circuit.

2.6 Switching times ($t_{d\ (on)}$, t_r, $t_{d\ (off)}$, t_f)[3]

2.6.1 **Turn-on Delay Time $t_{d\ (on)}$**

The turn-on delay time is defined as the time interval when the gate-source voltage (V_{GS}) has reached 10 % of its end value (V_{GG}), to the time when the drain-source voltage (V_{DS}) has dropped to 90 % of its initial value (V_{DD}).

2.6.2 **Rise Time t_r**

Following the turn-on delay time, the rise-time follows; it is the interval between the drain-source voltages from 90% to 10% of its initial value. The drain current starts to rise and the major part of turn-on losses is generated during this period.

2.6.3 **Turn-off Delay Time $t_{d\ (off)}$**

The turn-off delay time is defined as the time interval between the moment when the gate-emitter voltage (V_{GE}) has declined to 90 % of its initial value (V_{GG}) and the drain-source voltage has risen to 10 % of the supply voltage V_{DD}.

2.6.4 **Fall Time t_f**

Following the turn-off delay time, the fall-time follows; it is the interval between the drain-source voltage rises from 10% to 90% of its end value. During this period, the drain current starts to fall and the major part of turn-off losses is generated during this time.

2.7 Turn-on energy (per pulse) E_{on} where appropriate[3]

2.8 Turn-off energy (per pulse) E_{off} where appropriate[3]

2.9 Thermal Characteristic[2]

Power MOSFETs operate at elevated junction temperature and it is important to observe their thermal limitations in order to achieve acceptable performance and reliability.

2.9.1 **Thermal Resistance Junction to Case R_{thJC}**

It's the thermal resistance from the junction of the die to the outside of the device case. It describes the passage of heat between the semiconductor chip and case. IXYS specifies maximum static R_{thJC}.

2.9.2 **Thermal Resistance Case to Heatsink R_{thCK}**

The thermal resistance case to sink characterizes the static heat dissipation of a MOSFET and depends on module size, heatsink, case surfaces, thickness parameters of thermal layers between module and heatsink.

3.0 Intrinsic Diode Characteristics[2]

3.1 **Intrinsic Diode Forward Voltage V_{SD}**

The forward voltage is the maximum forward drop of the intrinsic diode at a specified value of source current.

3.2 **Reverse Recovery Time t_{rr}**

Reverse recovery time is the time interval starting as current flow reverses through the diode until it goes zero. IXYS shows typical t_{rr} at given test conditions.

3.3 **Reverse Recovery Charge Q_{rr}**

Reverse recovery charge is the integral of the reverse recovery current that occurs during current commutation.

3.4 **Peak Reverse Current I_{RM}**

Peak Reverse recovery charge is the integral of the reverse recovery current that occurs during current commutation.

Essential Curves Definitions

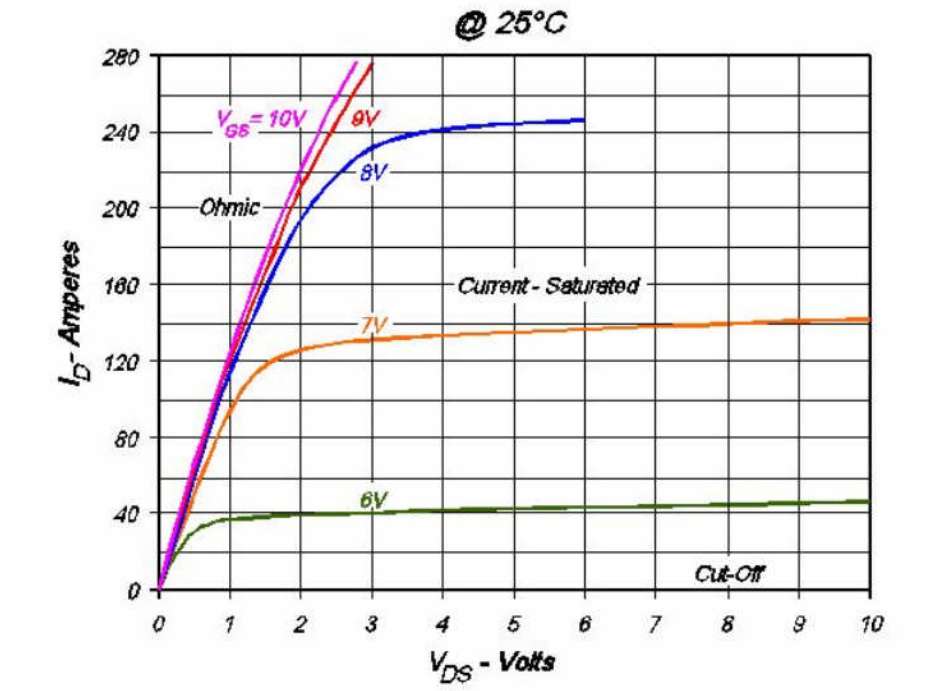

Figure 2: Output Characteristics of a Power MOSFET [IXTH/IXTQ130N10T][5]

1. Output Characteristics:

Figure 2 shows a typical output characteristic of an N-Channel Power MOSFET in which the different modes of operation are delineated. In the Cut-off region, the gate-source voltage (V_{GS}) is less than the gate-threshold voltage ($V_{GS(th)}$) and the device is an open-circuit or off. In the Ohmic region, the device acts as a resistor with almost a constant on-resistance $R_{DS\,(on)}$ and is equal to V_{DS} /$I_{DS.}$ In the linear-mode of operation, the device operates in the 'Current-Saturated' region where the drain current (I_{ds}) is a function of the gate-source voltage (V_{gs}) and defined by:

$$I_{DS} = K \bullet (V_{GS} - V_{GS(th)})^2 = g_{fs} \bullet (V_{GS} - V_{GS(th)}) \qquad (6)$$

Where K is a parameter depending on the temperature and device geometry and g_{fs} is the current gain or transconductance. When the drain voltage (V_{DS}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. The channel inversion layer charge decreases with increasing V_{DS} and ultimately, it becomes zero when the drain voltage equals to $(V_{GS} - V_{GS(th)})$. This point is called the "channel pinch-off point" where the drain current becomes saturated[4].

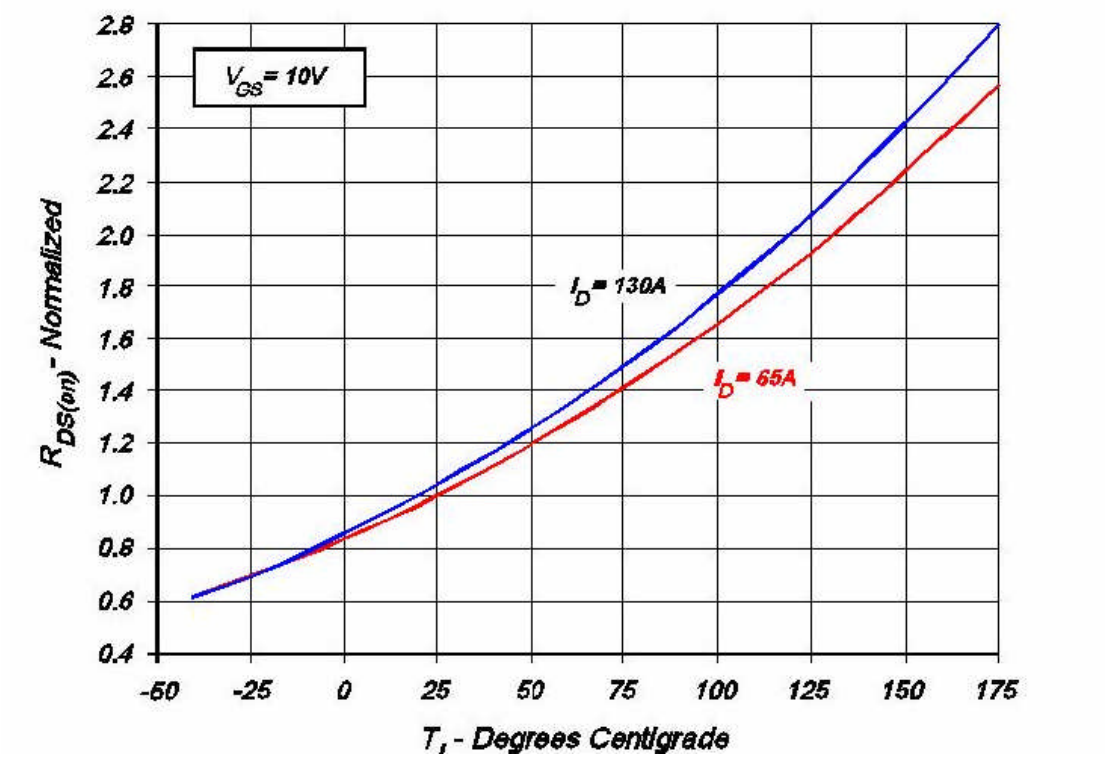

Figure 3: Normalized $R_{DS(on)}$ vs. Junction Temperature [IXTH/IXTQ130N10T][5]

2. On-Resistance $R_{DS(on)}$ vs. Junction Temperature:

Temperature has a strong effect on $R_{DS(on)}$, on-resistance, which is an important parameter in power MOSFET and a measure of the current handling capability of the device. An important merit is an increase in the on-resistance with increasing temperature as shown in Figure 3, which portrays a positive temperature coefficient. The positive temperature coefficient of $R_{DS\ (on)}$ is a nice feature when paralleling Power MOSFETs because it ensures thermal stability.

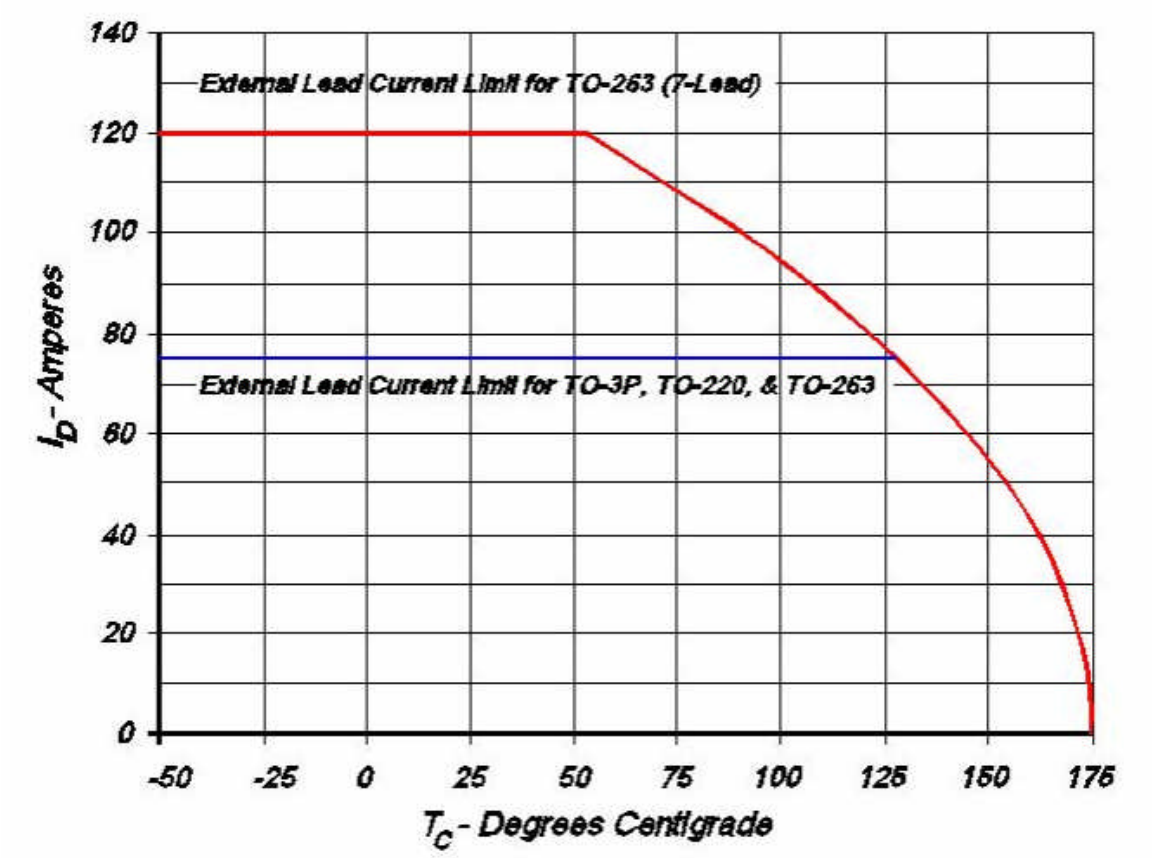

Figure 4: Drain Current vs. Case Temperature [IXTH/IXTQ130N10T][5]

3. Drain Current vs. Case Temperature:

The drain current I_D is a rating of the maximum continuous DC current with the die at its maximum rated junction temperature (T_{JM}) and the case at 25°C. It is related with the junction-to-case thermal resistance R_{thJC} and case temperature T_C as follows:

$$P_D = \frac{T_{JM} - T_C}{R_{thJC}} = I_D^2 \bullet R_{DS(on)atT_{JM}} \qquad (7)$$

Solving for I_D as

$$I_D = \sqrt{\frac{T_{JM} - T_C}{R_{thJC} \bullet R_{DS(on)atT_{JM}}}} \qquad (8)$$

Figure 4 is just the solution of equation (8) over a range of case temperature. Note that in some cases, the package leads limit the continuous current (the switched current can be higher). 75A is for TO-3P, TO-220 and TO-263 and 120A is for 7-leaded TO-263.

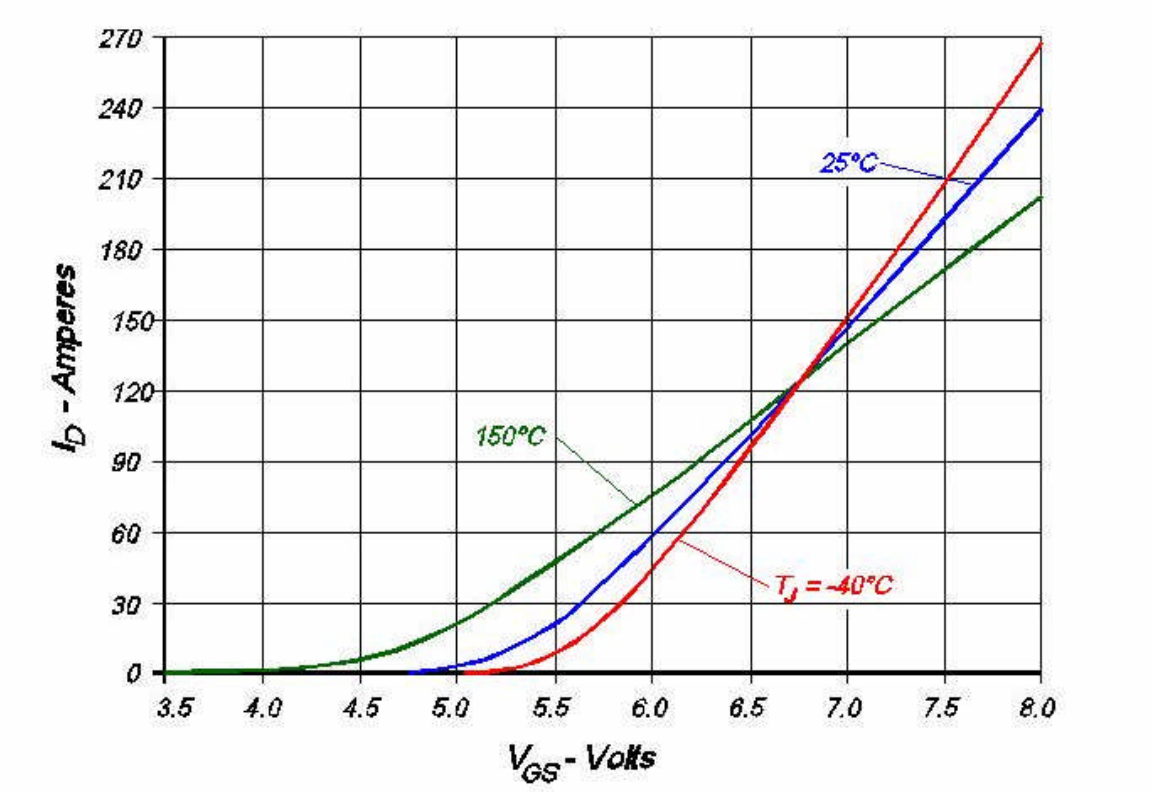

Figure 5: Transfer Characteristics (Input Admittance) [IXTH/IXTQ130N10T][5]

4. Transfer Characteristics (Input Admittance):

Figure 5 shows a typical transfer characteristic, which is a plot of drain current as a function of gate voltage at three different temperature ranges -40, 25 and 150 ^{o}C. The intercepts of these lines at I_D =0 provides the threshold voltages for respective temperature. It can be concluded that the transfer characteristic depends on both temperature and drain current and the threshold voltage decreases with increasing temperature. It can be further concluded that at below 120A, which is the cross-over point, the gate-source voltage has negative temperature coefficient means less gate-source voltage at higher temperature for a given drain current. At above 120A, the temperature coefficient for gate-source voltage is positive.

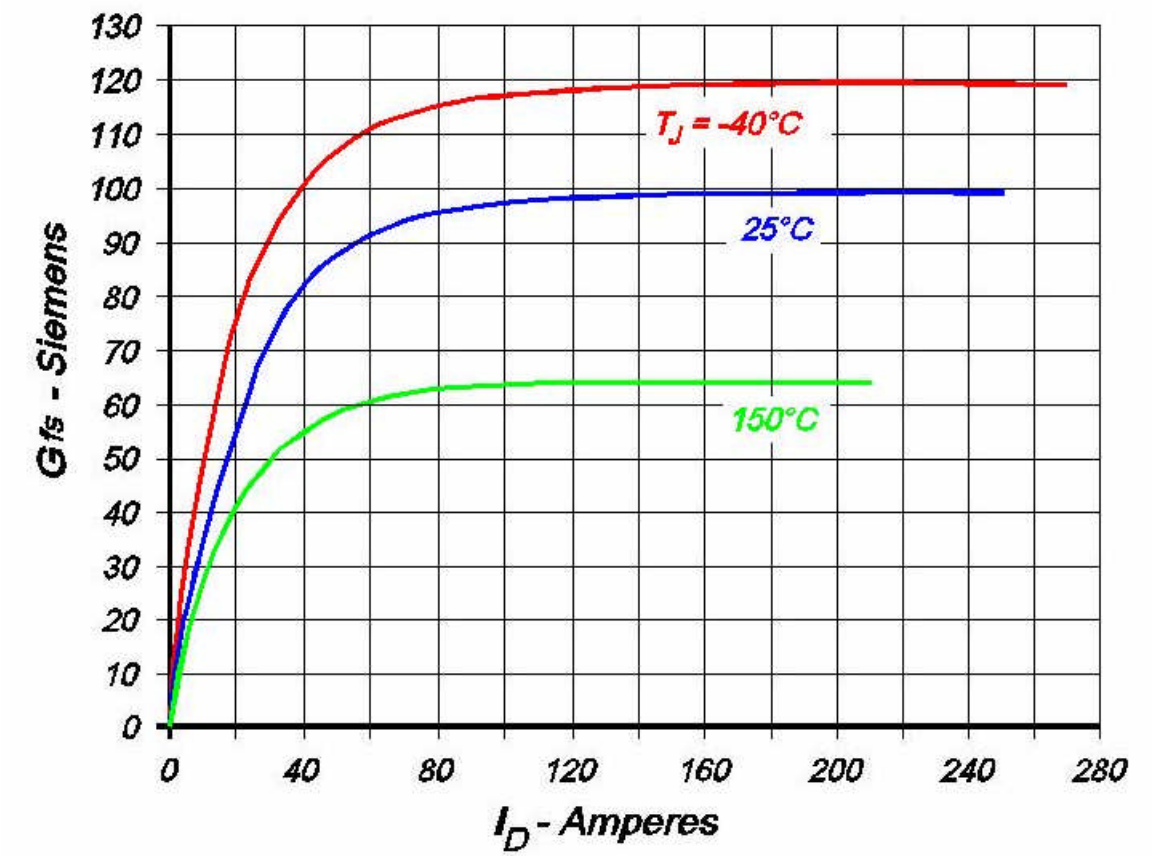

Figure 6: Current Gain (transconductance) vs. drain current [IXTH/IXTQ130N10T][5]

5. Current Gain or Transconductance:

It's defined as the change in drain current divided by the change in gate voltage for a constant drain voltage:

$$g_{fs} = \frac{dI_D}{dV_{GS}}\Big|V_{DS=constant} \qquad (9)$$

A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. A typical variation of transconductance as a function of drain current is shown in Figure 6. The reduction in the mobility with increasing temperature adversely affects the transconductance.

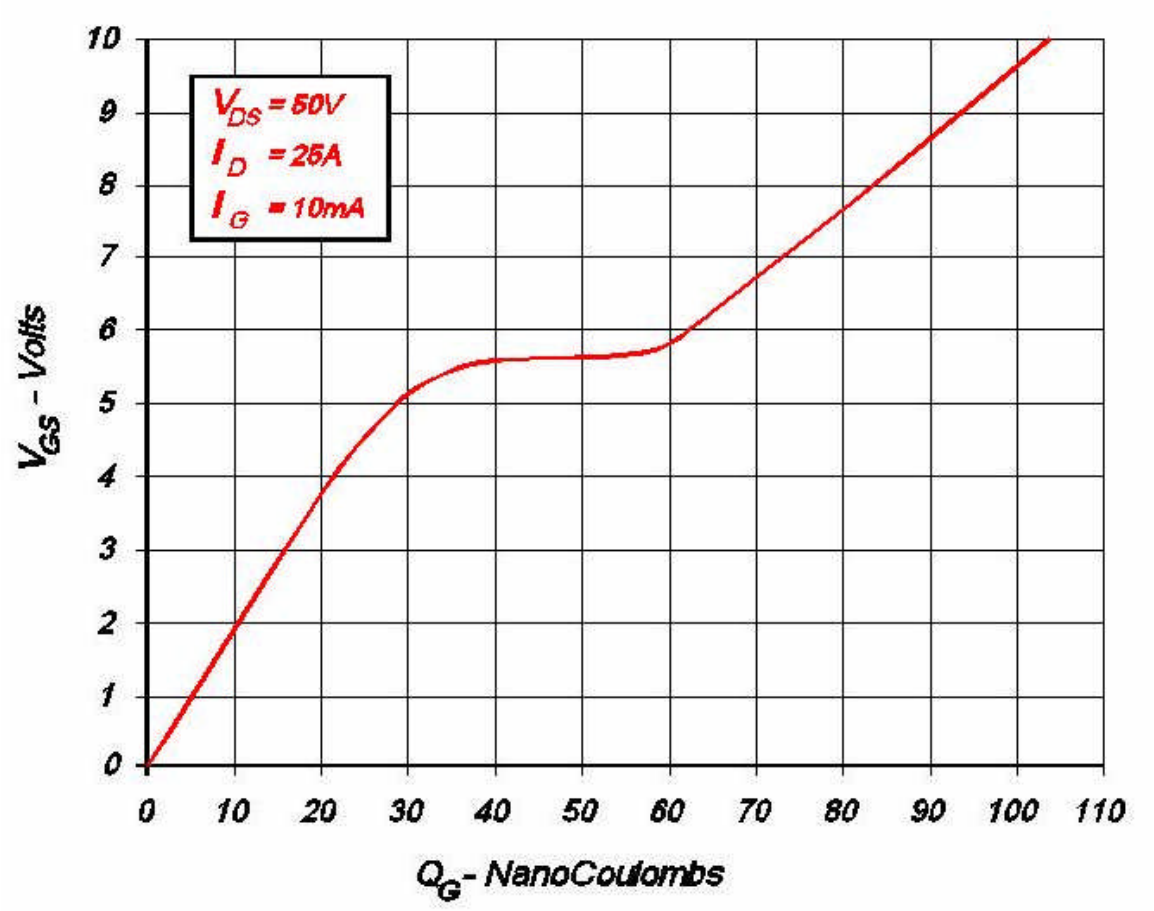

Figure 7: Gate Charge [IXTH/IXTQ130N10T][5]

6. Gate Charge:

It's the total gate charge required to raise the gate-source voltage to 15V, which is necessary in most cases to fully turn-on the device. All values are measured at a specified drain current, drain-source voltage and gate current. A typical gate charge waveform for a power MOSFET is shown in Figure 7. The gate charge reflects the charge stored on the inter-terminal capacitances described earlier and is used in designing the gate drive circuit.

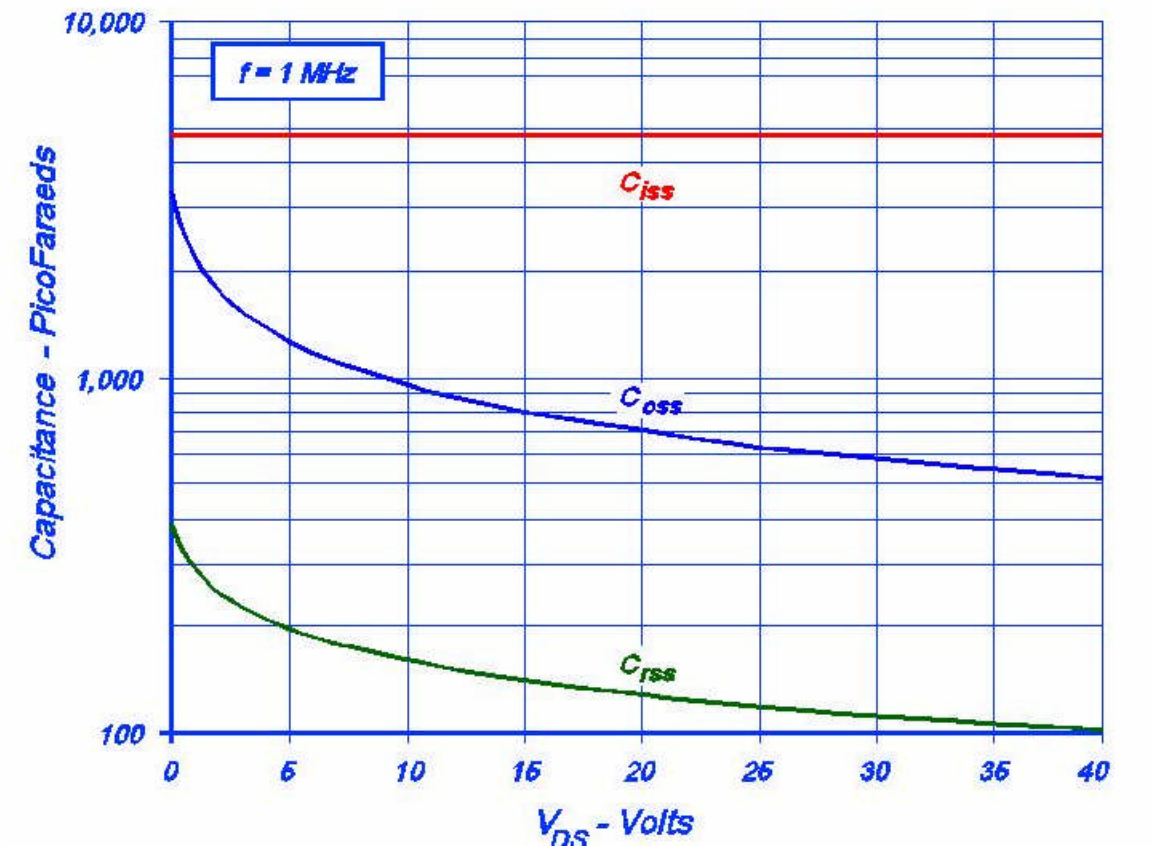

Figure 8: Capacitance [IXTH/IXTQ130N10T][5]

7. Capacitance:

Figure 8 shows parasitic capacitances characteristics as a function of drain-source voltage. Its components include input capacitance (Ciss), which consists of C_{GS} in parallel with C_{DG}, output capacitance (Coss), which consists of C_{DG} in parallel with C_{DS} and reverse transfer capacitance (Crss), which is the drain-source capacitance.

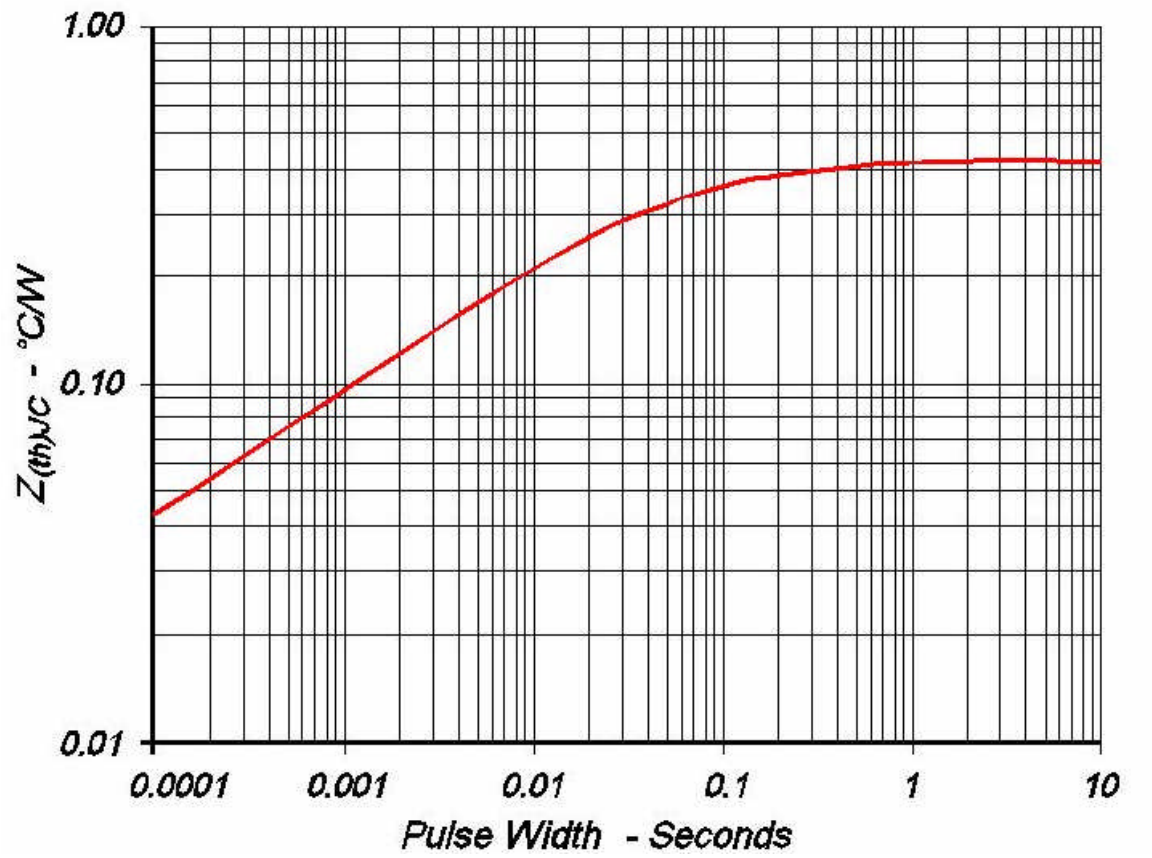

Figure 9: Transient Thermal Impedance [IXTH/IXTQ130N10T][5]

8. Transient Thermal Impedance:

Power MOSFET has junction temperature (T_J) limitation. It should be operated below the maximum junction temperature (T_{JM}) specified in the datasheet to ensure reliability. The heat generated within the silicon chip is typically dissipated by means of a heat sink into the ambient surroundings. The junction temperature rise above the ambient surrounding (T_A) is directly proportional to this heat flow and the junction-to-ambient thermal resistance (R_{thJA}). The steady-state junction temperature can be defined by:

$$T_J = P_D R_{(th)JA} + T_A \le T_{JM} \qquad (10)$$

Where, P_D = Maximum power dissipated in the junction. The total thermal resistance between junction and ambient is,

$$R_{(th)JA} = R_{(th)JC} + R_{(th)CS} + R_{(th)SA} \qquad (11)$$

The steady-state thermal resistance is not enough for finding peak junction temperatures for pulsed applications. When a power pulse applied to the device, the peak junction temperature varies depending on peak power and pulse width. The thermal resistance for junction-to-case at a given time is called transient thermal resistance and it is defined by:

$$Z_{(th)JC}(t) = r(t)R_{(th)JC} \qquad (12)$$

Where r(t) is a time dependent factor that defines the thermal capacity of the device. For short pulse, the r(t) value is small but for long pulse, it approaches 1 that means the transient thermal resistance approaches to steady-state thermal resistance. A typical transient thermal resistance curve is shown in Figure 9. It approaches the steady-state value at long pulse values. It can be used to estimate the peak temperature rise for square wave power pulses, which is typical in power supply design circuits

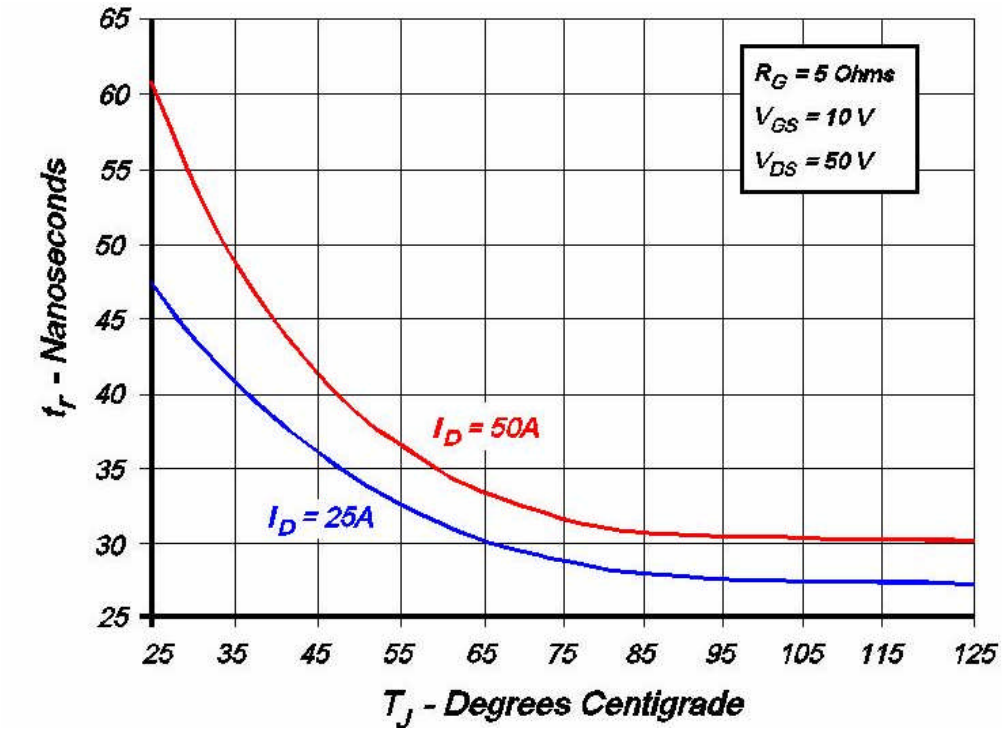

Figure 10: Resistive Turn-on Rise Times vs. Junction Temperature [IXTH/IXTQ130N10T][5]

9. Resistive Turn-on Rise Times vs. Junction Temperature

Figure 10 shows the resistive turn-on rise time decreases with increasing junction temperature. It also shows that rise time increases with increasing current.

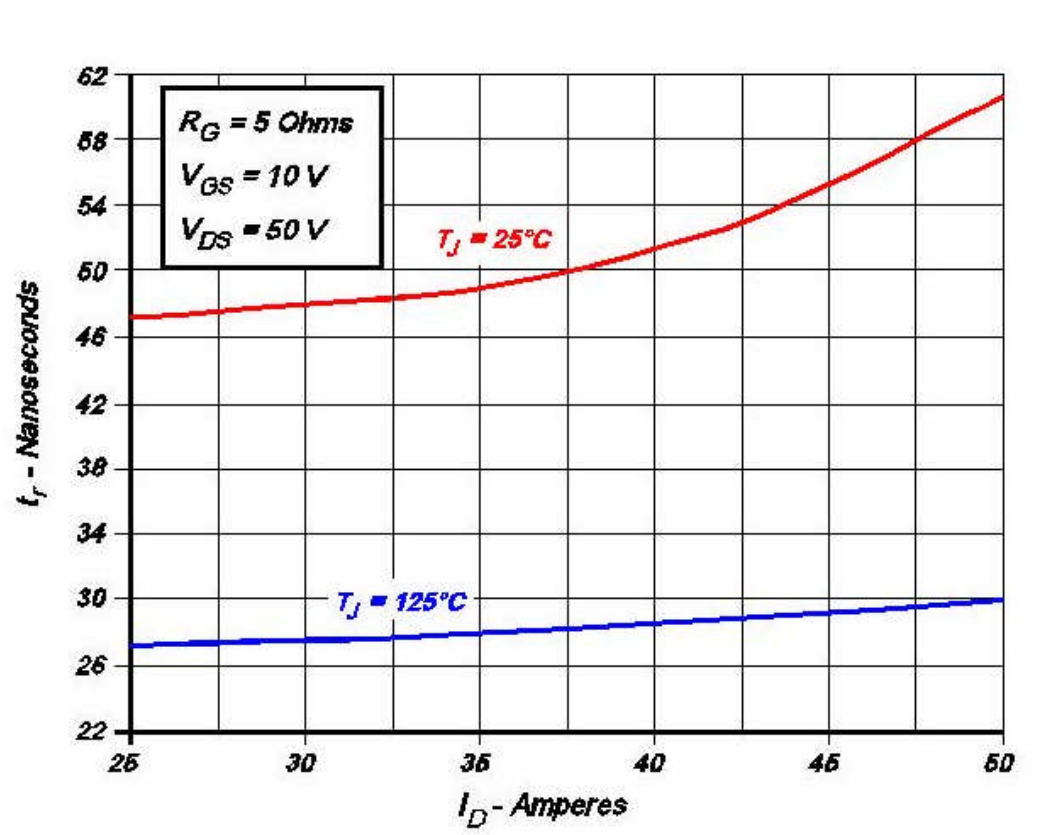

Figure 11: Resistive Turn-on Rise Times vs. Drain Current [IXTH/IXTQ130N10T][5]

10. Resistive Turn-on Rise Times vs. Drain Current

Figure 11 shows the resistive turn-on rise time increases with increasing junction temperature. It also shows that rise time increases with increasing temperature.

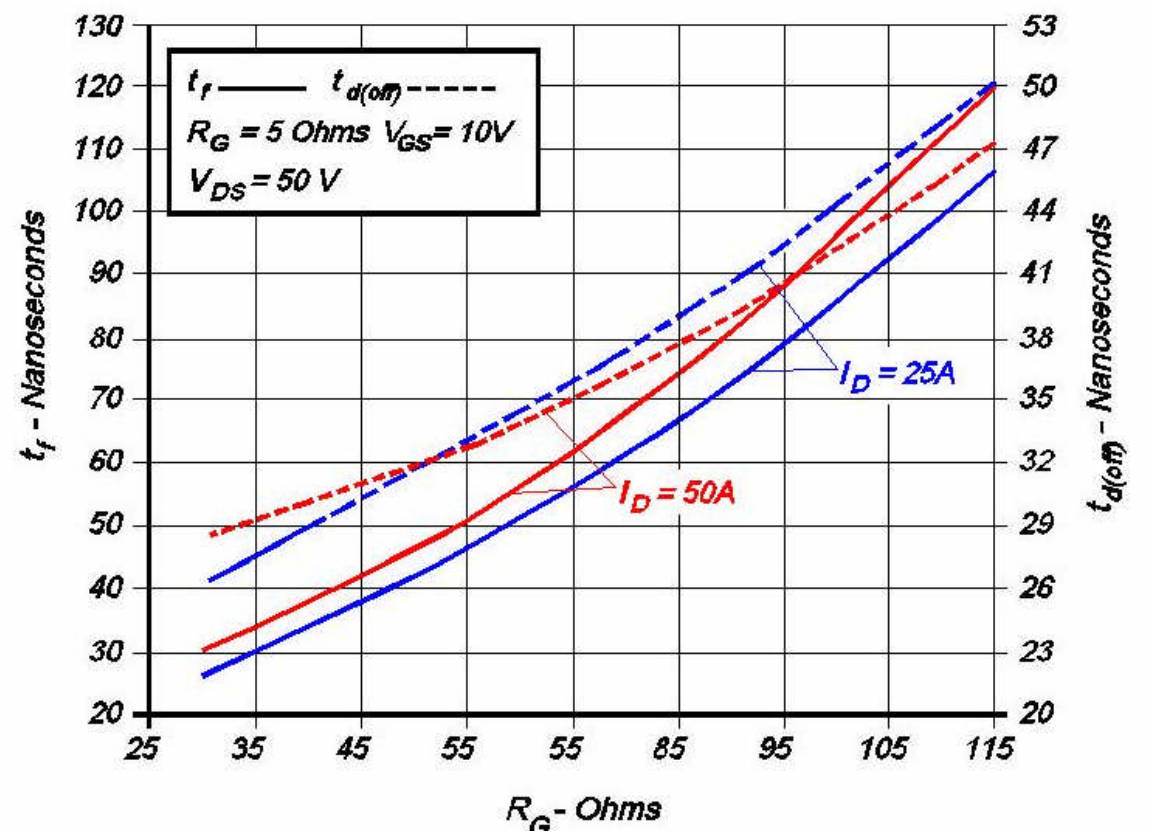

Figure 12: Resistive Turn-on Switching Times vs. Gate Resistance [IXTH/IXTQ130N10T][5]

11. Resistive Turn-on Switching Times vs. Gate Resistance:
Figure 12 shows the resistive turn-on switching time increases with increasing gate resistance. It also shows that rise time increases with increasing drain current.

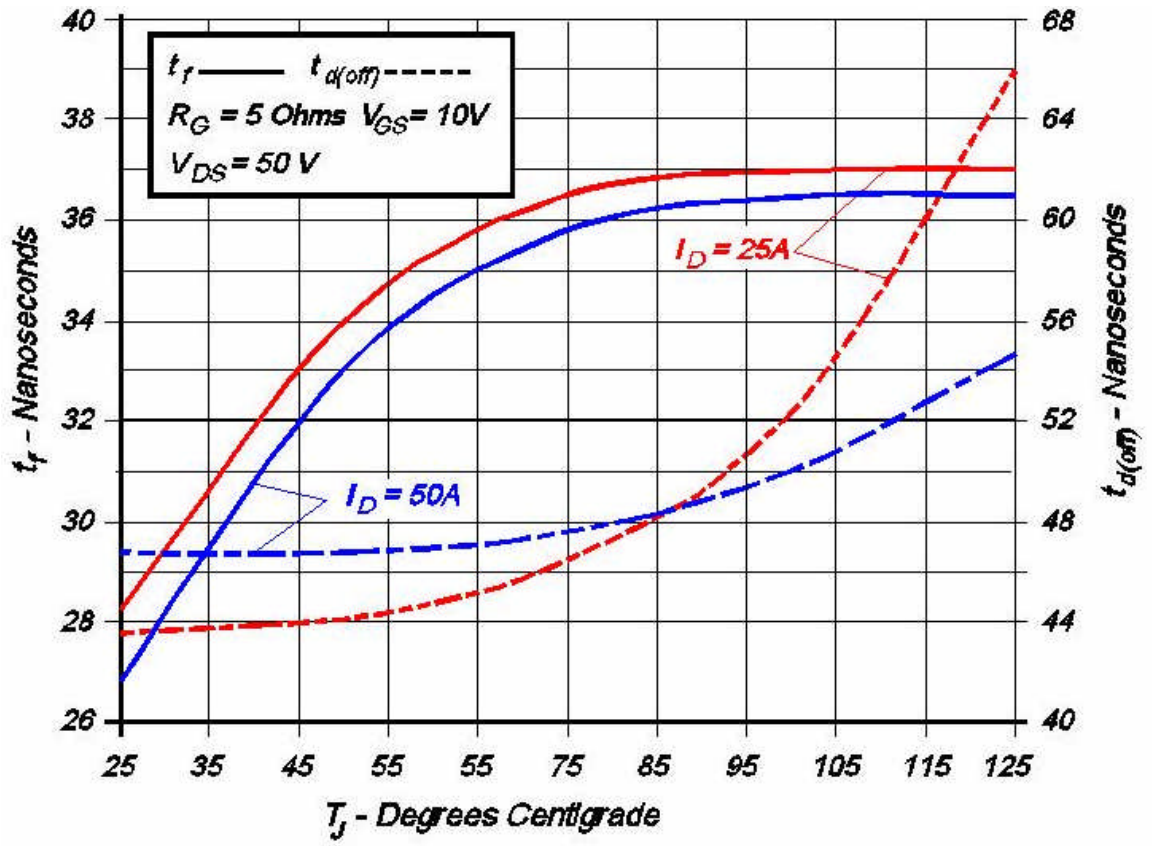

Figure 13: Resistive Turn-off Switching Times vs. Junction Temperature [IXTH/IXTQ130N10T][5]

12. Resistive Turn-off Switching Times vs. Gate Resistance:
Figure 13 shows the resistive turn-on switching time increases with increasing gate resistance. It also shows that rise time increases with increasing drain current.

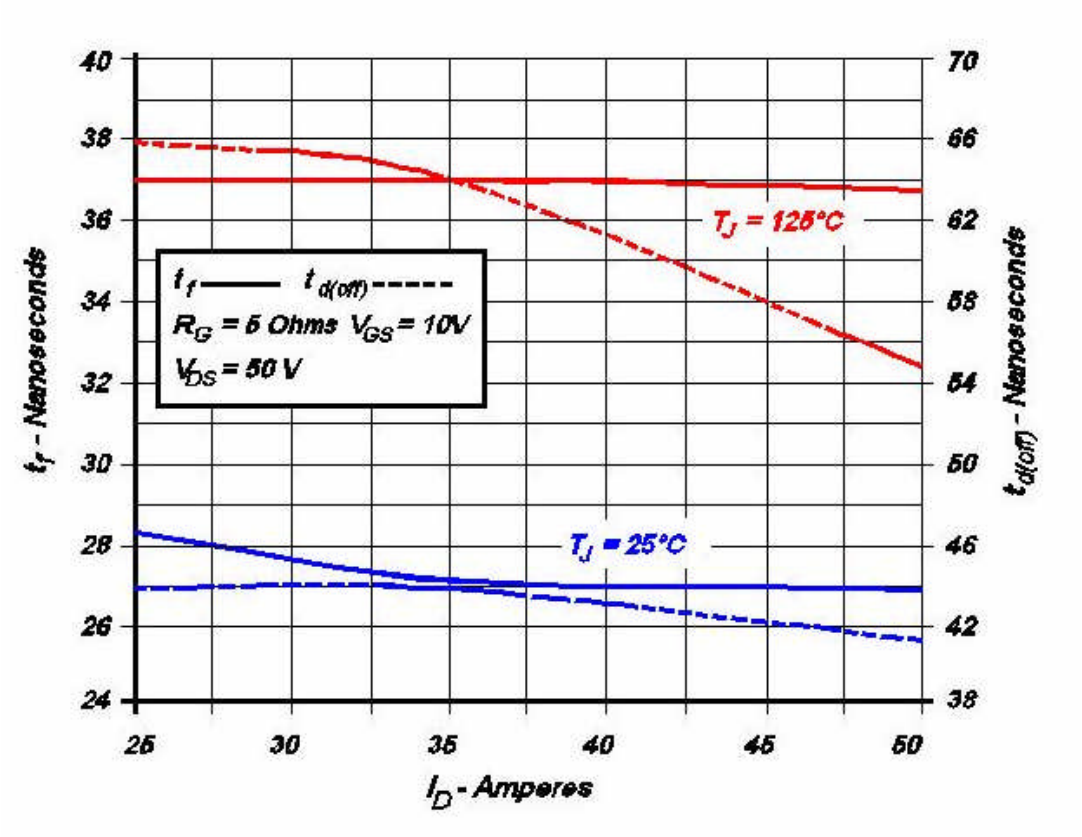

Figure 14: Resistive Turn-off Switching Times vs. Drain Current [IXTH/IXTQ130N10T][5]

13. Resistive Turn-off Switching Times vs. Drain Current:
Figure 14 shows the resistive turn-off switching time stays almost constant with increasing drain current. It also shows the fall time increases with increasing temperature.

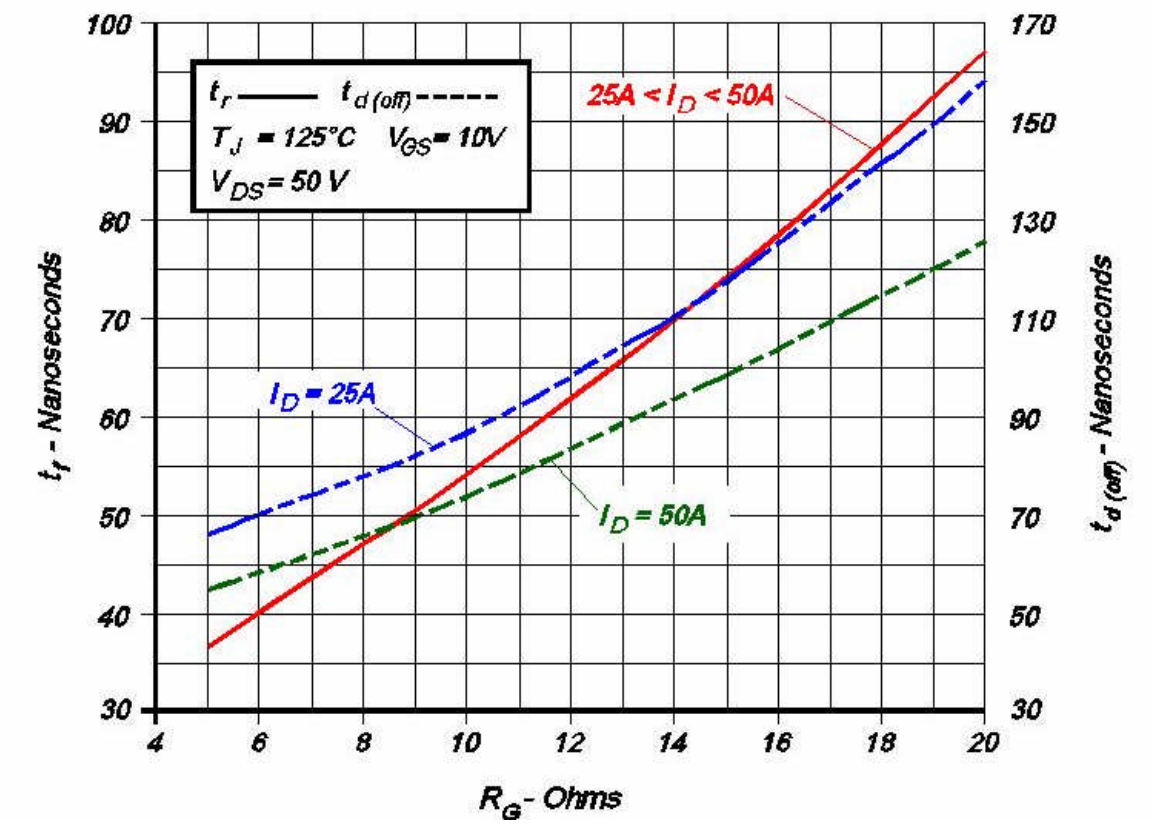

Figure 15: Resistive Turn-off Switching Times vs. Gate Resistance [IXTH/IXTQ130N10T][5]

14. Resistive Turn-off Switching Times vs. Gate Resistance:

Figure 15 shows the resistive turn-off switching time increases with increasing gate resistance. It also shows that the fall times decreases with increasing drain current.

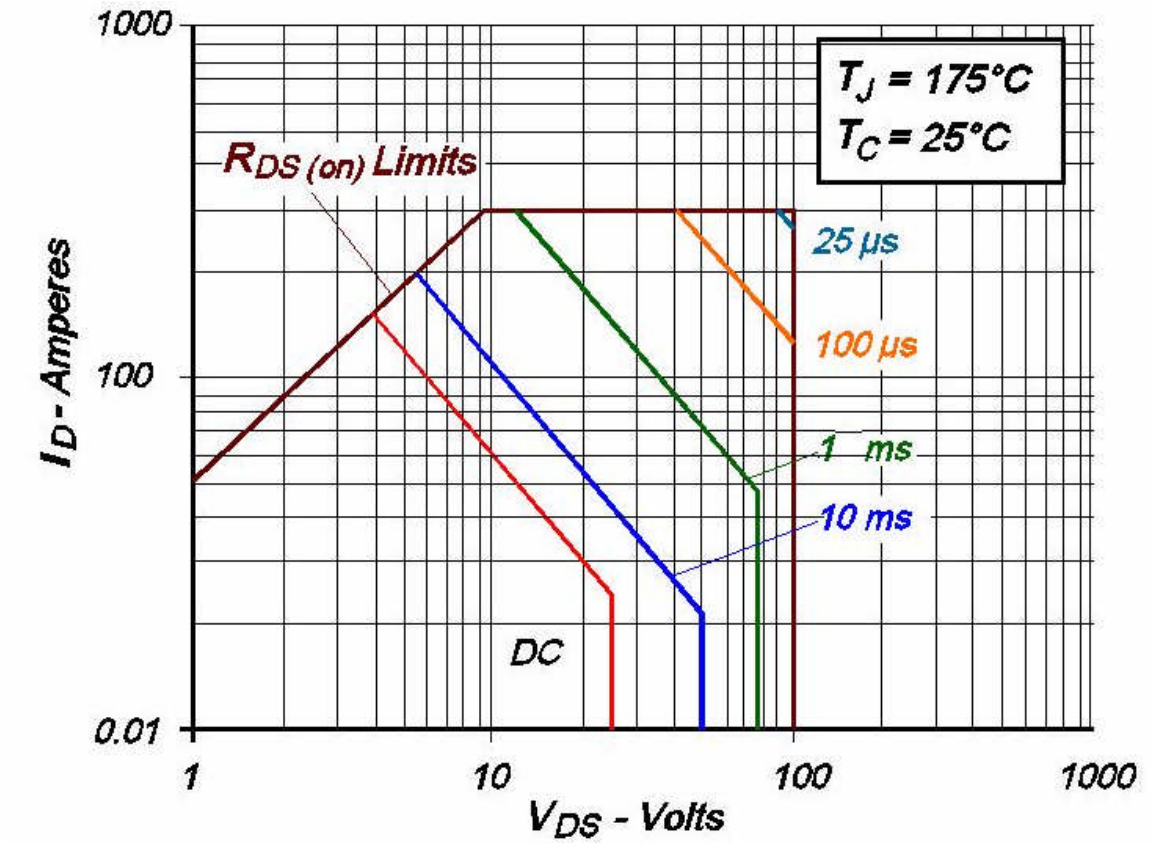

Figure 16: Forward-Biased Safe Operating Area (FBSOA) graph for an N-Channel Power MOSFET [IXFH/IXFT140N10P] [5]

15. Forward-Biased Safe Operating Area (FBSOA):

The FBSOA is a datasheet figure of merit that defines the maximum allowed operating points. Figure 16 shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bounded by the maximum drain-to-source voltage V_{DSS}, maximum conduction current I_{DM} and constant power dissipation lines for various pulse durations. In this figure, the set of the curves shows a DC line and four single pulse operating lines, 10ms, 1ms, 100 µs and 25 µs. The top of each line is truncated to limit the maximum drain current and is bounded by a positive slope line defined by the $R_{DS(on)}$ of the device. The right hand side of each line is terminated at the rated drain-to-source voltage limit (Vdss). Each line has a negative slope and is determined by the maximum allowed power dissipation of the device P_d:

$$P_d = [T_{JM} - T_C] / Z_{thJC} = V_{DS}\, I_D \qquad (13)$$

Where Z_{thJC} is the junction-to-case transient thermal impedance and $T_{J\,(max)}$ is the maximum allowed junction temperature of the MOSFET. These theoretical constant

power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFETs. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, the result of lateral heat flow. Secondly, material imperfections (die attach voids, thermal grease cavities, etc.) may cause local decrease of thermal conductivity, i.e. increase of local temperature. Thirdly, fluctuations in dopant concentrations and gate oxide thickness and fixed charge will cause fluctuations of local threshold voltage and the current gain (g_{fs}) of MOSFET cells, which will also affect local temperature of the die. Die temperature variations are mostly harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications were found to have limited capability to operate in the right-side bottom corner of the FBSOA graph.

Bibliography

[1] John G. Kassakian, Martin F. Schlecht, George C. Verghese, “Principles of Power Electronics” Addison-Wesley Publishing Company, ISBN: 0-201-09689-7

[2] “Power Semiconductors Application Notes, 2002” IXYS Corporation, 3540 Bassett Street, Santa Clara CA 95054.

[3] BS IEC 60747-8-4: Discrete Semiconductor Devices: Metal-oxide-semiconductor field effect transistors (MOSFETs) for power switching applications.

[4] B. Jayant Baliga, “Power Semiconductor Devices” PWS Publishing Company, ISBN: 0-534-94098-6, 1996.

[5] “Product Datasheet, IXTH/IXTQ130N10T”, IXYS Corporation, 3540 Bassett Street, Santa Clara, CA 95054.