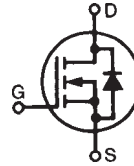


PolarHV™ HiPerFET Power MOSFET

IXFC 16N50P

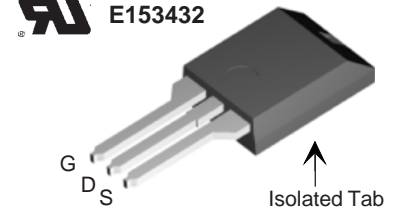
$$\begin{aligned} V_{DSS} &= 500 \text{ V} \\ I_{D25} &= 10 \text{ A} \\ R_{DS(on)} &= 450 \text{ m}\Omega \\ t_{rr} &= 200 \text{ ns} \end{aligned}$$

Electrically Isolated Tab,
N-Channel Enhancement Mode,
Fast Intrinsic Diode
Avalanche Rated



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 1 \text{ M}\Omega$	500	V
V_{GS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	10	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	50	A
I_{AR}	$T_C = 25^\circ\text{C}$	10	A
E_{AR}	$T_C = 25^\circ\text{C}$	25	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	750	mJ
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 10 \Omega$	10	V/ns
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s Plastic body for 10 s	300 250	$^\circ\text{C}$ $^\circ\text{C}$
V_{ISOL}	50/60 Hz, RMS, $t = 1$, leads-to-tab	2500	V~
F_C	Mounting Force	11..65/2.5..15	N/lb
Weight		2	g

ISOPLUS220™ (IXFC)
E153432



G = Gate D = Drain
S = Source TAB = Drain

Features

- Silicon chip on Direct-Copper-Bond substrate
 - High power dissipation
 - Isolated mounting surface
 - 2500V electrical isolation
- Low drain to tab capacitance (<30pF)
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
 - easy to drive and to protect

Advantages

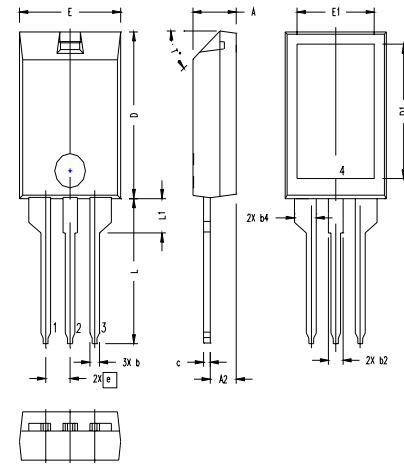
- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	3.0		5.5 V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$ $V_{GS} = 0 \text{ V}$ $T_J = 125^\circ\text{C}$			5 μA 50 μA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2 \%$			450 $\text{m}\Omega$

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
g_{fs}	V _{DS} = 20 V; I _D = 0.5 I _{D25} , pulse test	8	16	S
C_{iss} C_{oss} C_{rss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		2250	pF
			240	pF
			12	pF
t_{d(on)} t_r t_{d(off)} t_f	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = I _{D25} R _G = 18 Ω (External)		23	ns
			25	ns
			70	ns
			22	ns
Q_{g(on)} Q_{gs} Q_{gd}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} , I _D = 0.5 I _{D25}		43	nC
			15	nC
			12	nC
R_{thJC} R_{thCK}	(ISOPLUS220)		0.21	1.25 K/W K/W

Symbol	Test Conditions	Characteristic Values			
		(T _J = 25°C, unless otherwise specified)			
		Min.	typ.	Max.	
I_S	V _{GS} = 0 V			16 A	
I_{SM}	Repetitive			35 A	
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V	
t_{rr} I_{RM} Q_{RM}	I _F = 16 A, -di/dt = 100 A/μs V _R = 100 V		130	200 ns	
				6	A
				0.6	μC

ISOPLUS220 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5°	47.5°

- NOTE:
 1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
 2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 1. Output Characteristics @ 25°C

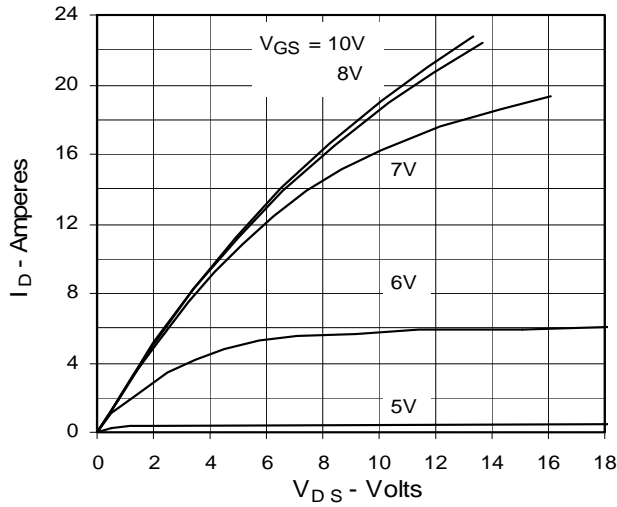


Fig. 2. Output Characteristics @ 125°C

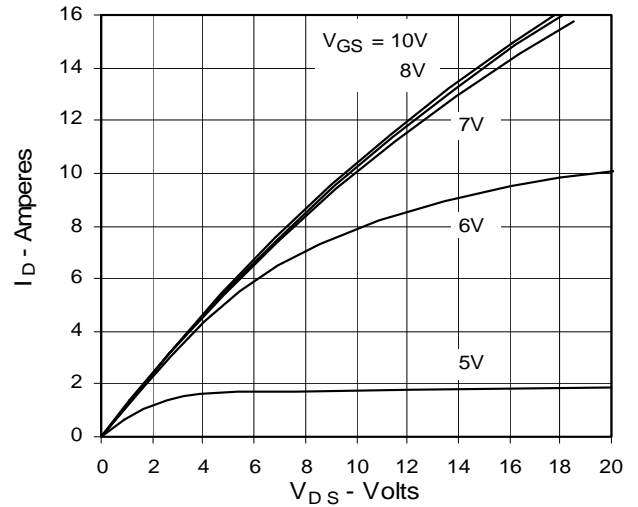


Fig. 3. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

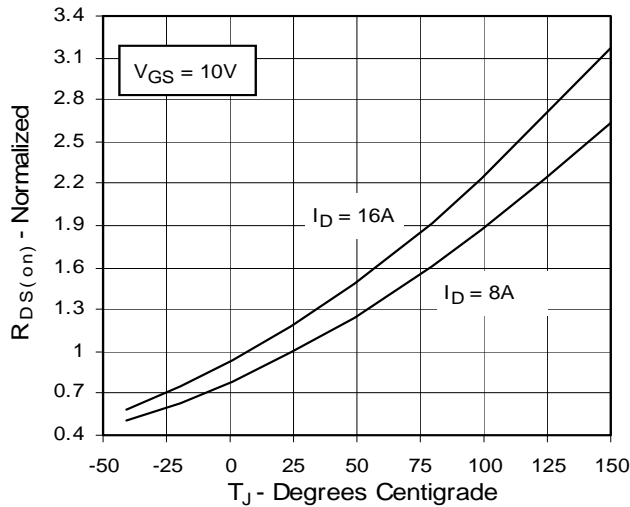


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

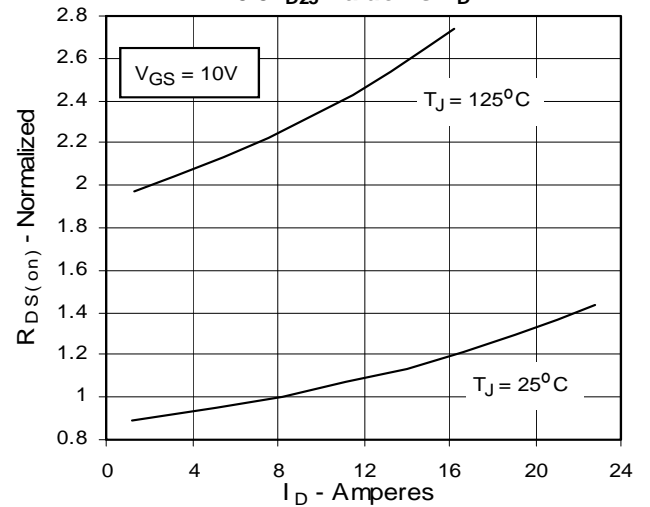


Fig. 5. Drain Current vs. Case Temperature

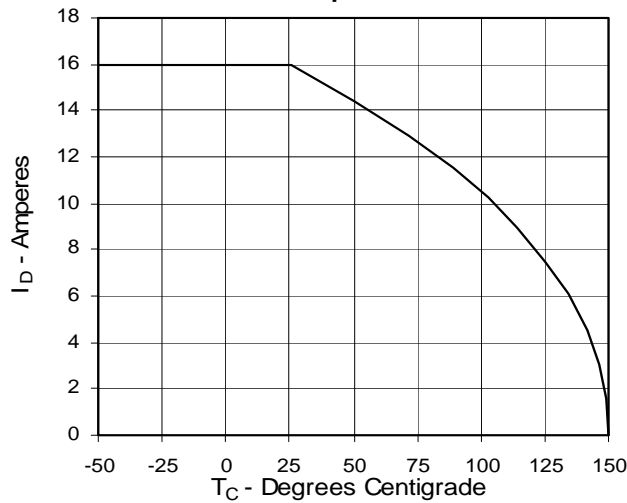


Fig. 6. Input Admittance

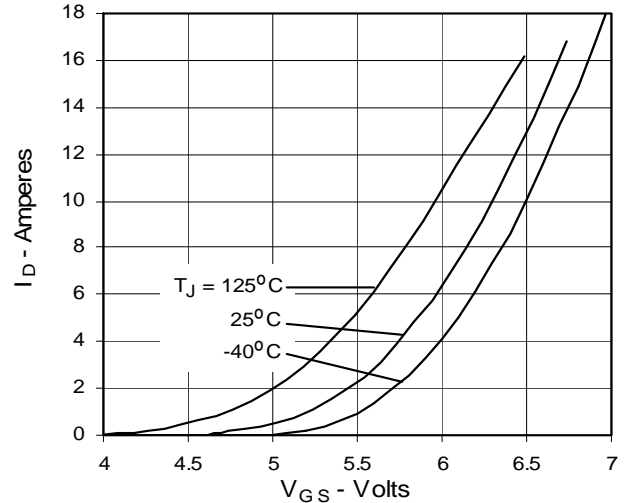


Fig. 7. Transconductance

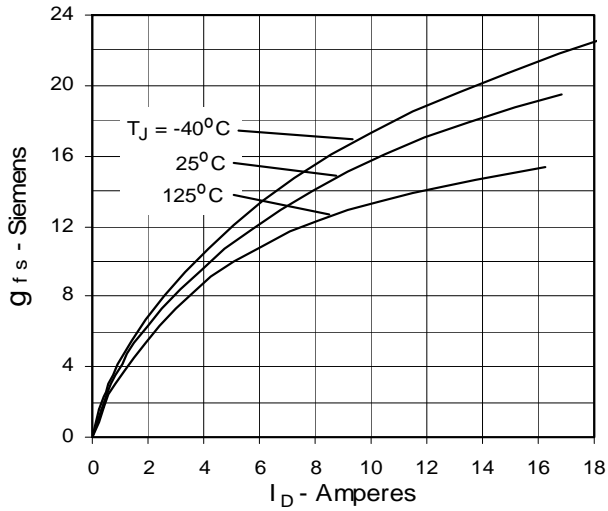


Fig. 8. Source Current vs. Source-To-Drain Voltage

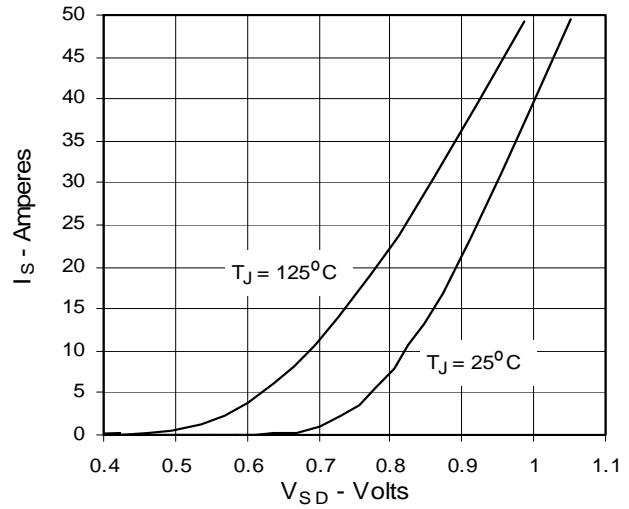


Fig. 10. Gate Charge

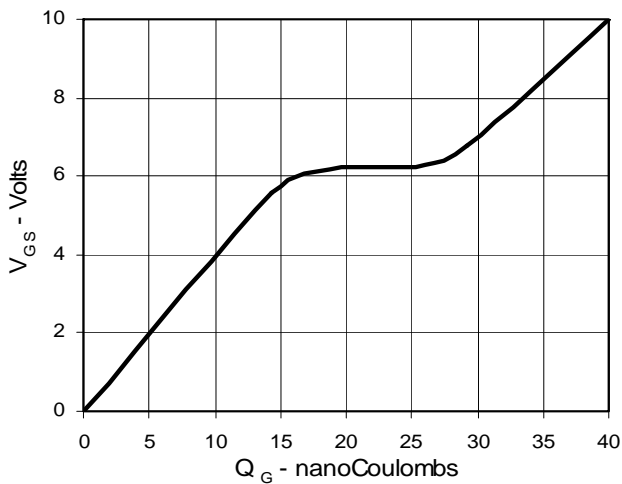


Fig. 10. Capacitance

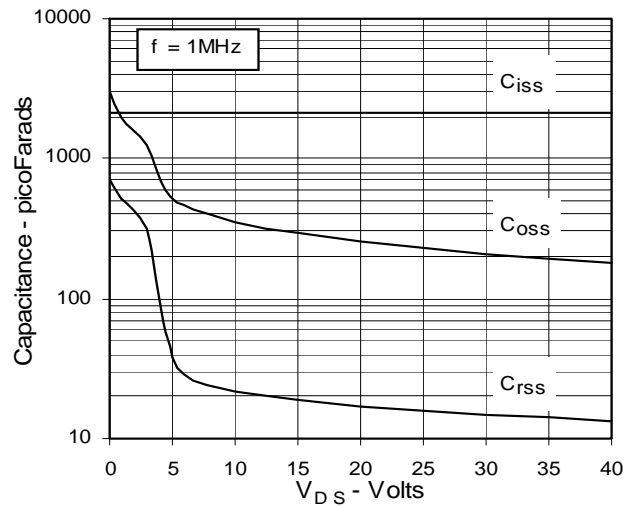


Fig. 11. Forward-Bias Safe Operating Area

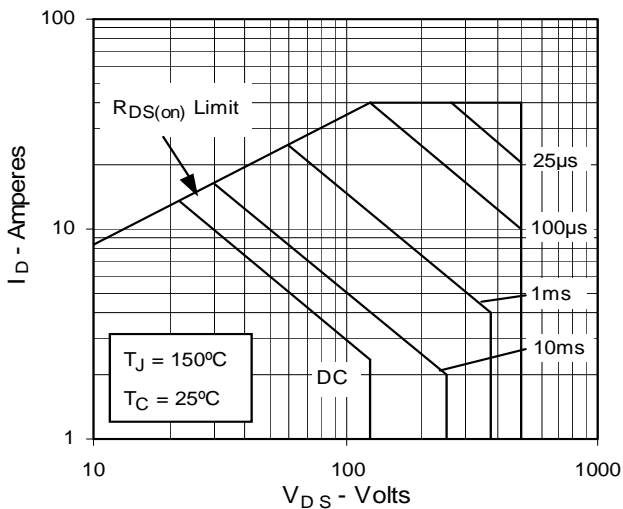


Fig. 12. Maximum Transient Thermal Resistance

