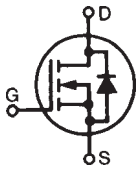
PolarHV™ HiPerFET Power MOSFET ISOPLUS247™

(Electrically Isolated Back Surface)

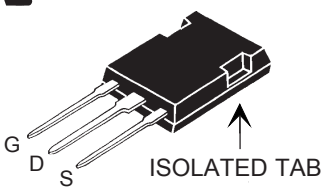
IXFR 44N50P

V_{DSS} = 500 V
I_{D25} = 24 A
$R_{DS(on)}$ ≤ 150 mΩ
t_{rr} ≤ 200 ns

N-Channel Enhancement
Avalanche Rated
Fast Intrinsic Diode



ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25° C to 175° C	500	V
V_{DGR}	T_J = 25° C to 175° C; R_{GS} = 1 MΩ	500	V
V_{GSM}	Transient	±40	V
V_{GSM}	Continuous	±30	V
I_{D25}	T_C = 25° C	24	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}	132	A
I_{AR}	T_C = 25° C	44	A
E_{AR}	T_C = 25° C	55	mJ
E_{AS}	T_C = 25° C	1.7	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤100 A/μs, $V_{DD} \le V_{DSS}$, T_J ≤150° C, R_G = 10 Ω	10	V/ns
P_D	T_C = 25° C	208	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_C	Mounting Force	20..120 / 4.5..25	N/lb
Weight		5	g

Features

- International standard isolated package
- UL recognized package
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±30 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$			25	μA
	V_{GS} = 0 V, T_J = 125° C			500	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 22 A			150	mΩ

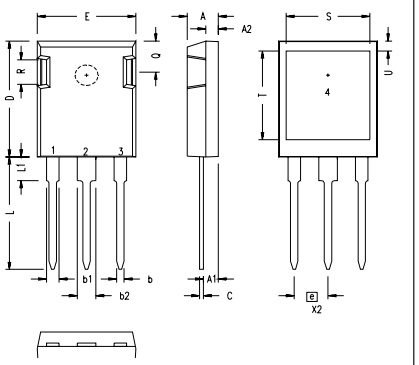
Symbol	Test Conditions	Characteristic Values (T_J = 25° C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS}= 20 V; I_D = 22 A, Note 1		32		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		5440		pF
C_{oss}			639		pF
C_{rss}			40		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 22 A R_G = 3 Ω (External)		25		ns
t_r			27		ns
$t_{d(off)}$			70		ns
t_f			18		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 22 A		98		nC
Q_{gs}			35		nC
Q_{gd}			30		nC
R_{thJC}				0.6	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25° C, unless otherwise specified) Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			30	A
I_{SM}	Repetitive			132	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 22 A,			200	ns
Q_{RM}	-di/dt = 100 A/µs		0.6		µC
I_{RM}	V_R = 100V		6.0		A

Notes: 1. Pulse test, t ≤300 ms, duty cycle d ≤2 %

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 1. Output Characteristics @ 25ºC

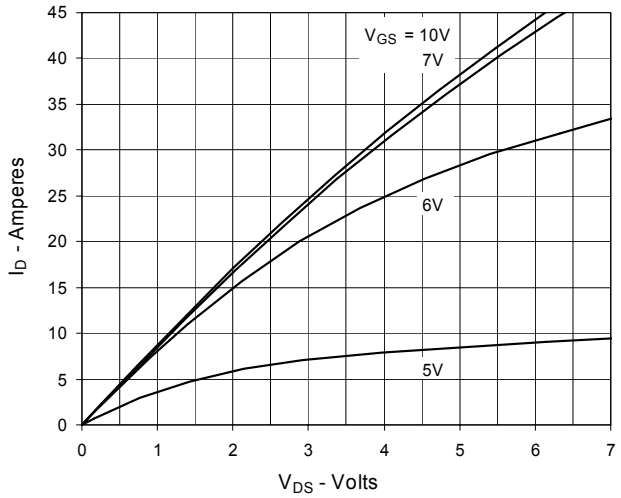


Fig. 2. Extended Output Characteristics @ 25ºC

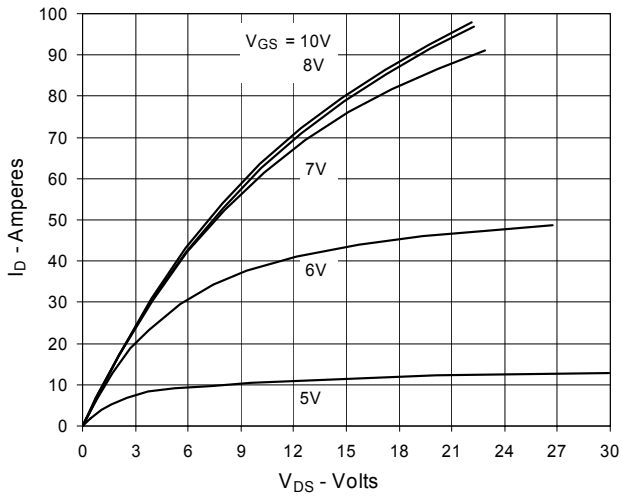


Fig. 3. Output Characteristics @ 125ºC

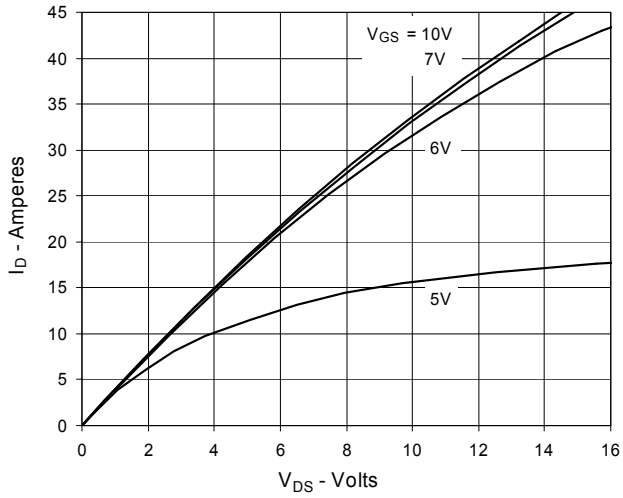


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Junction Temperature

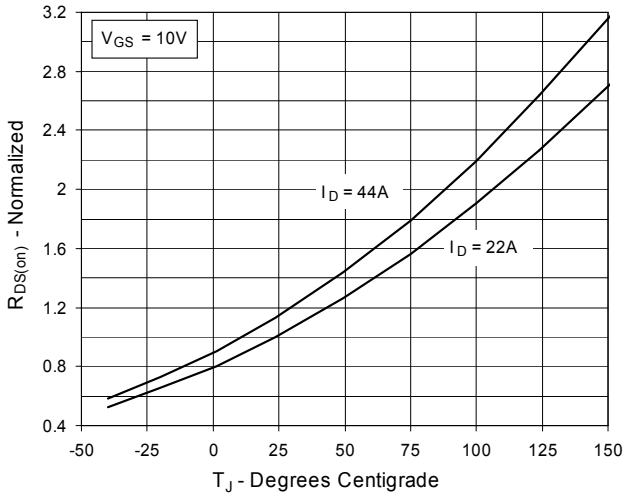


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Drain Current

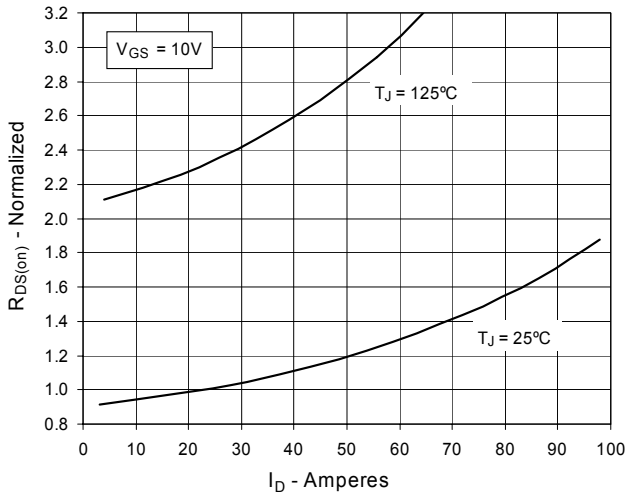


Fig. 6. Maximum Drain Current vs. Case Temperature

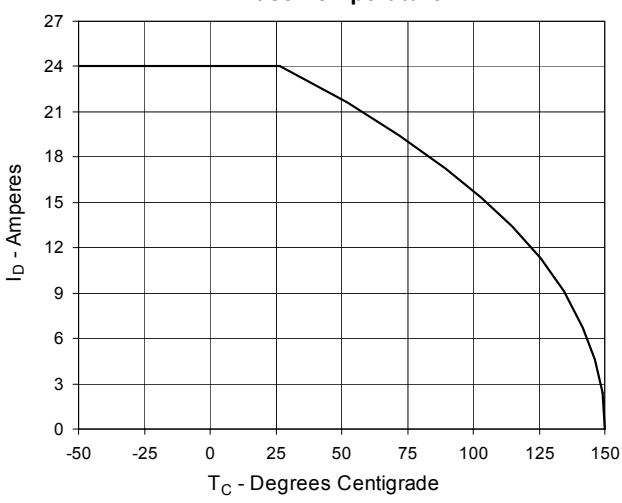


Fig. 7. Input Admittance

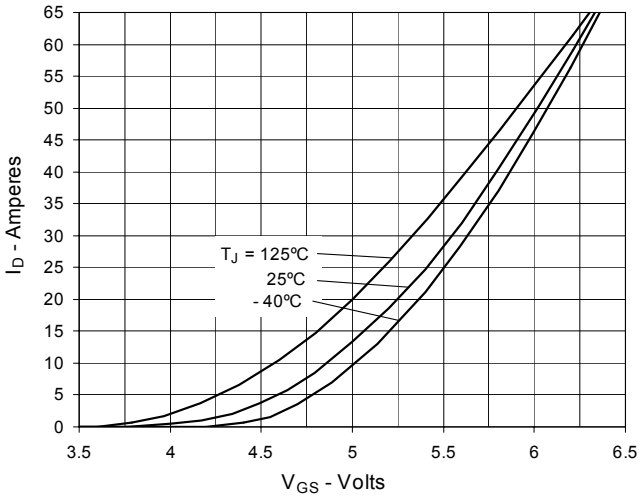


Fig. 8. Transconductance

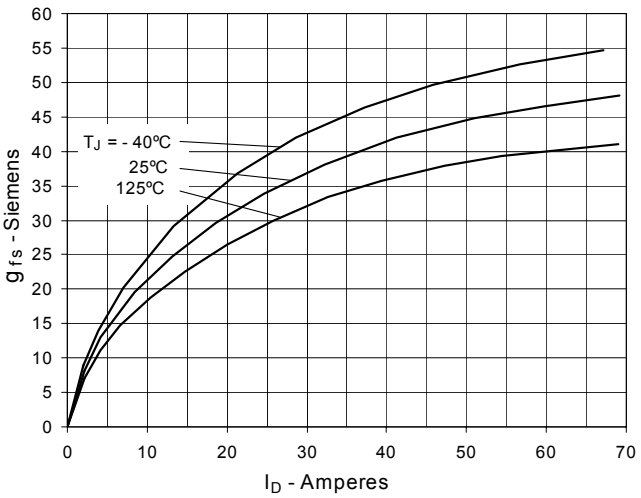


Fig. 9. Forward Voltage Drop of Intrinsic Diode

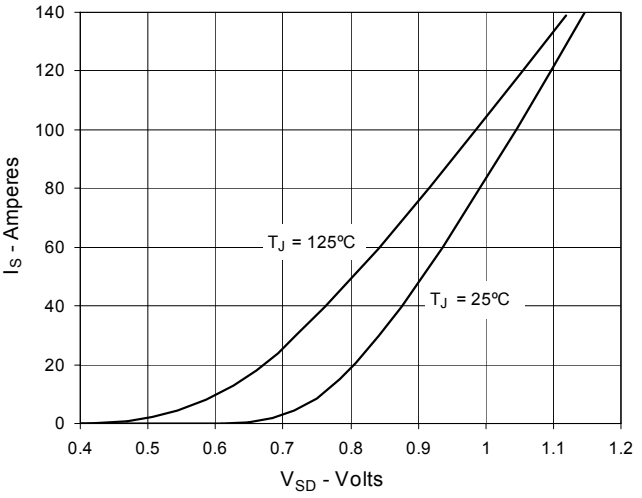


Fig. 10. Gate Charge

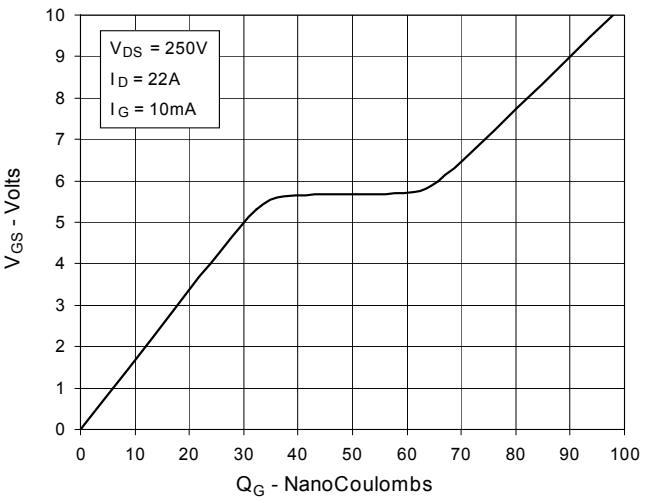


Fig. 11. Capacitance

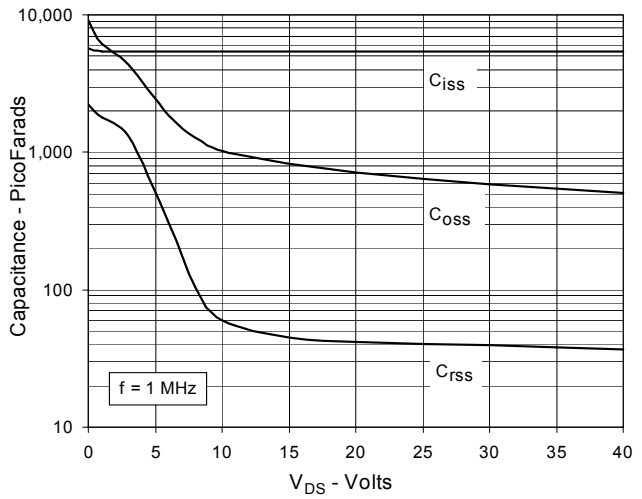


Fig. 12. Forward-Bias Safe Operating Area

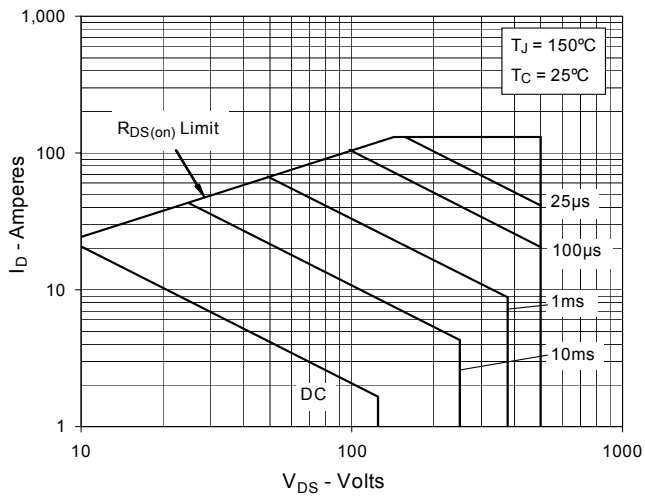


Fig. 13. Maximum Transient Thermal Resistance