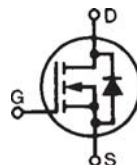


HiPerFET™ Power MOSFETs Q-Class

IXFR 66N50Q2

$V_{DSS} = 500 \text{ V}$
 $I_{D25} = 50 \text{ A}$
 $R_{DS(on)} = 85 \text{ m}\Omega$
 $t_{rr} \leq 250 \text{ ns}$

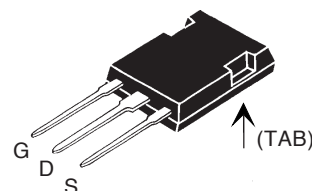
N-Channel Enhancement Mode
 Avalanche Rated, High dv/dt, Low Q_g
 Low intrinsic R_g , low t_{rr}



Preliminary Data Sheet

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	500	V
V_{GS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ\text{C}$	50	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	264	A
I_{AR}	$T_C = 25^\circ\text{C}$	66	A
E_{AR}	$T_C = 25^\circ\text{C}$	75	mJ
E_{AS}	$T_C = 25^\circ\text{C}$	4.0	J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_g = 2 \Omega$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	500	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	1.6 mm (0.063 in) from case for 10 s	300	$^\circ\text{C}$
F_C	Mounting force	22...130/5...30	N/lb
Weight		5	g

ISOPLUS247™ (IXFR)



G = Gate
 S = Source
 D = Drain
 TAB = Drain

Features

- Double metal process for low gate resistance
- International standard packages
- Epoxy meet UL 94 V-0, flammability classification
- Avalanche energy and current rated
- Fast intrinsic Rectifier

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$ unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ mA}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	2.0		V
I_{GSS}	$V_{GS} = \pm 30 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$			50 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = I_T$ Pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2\%$			85 m Ω

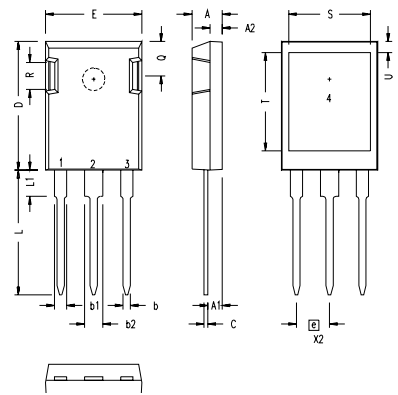
Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
		min.	typ.	max.
g_{fs}	V _{DS} = 10 V; I _D = I _T , pulse test	30	44	S
C_{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		6800	pF
C_{oss}			1200	pF
C_{rss}			270	pF
t_{d(on)}	V _{GS} = 10 V, V _{DS} = 0.5 i V _{DSS} , I _D = I _T R _G = 1.0 Ω (External),		32	ns
t_r			16	ns
t_{d(off)}			60	ns
t_f			10	ns
Q_{g(on)}	V _{GS} = 10 V, V _{DS} = 0.5 i V _{DSS} , I _D = I _T		199	nC
Q_{gs}			42	nC
Q_{gd}			92	nC
R_{thJC}			0.25	KW
R_{thCK}			0.15	KW

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C, unless otherwise specified)		
		min.	typ.	max.
I_S	V _{GS} = 0 V			66 A
I_{SM}	Repetitive; pulse width limited by T _{JM}			264 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
t_{rr}	I _F = 25A, -di/dt = 100 A/μs, V _R = 100 V		1	250 ns
Q_{RM}			10	μC
I_{RM}				

Note: Test current I_T = 33A

ISOPLUS247 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

- 1 - GATE
- 2 - DRAIN (COLLECTOR)
- 3 - SOURCE (EMITTER)
- 4 - NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline 10-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 1. Output Characteristics @ 25°C

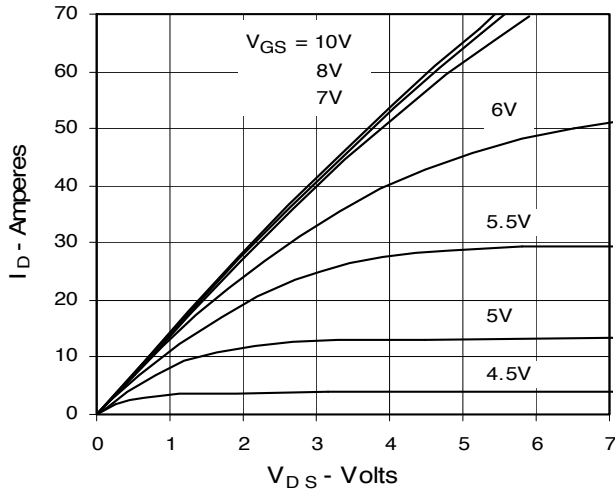


Fig. 2. Extended Output Characteristics @ 25°C

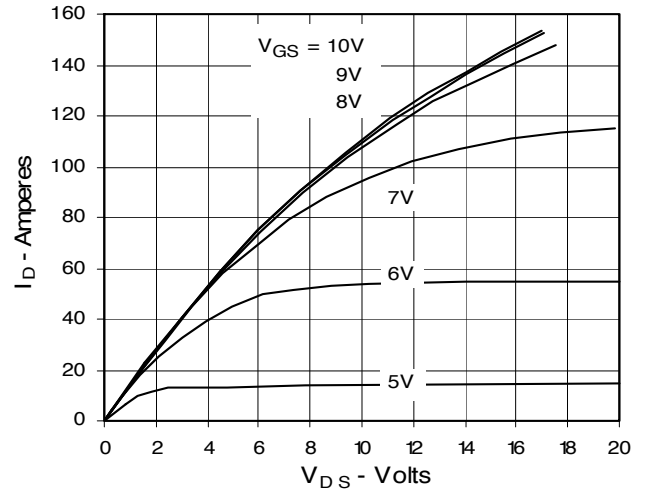


Fig. 3. Output Characteristics @ 125°C

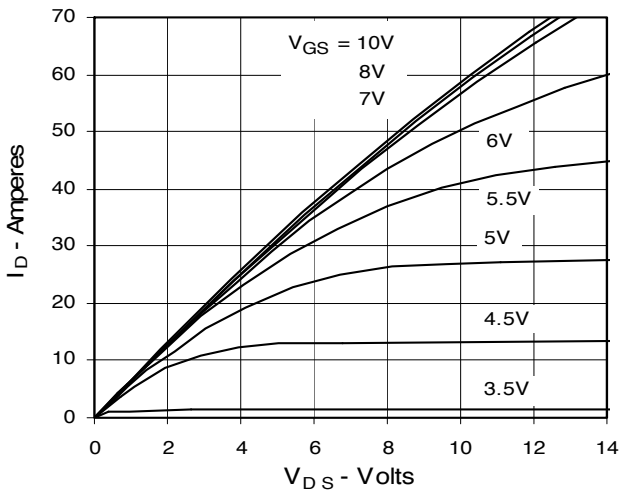


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

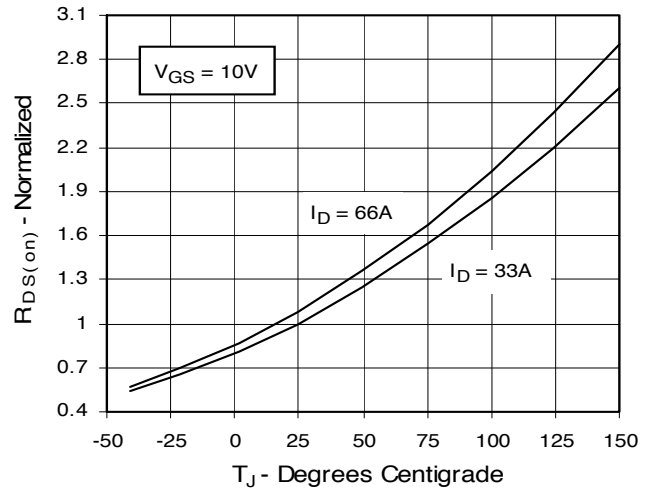


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

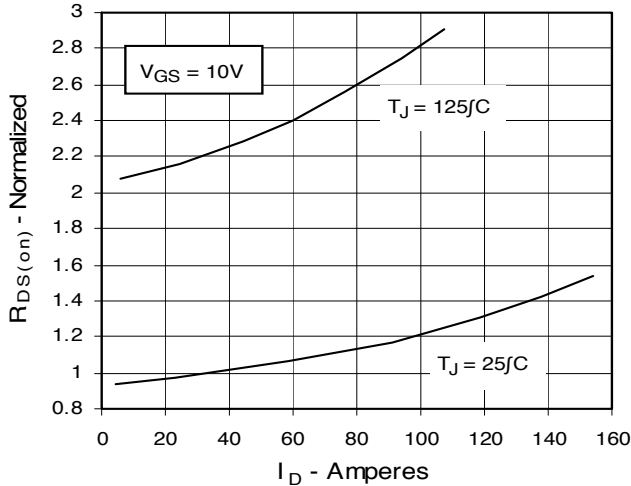


Fig. 6. Drain Current vs. Case Temperature

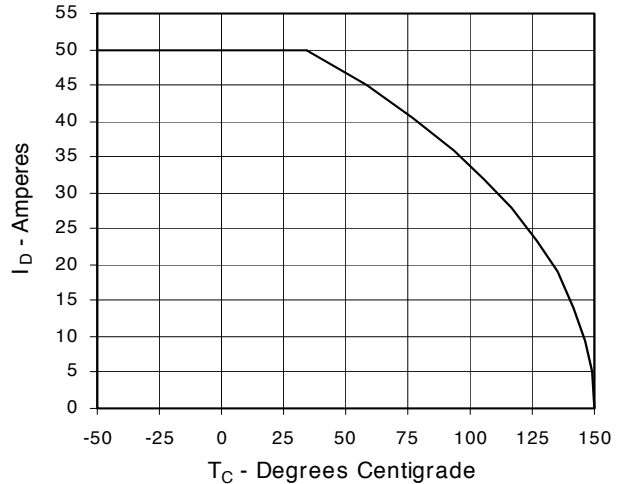


Fig. 7. Input Admittance

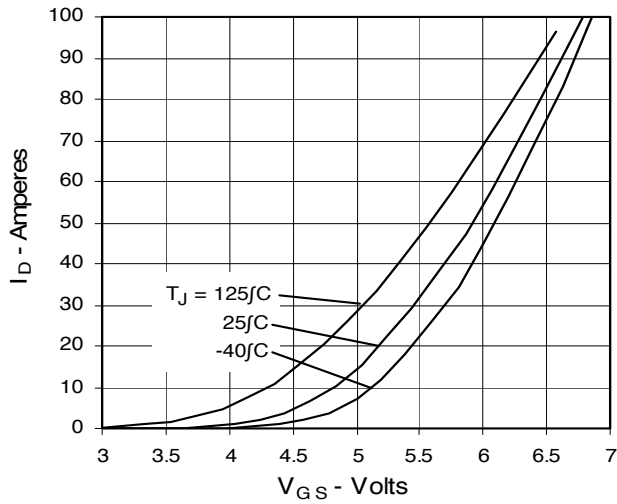


Fig. 8. Transconductance

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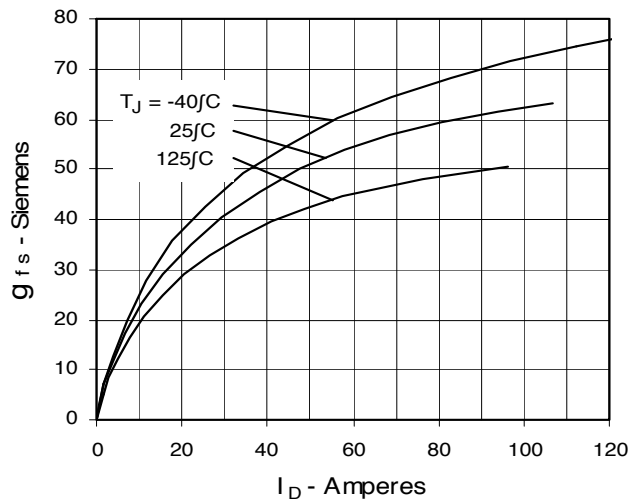


Fig. 9. Source Current vs. Source-To-Drain Voltage

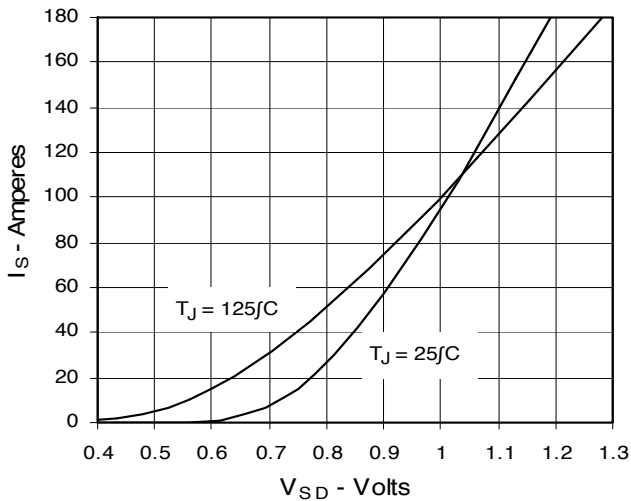


Fig. 10. Gate Charge

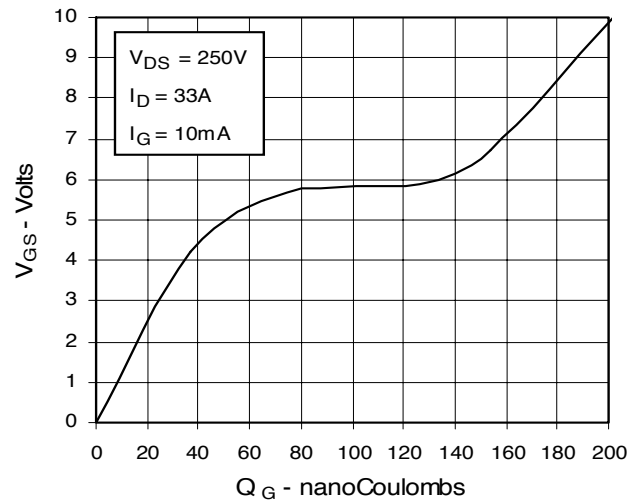


Fig. 11. Capacitance

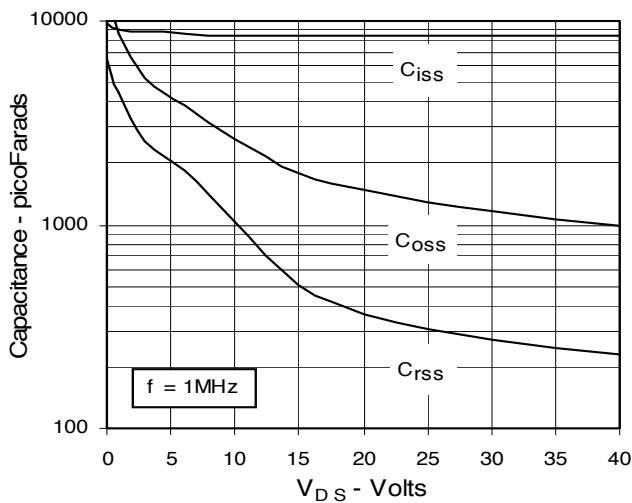


Fig. 12. Forward-Bias Safe Operating Area

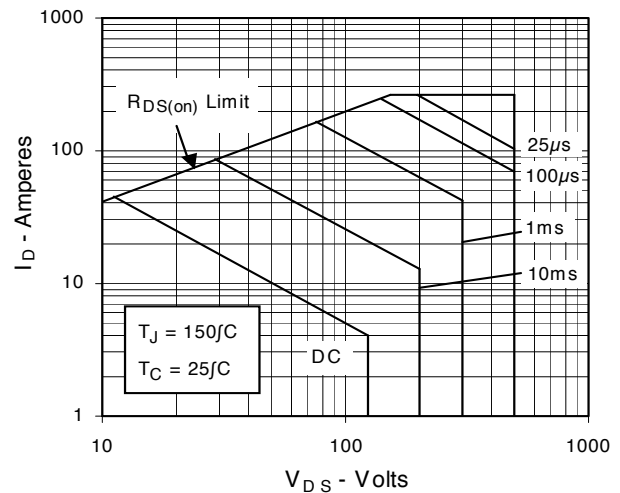


Fig. 13. Maximum Transient Thermal Resistance

