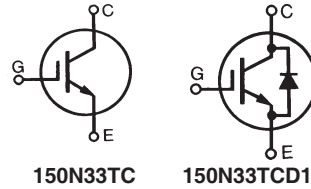


Trench Gate High Speed IGBT

IXGA150N33TC
IXGQ150N33TC
IXGQ150N33TCD1

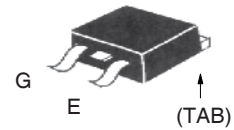
$V_{CES} = 330V$
 $I_{CP} = 400A$
 $V_{CE(sat)} \leq 1.8V$

For PDP Applications

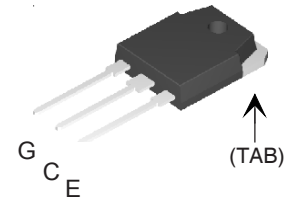


Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_C = 25^\circ C$ to $150^\circ C$	330	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$, IGBT chip capability	150	A
I_{CP}	$T_J \leq 150^\circ C$, $tp < 10 \mu s$	400	A
I_{DP}	$T_J \leq 150^\circ C$, $tp < 10 \mu s$	40	A
$I_{C(RMS)}$	Lead current limit	75	A
P_C	$T_C = 25^\circ C$	300	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	1.6mm (0.062 in.) from case for 10s	300	$^\circ C$
T_{SOLD}	Plastic body for 10 seconds	260	$^\circ C$
M_d	Mounting torque (TO-220)(TO-3P)	1.13/10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-3P	5.5	g

TO-263 (IXGA)



TO-3P (IXGQ)



G = Gate C = Collector
 E = Emitter TAB = Collector

Symbol	Test Conditions ($T_J = 25^\circ C$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250 \mu A$, $V_{GE} = 0V$	330		V
$V_{GE(th)}$	$I_C = 250 \mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 330 V$			1 μA
	$V_{GE} = 0 V$ $T_J = 125^\circ C$			200 μA
I_{GES}	$V_{CE} = 0 V$, $V_{GE} = \pm 20 V$			± 100 nA
$V_{CE(sat)}$	$V_{GE} = 15V$, $I_C = 75A$		1.48	1.8 V
		$T_J = 125^\circ C$	1.49	V
	$I_C = 150A$		1.83	V
	$T_J = 125^\circ C$		1.97	V

Features

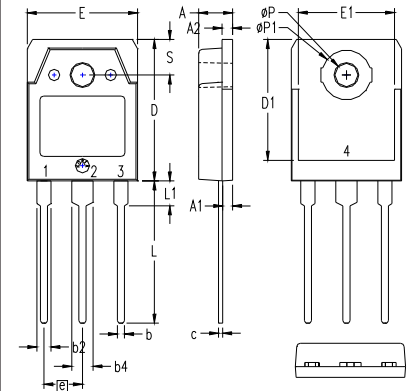
- International standard packages
- Low $V_{CE(sat)}$
 - for minimum on-state conduction losses
- Fast switching

Applications

- PDP Screen Drivers

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 75A, V_{CE} = 10V, \text{Note 1}$	65	103	S
C_{ies}	$V_{CE} = 25V, V_{GE} = 0V, f = 1\text{ MHz}$		4270	pF
C_{oes}			308	pF
C_{res}			49	pF
Q_g	$I_C = 75A, V_{GE} = 15V, V_{CE} = 0.5 \cdot V_{CES}$		118	nC
Q_{ge}			25	nC
Q_{gc}			25	nC
$t_{d(on)}$	Resistive load, $T_J = 25^\circ\text{C}$		17	ns
t_{ri}			29	ns
$t_{d(off)}$			42	ns
t_{fi}			54	ns
$t_{d(on)}$	Resistive load, $T_J = 125^\circ\text{C}$		17	ns
t_{ri}			25	ns
$t_{d(off)}$			59	ns
t_{fi}			73	ns
R_{thJC}	TO-3P		0.25	0.42 °C/W
R_{thCH}				°C/W

TO-3P (IXGQ) Outline



Pins: 1 - Gate 2 - Drain
3 - Source 4, TAB - Drain

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.791	19.80	20.10
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP	.126	.134	3.20	3.40
øP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

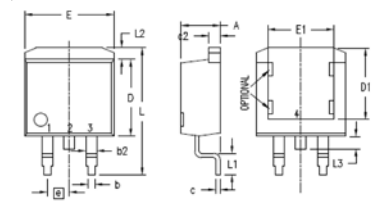
All metal area are tin plated.

Reverse Diode

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
V_F	$I_F = 20A, V_{GE} = 0V$			2.0 V
R_{thJC}				2.5 °C/W

Characteristic Values
($T_J = 25^\circ\text{C}$, unless otherwise specified)

TO-263 (IXGA) Outline



1. GATE
2. DRAIN (COLLECTOR)
3. SOURCE (EMITTER)
4. DRAIN (COLLECTOR)
BOTTOM SIDE

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
A1	.080	.110	2.03	2.79
b	.020	.039	0.51	0.99
b2	.045	.055	1.14	1.40
c	.016	.029	0.40	0.74
c2	.045	.055	1.14	1.40
D	.340	.380	8.64	9.65
D1	.315	.350	8.00	8.89
E	.380	.410	9.65	10.41
E1	.245	.320	6.22	8.13
e	.100 BSC		2.54 BSC	
L	.575	.625	14.61	15.88
L1	.090	.110	2.29	2.79
L2	.040	.055	1.02	1.40
L3	.050	.070	1.27	1.78
L4	0	.005	0	0.13

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ 25°C

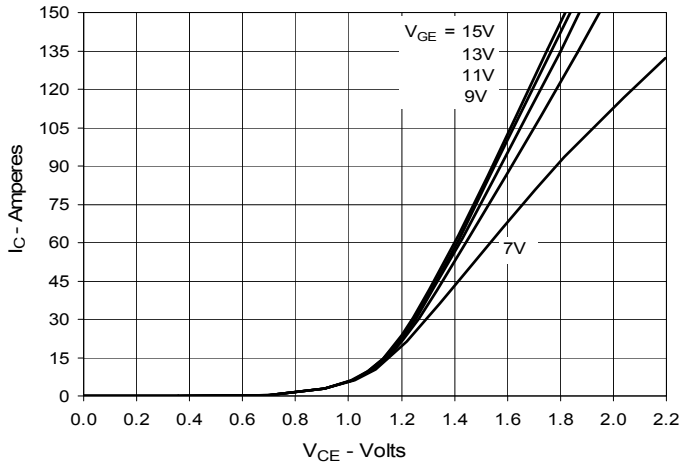


Fig. 2. Extended Output Characteristics @ 25°C

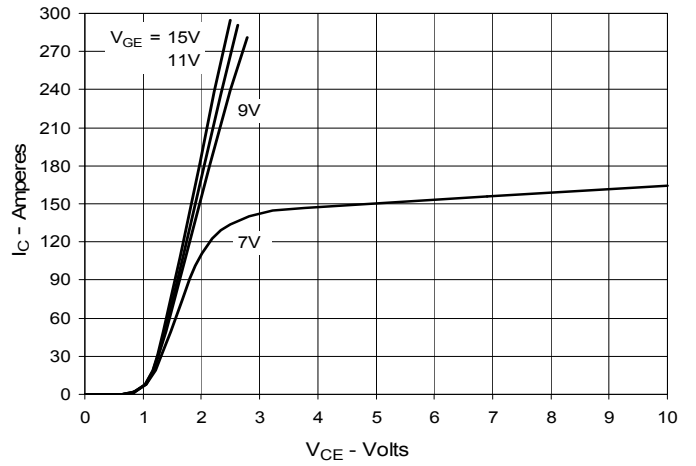


Fig. 3. Output Characteristics @ 125°C

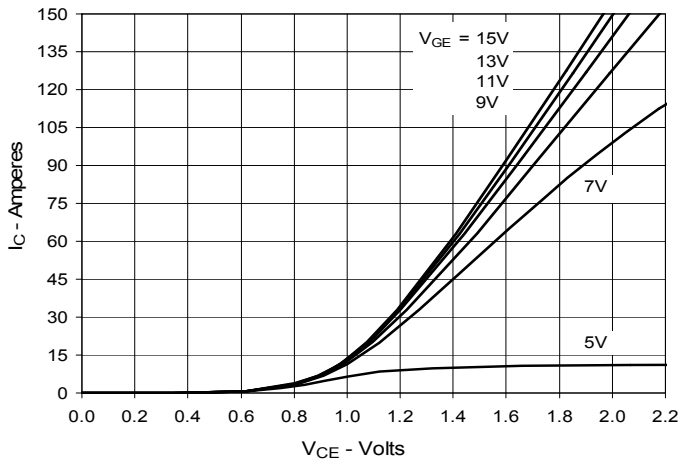


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

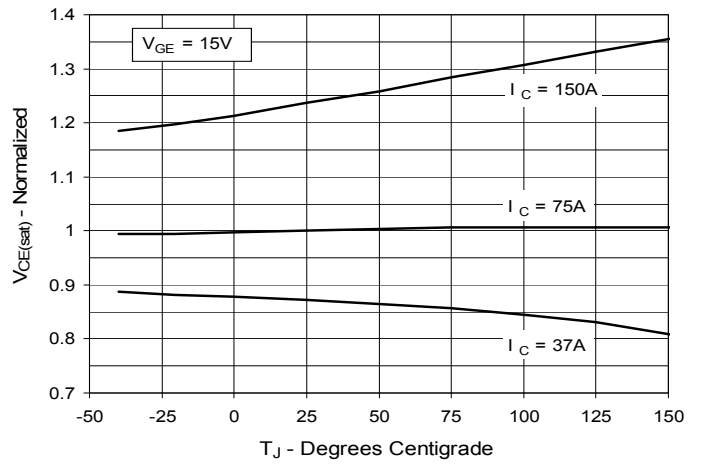


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

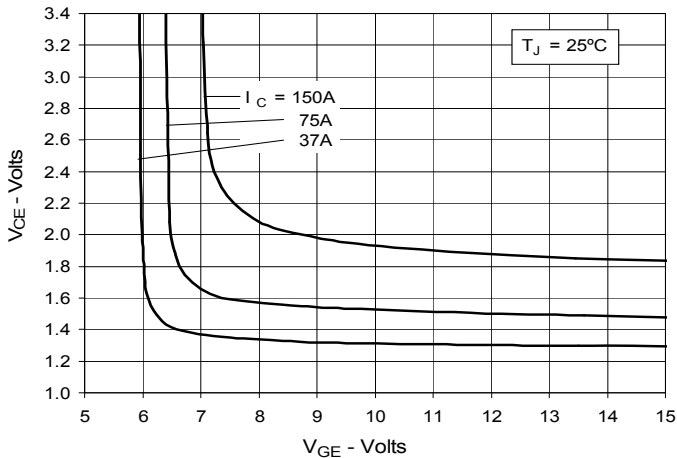


Fig. 6. Input Admittance

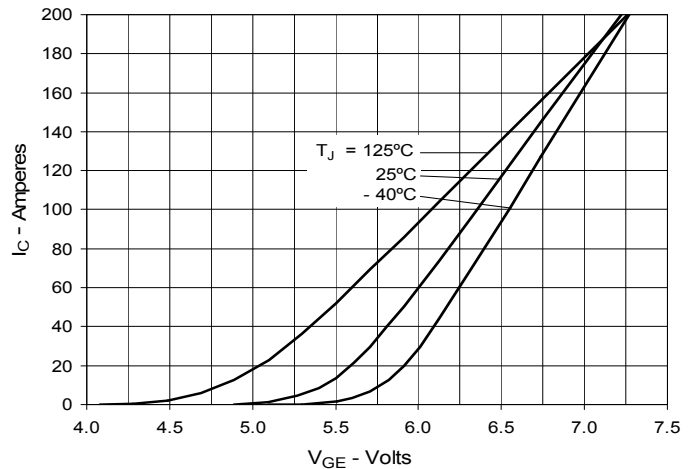


Fig. 7. Transconductance

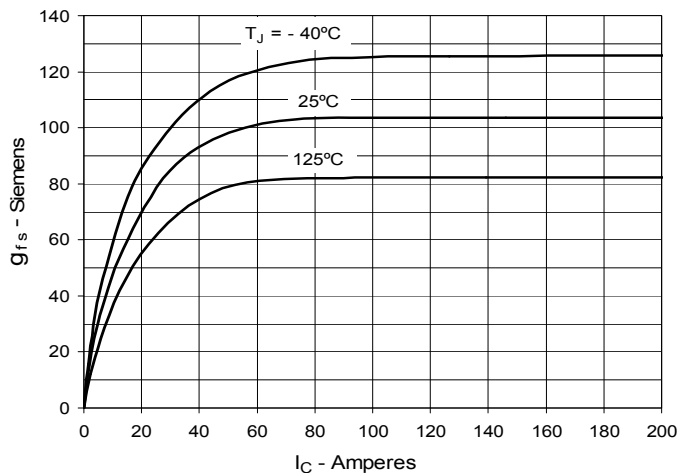


Fig. 8. Gate Charge

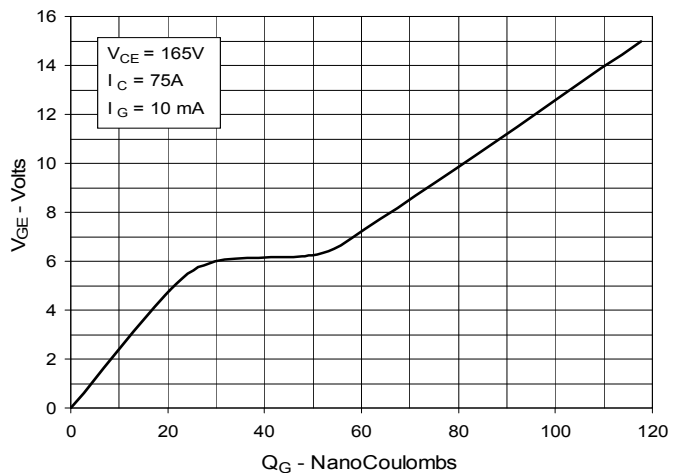


Fig. 9. Reverse-Bias Safe Operating Area

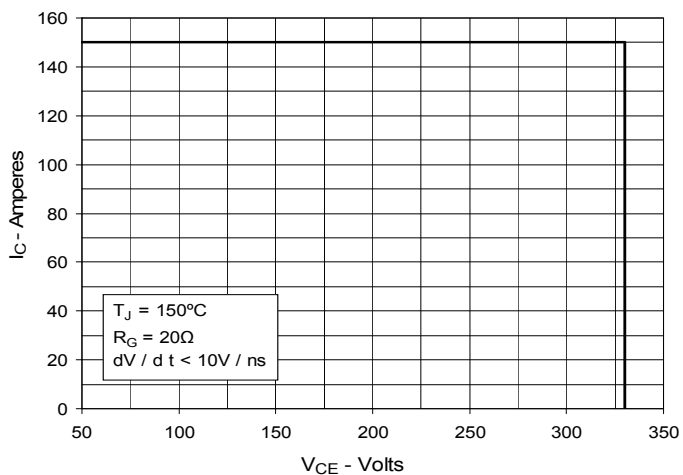


Fig. 10. Capacitance

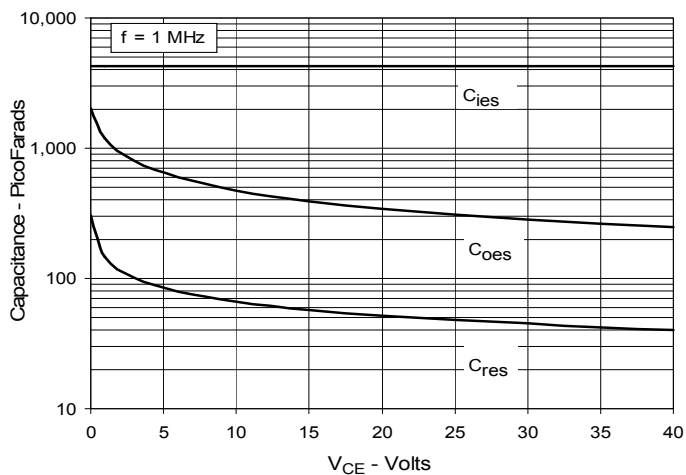


Fig. 11. Forward-Bias Safe Operating Area

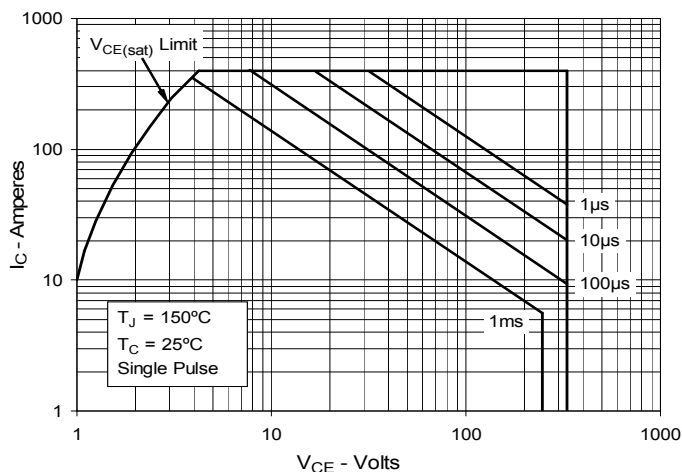


Fig. 12. Maximum Transient Thermal Impedance

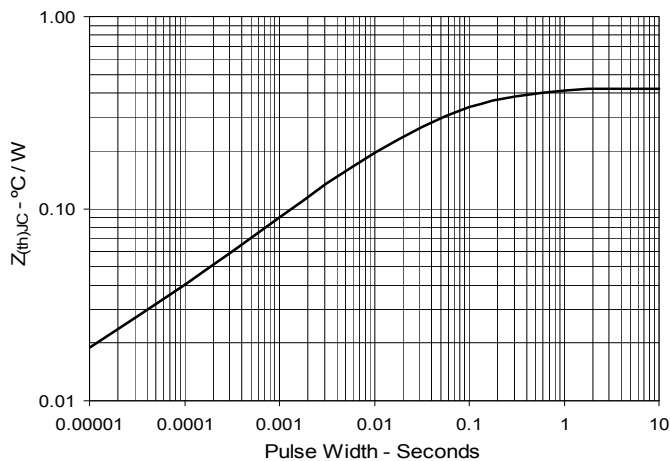


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

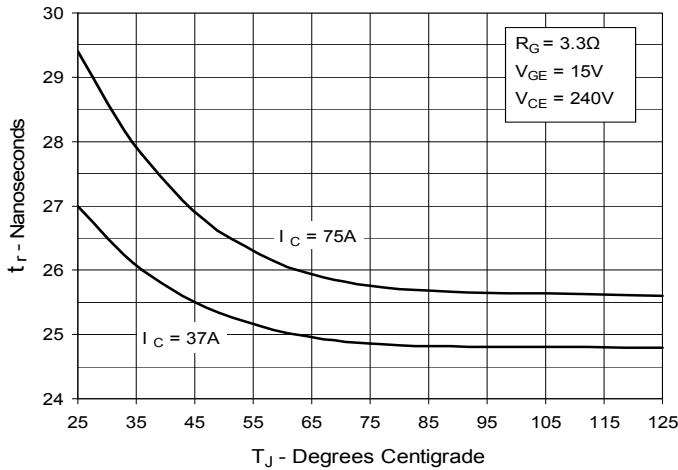


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

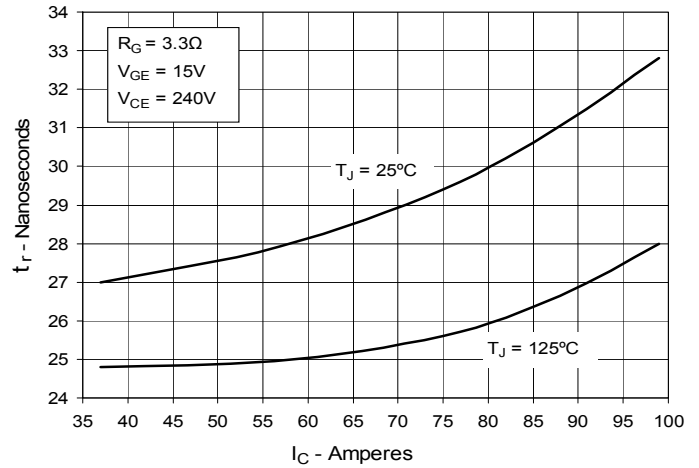


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

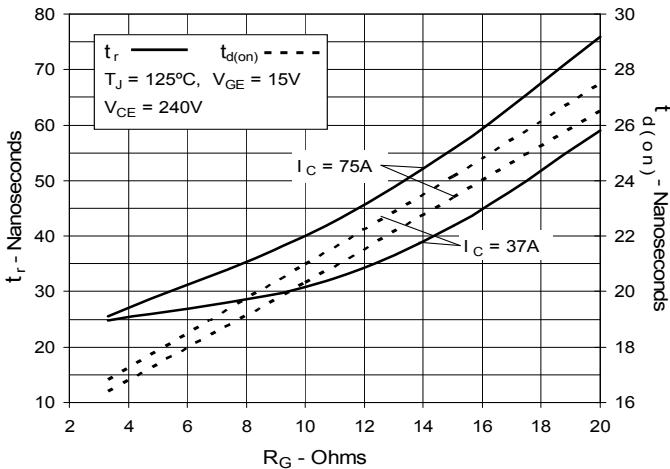


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

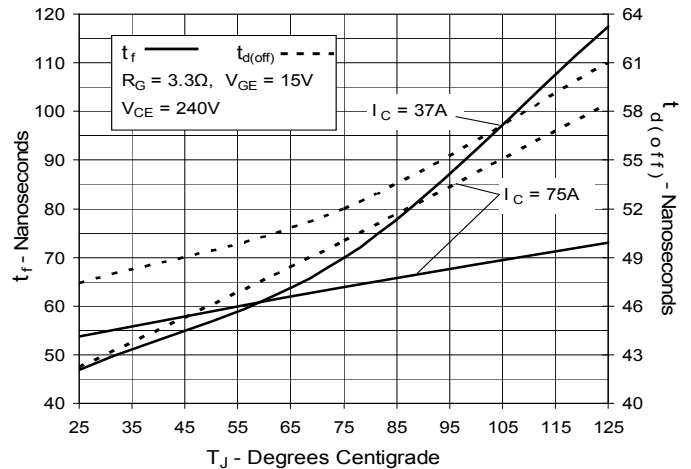


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

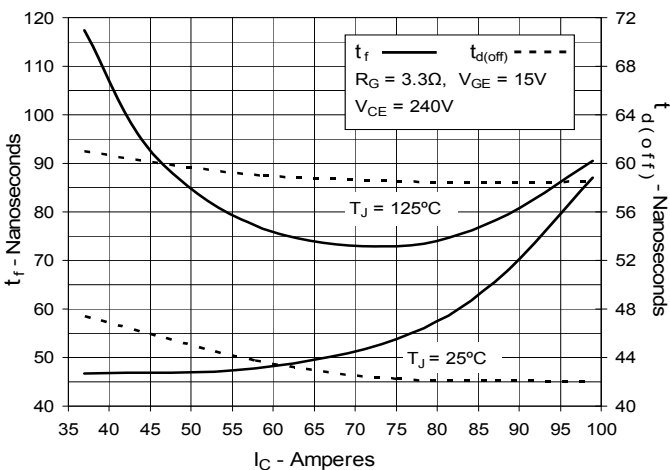


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

