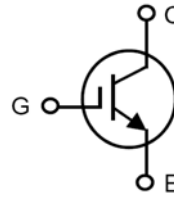


For Capacitor Discharge Applications

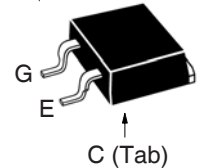


$$V_{CES} = 2500V$$

$$I_{C110} = 12A$$

$$V_{CE(sat)} \leq 3.1V$$

TO-263HV



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ C$ to $150^\circ C$	2500	V
V_{GGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GE} = 1M\Omega$	2500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ C$	30	A
I_{C110}	$T_C = 110^\circ C$	12	A
I_{CM}	$T_C = 25^\circ C$, $V_{GE} = 19V$, 1ms 10ms	105	A
		55	A
SSOA	$V_{GE} = 15V$, $T_{VJ} = 125^\circ C$, $R_G = 20\Omega$	$I_{CM} = 60$	A
(RBSOA)	Clamped Inductive Load	1500	V
P_C	$T_C = 25^\circ C$	150	W
T_J		-55 ... +150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55 ... +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		2.3	g

Features

- International Standard Package
- High Voltage Package
- Electrically Isolated Tab
- High Peak Current Capability
- Low Saturation Voltage
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Advantages

- High Power Density
- Easy to Mount

Applications

- Capacitor Discharge
- Pulsar Circuits

Symbol	Test Conditions ($T_J = 25^\circ C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	2500		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ $T_J = 125^\circ C$			25 μA 750 μA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 20A$, $V_{GE} = 15V$, Note 1			3.1 V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 20\text{A}$, $V_{CE} = 10\text{V}$, Note 1	8	13	S
$I_{C(ON)}$	$V_{GE} = 20\text{V}$, $V_{CE} = 15\text{V}$, Note 1		190	A
C_{ies}	$V_{CE} = 15\text{V}$, $V_{GE} = 25\text{V}$, $f = 1\text{MHz}$		1190	pF
C_{oes}			53	pF
C_{res}			18	pF
Q_g	$I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 1000\text{V}$		53	nC
Q_{ge}			8	nC
Q_{gc}			22	nC
$t_{d(on)}$	Resistive Switching Times $I_C = 40\text{A}$, $V_{GE} = 15\text{V}$, Note 1 $V_{CE} = 1250\text{V}$, $R_G = 10\Omega$		57	ns
t_r			160	ns
$t_{d(off)}$			136	ns
t_f			930	ns
R_{thJC}				0.83 $^\circ\text{C/W}$

Note 1. Pulse test, $t < 300\mu\text{s}$, duty cycle, $d < 2\%$.

TO-263HV Outline

CREEPAGE DISTANCE		
DESCRIPTION	SYMBOL	MIN DISTANCE
LEAD TO LEAD AIR CLEARANCE	e2	0.163 [4.15mm]
LEAD TO LEAD Pkg SURFACE CREEPAGE	e2	0.165 [4.20mm]
LEAD TO BOTTOM DRAIN CREEPAGE	A2+D2	0.177 [4.50mm]

SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.054	1.18	1.38
C	.018	.024	0.45	0.60
C2	.049	.055	1.25	1.40
D	.354	.370	9.00	9.40
D1	.311	.327	7.90	8.30
D2	.083	.098	2.10	2.50
E	.386	.402	9.80	10.20
E1	.307	.323	7.80	8.20
e1	.200	BSC	5.08	BSC
(e2)	.163	.174	4.13	4.43
H	.591	.614	15.00	15.60
L	.079	.102	2.00	2.60
L1	.039	.055	1.00	1.40
L3	.010	BSC	0.254	BSC
(L4)	.071	.087	1.80	2.20

NOTE:

1. These dimensions do not include mold protrusion.
2. () is reference dimension only.
3. Metal finish – Matte pure tin plating except trim area.
4. Pin call out: 1- Gate; 2 - Emitter; 3 - Collector

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

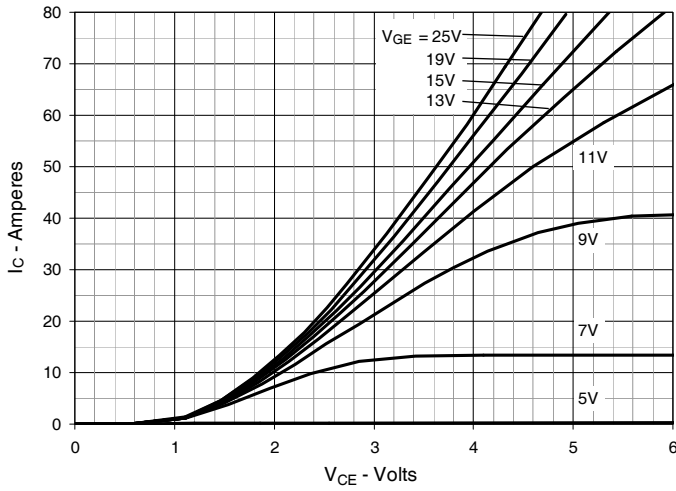


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

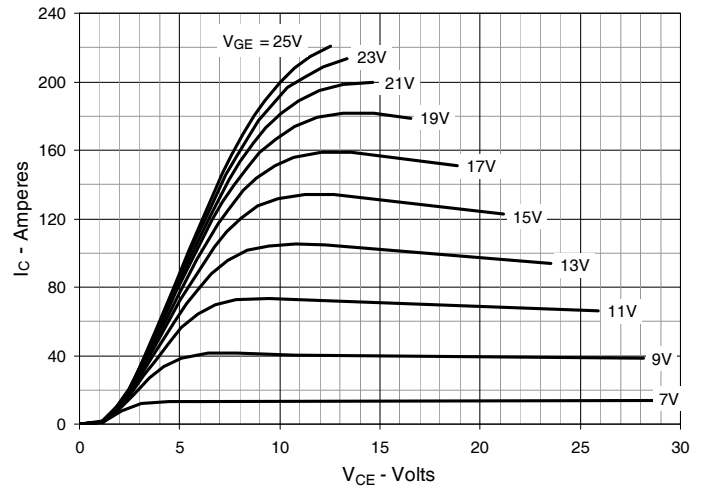


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

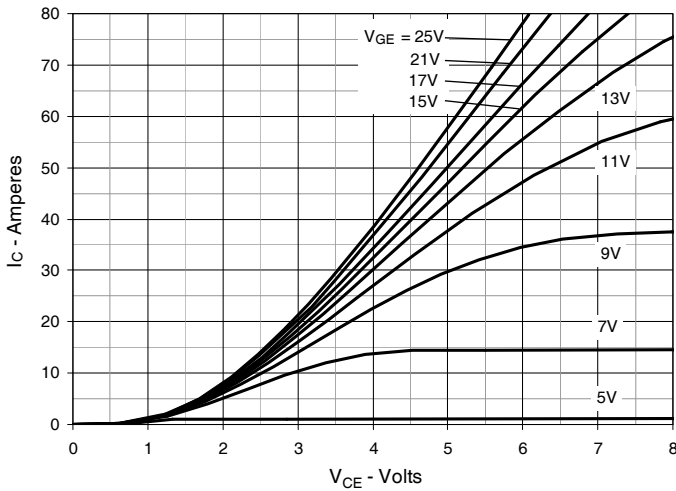


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

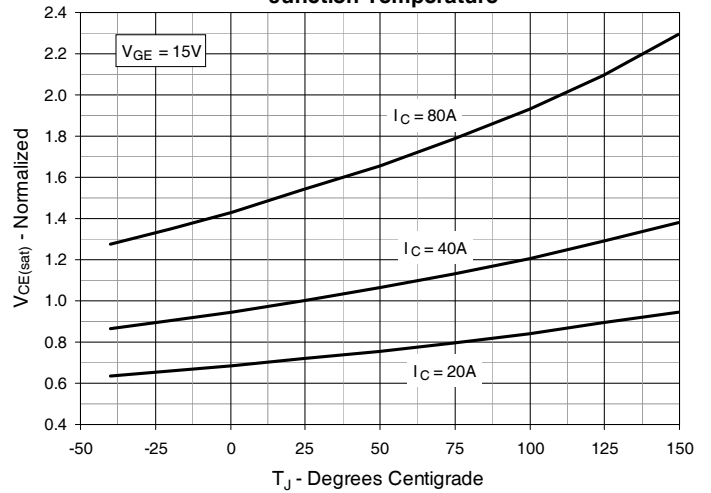


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

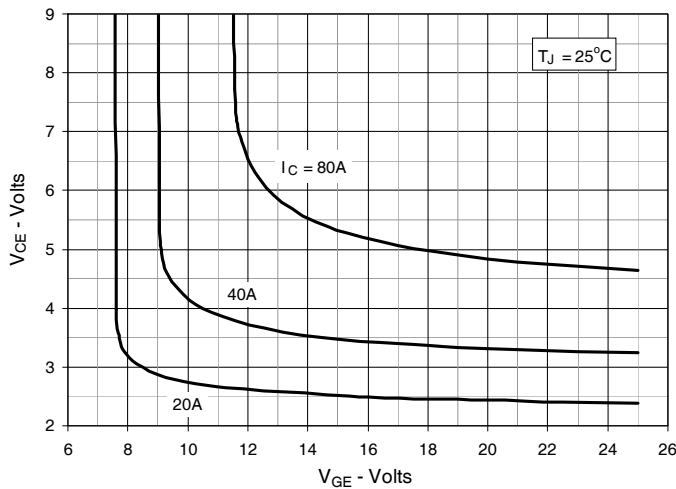


Fig. 6. Input Admittance

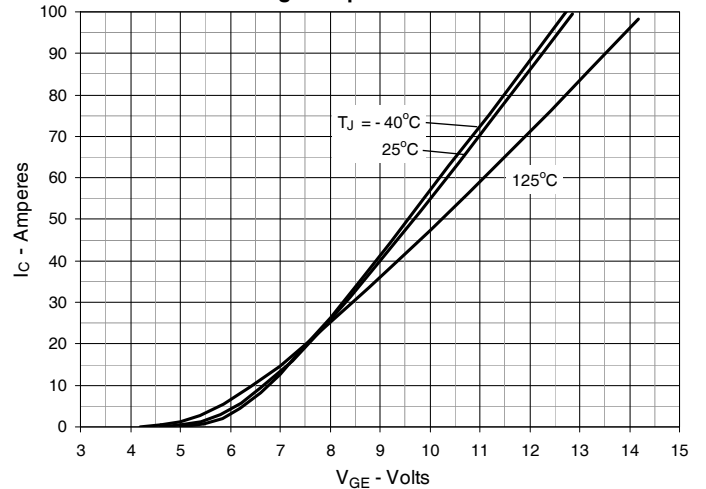


Fig. 7. Transconductance

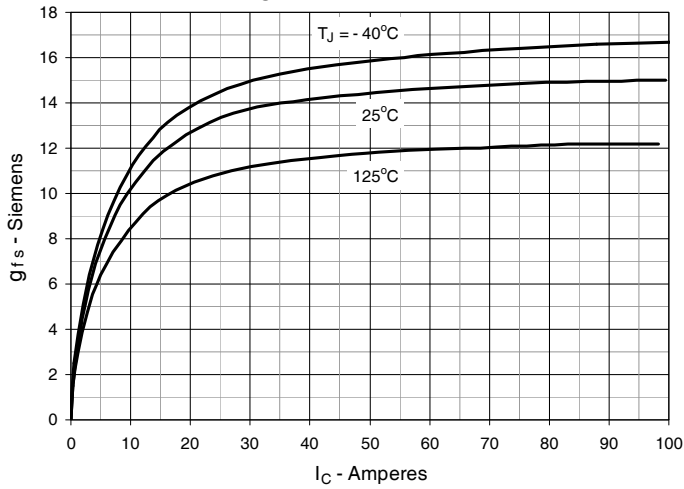


Fig. 8. Gate Charge

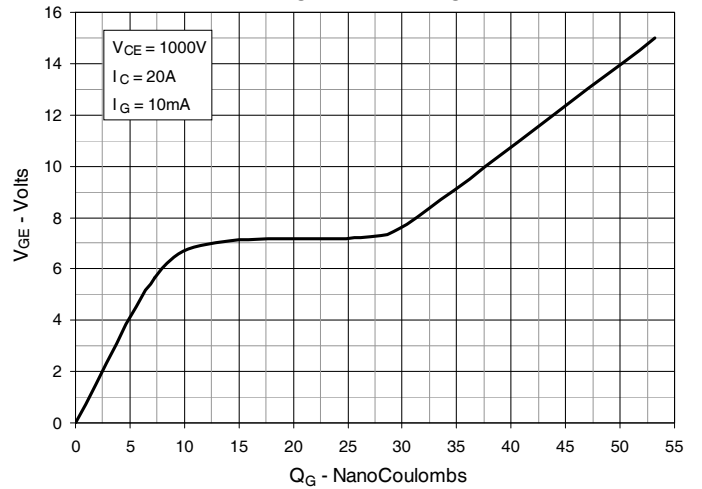


Fig. 9. Reverse-Bias Safe Operating Area

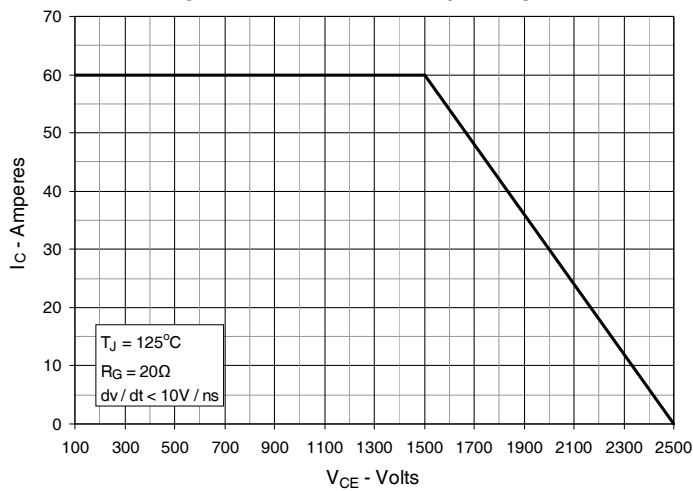


Fig. 10. Capacitance

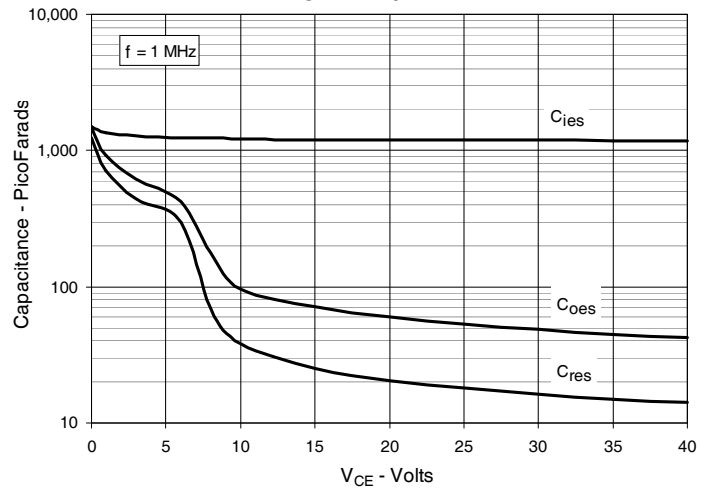


Fig. 11. Maximum Transient Thermal Impedance

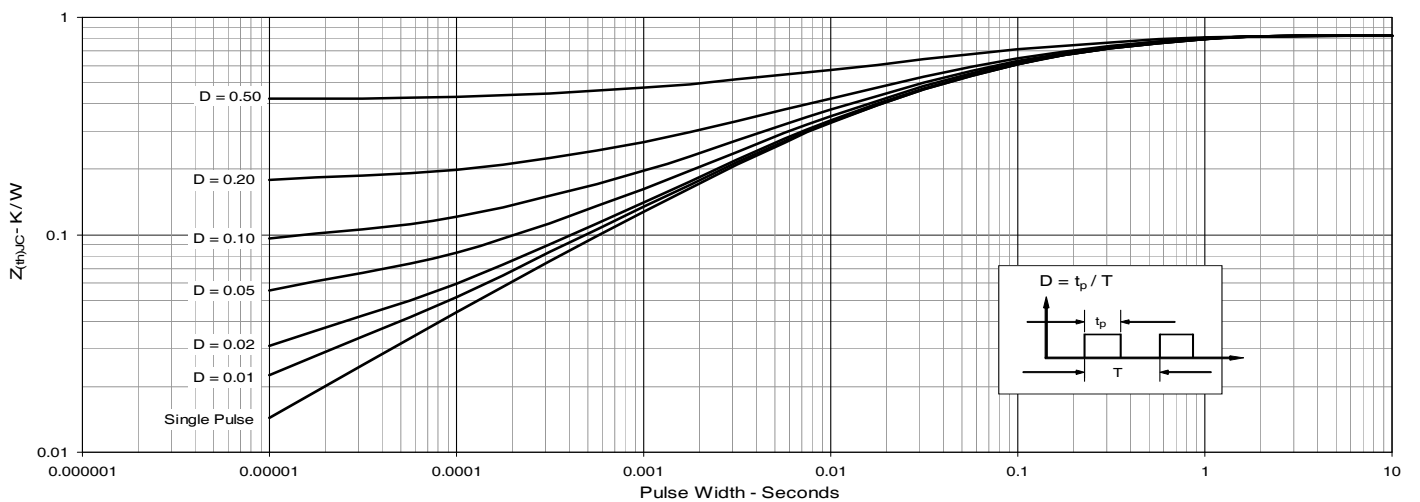


Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

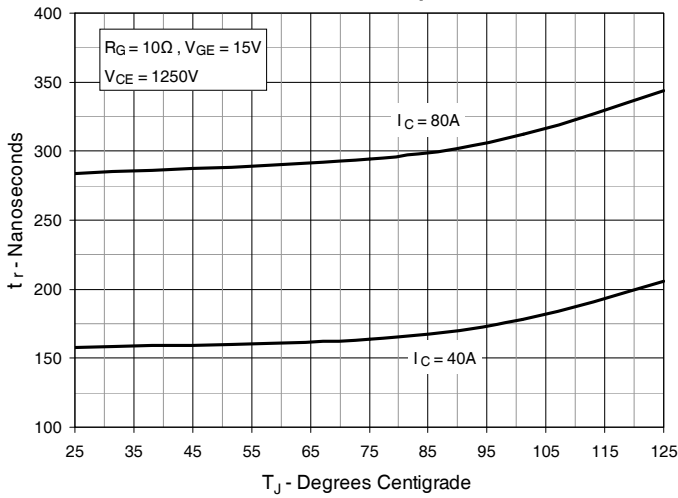


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

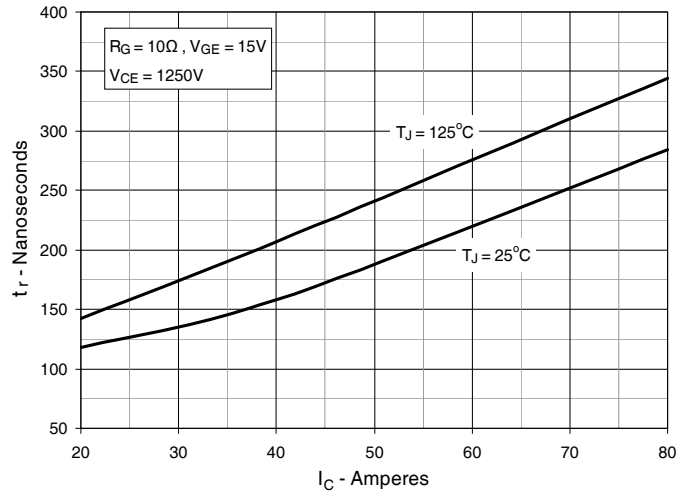


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

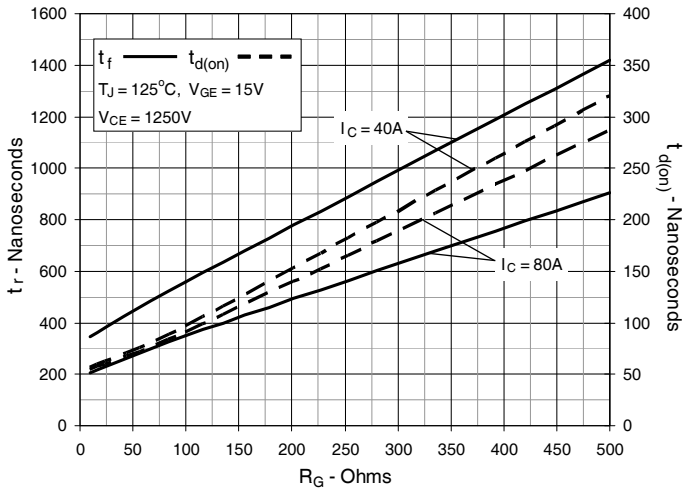


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

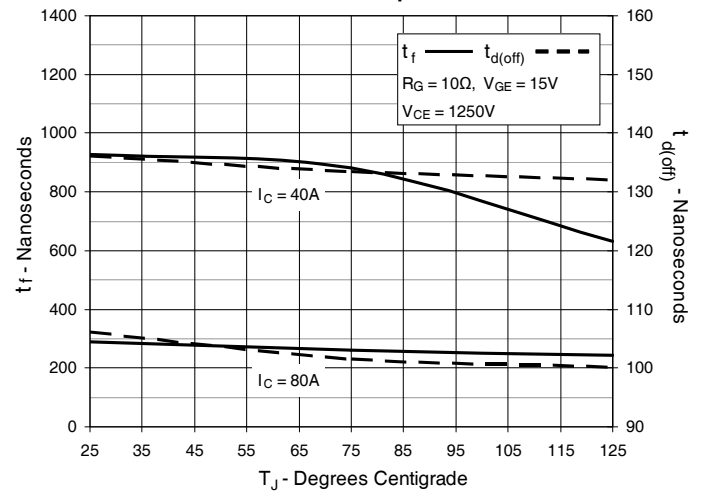


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

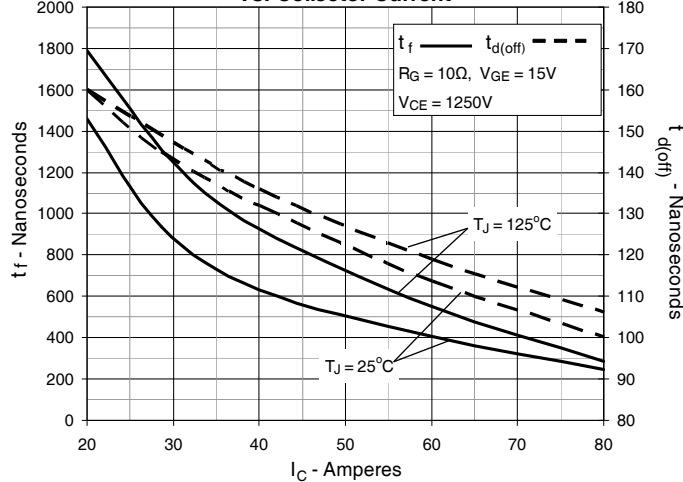
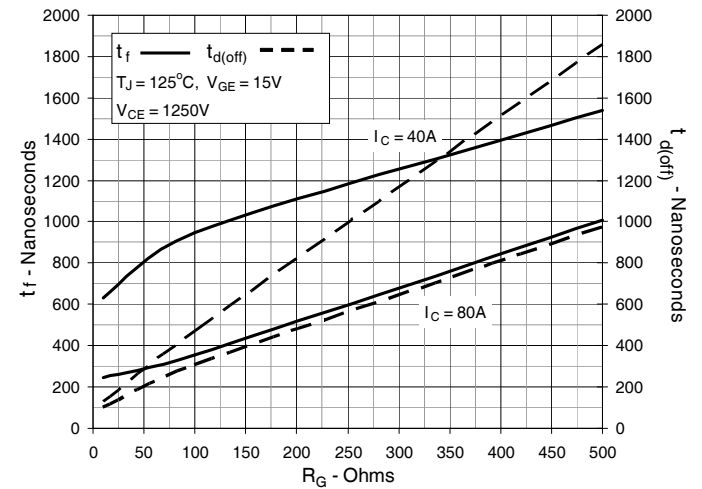


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance





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