IXYS

Power MOSFET ISOPLUS220™

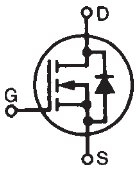
IXKC 25N80C

V_{DSS} = 800 V
I_{D25} = 20 A
$R_{DS(on)}$ = 150 mΩ

Electrically Isolated Back Surface

Low $R_{DS(on)}$, High Voltage, CoolMOS™ Superjunction MOSFET

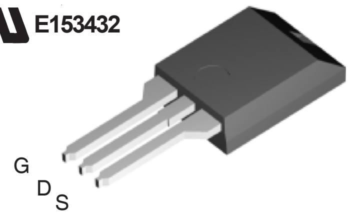
Preliminary Data Sheet



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	800	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	20	A
I_{D90}	T_C = 90°C	14	A
$I_{D(RMS)}$	Package lead current limit	45	A
E_{AS}	I_o = 10A, T_C = 25°C	690	mJ
E_{AR}	I_o = 20A	0.5	mJ
dv/dt	V_{DS} < V_{DSS}, I_F ≤ 17 A, T_{VJ} = 150°C d_{IR}/dt = 100 A/µs	6	V/ns
P_D	T_C = 25°C	140	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +125	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	RMS leads-to-tab, 50/60 Hz, t = 1 minute	2500	V~
F_C	Mounting force	11 ... 65 / 2.4 ...11	N/lb
Weight		3	g

ISOPLUS220™

E153432



G = Gate, D = Drain,
S = Source

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
$R_{DS(on)}$	V_{GS} = 10 V, I_D = I_{D90}, Note 1			136	150	mΩ
	V_{GS} = 10 V, I_D = I_{D90}, Note 1	T_J = 125°C		280		mΩ
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 2 mA		2		4	V
I_{DSS}	V_{DS} = V_{DSS}	T_J = 25°C			50	µA
	V_{GS} = 0 V	T_J = 125°C		10		µA
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±200	nA

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- 3RD generation CoolMos power MOSFET
  - High blocking capability
  - Low on resistance
  - Avalanche rated for unclamped inductive switching (UIS)
- Low thermal resistance due to reduced chip thickness
- Low drain to tab capacitance(<30pF)

Applications

- Switched Mode Power Supplies (SMPS)
- Uninterruptible Power Supplies (UPS)
- Power Factor Correction (PFC)
- Welding
- Inductive Heating

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density

CoolMos is a trademark of Infineon Technology.

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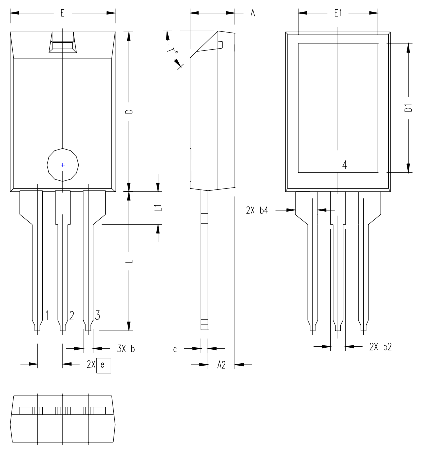
Symbol	Test Conditions	Characteristic Values ($T_J = 25°C$, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 15 V; $I_D = 0.5 \cdot I_{D90}$, pulse test	14	20		S
C_{iss}			4600		pF
C_{oss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2500		pF
C_{rss}			120		pF
$Q_{g(on)}$			180		nC
Q_{gs}	V_{GS} = 10 V, V_{DS} = 640 V, $I_D = I_{D90}$		20		nC
Q_{gd}			80		nC
$t_{d(on)}$			25		ns
t_r	V_{GS} = 10 V, V_{DS} = 640V		25		ns
$t_{d(off)}$	I_D = 35 A, R_G = 2.2 Ω		75		ns
t_f			10		ns
R_{thJC}				0.9	K/W
R_{thCH}			0.30		K/W

Reverse Conduction

Symbol	Test Conditions	Characteristic Values ($T_J = 25°C$, unless otherwise specified) min.	typ.	max.	
V_{SD}	I_F = 12.5 A, V_{GS} = 0 V Note 1		1	1.2	V

Note: 1. Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %

ISOPLUS220 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T°			42.5°	47.5°

NOTE:
1. Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

Fig. 1. Output Characteristics @ 25°C

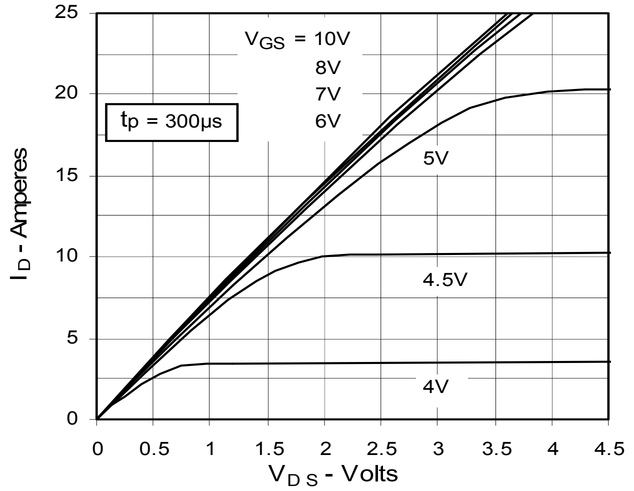


Fig. 2. Extended Output Characteristics @ 25°C

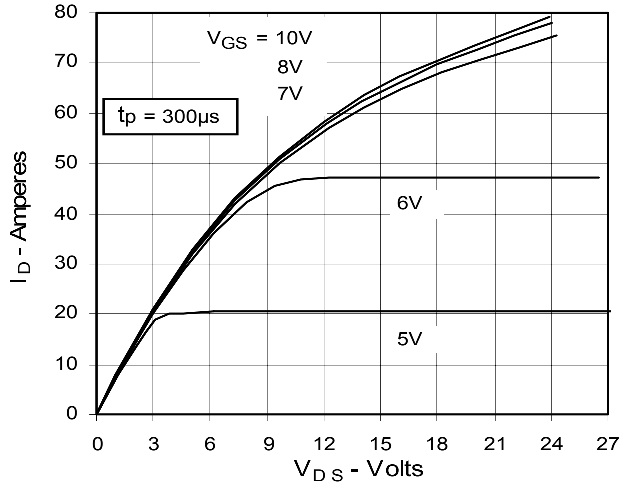


Fig. 3. Output Characteristics @ 125°C

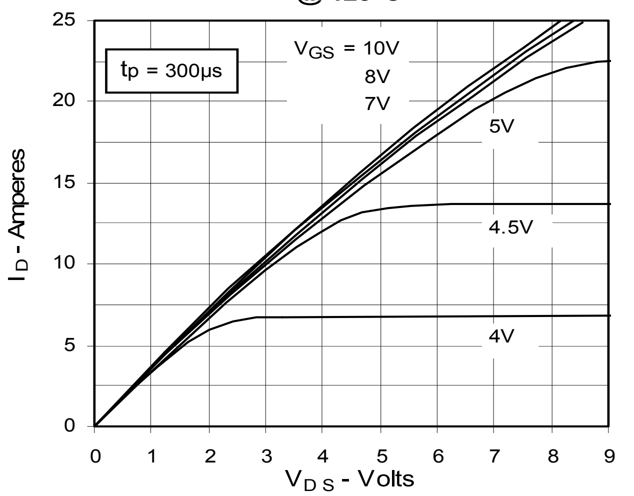


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D90} Value vs. Junction Temperature

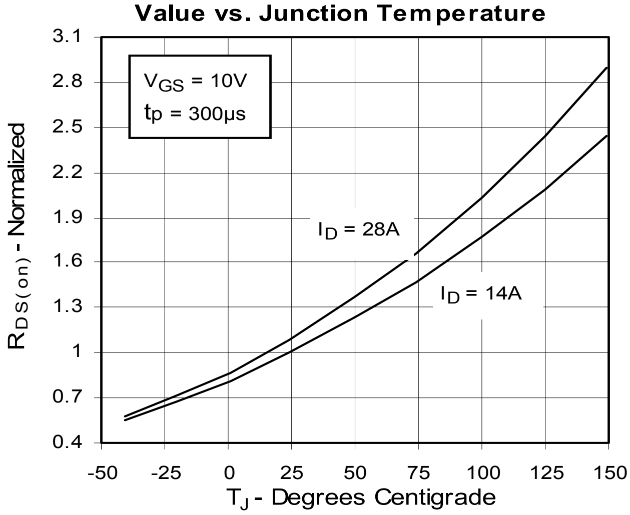


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D90} Value vs. I_D

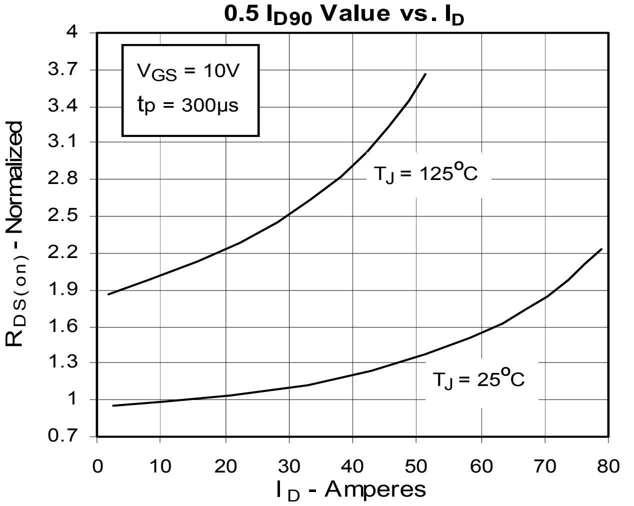


Fig. 6. Drain Current vs. Case Temperature

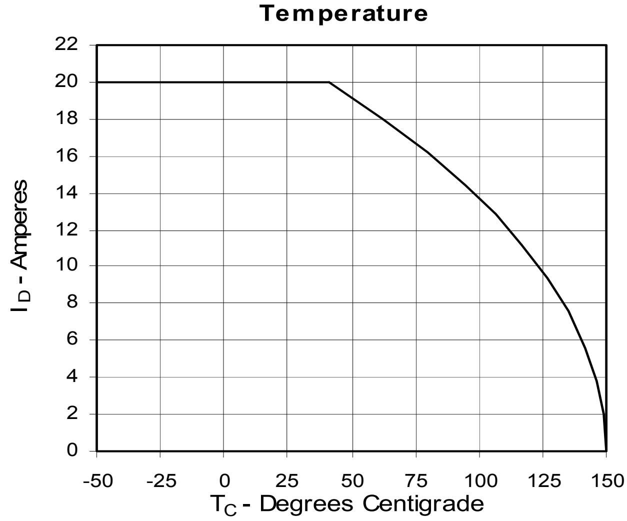


Fig. 7. Input Admittance

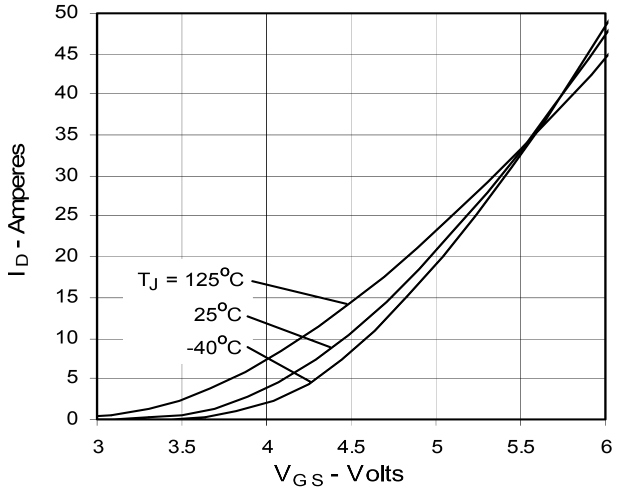


Fig. 8. Transconductance

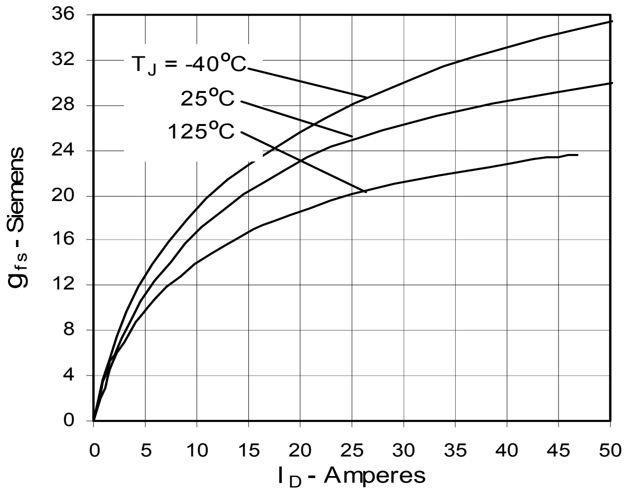


Fig. 9. Source Current vs. Source-To-Drain Voltage

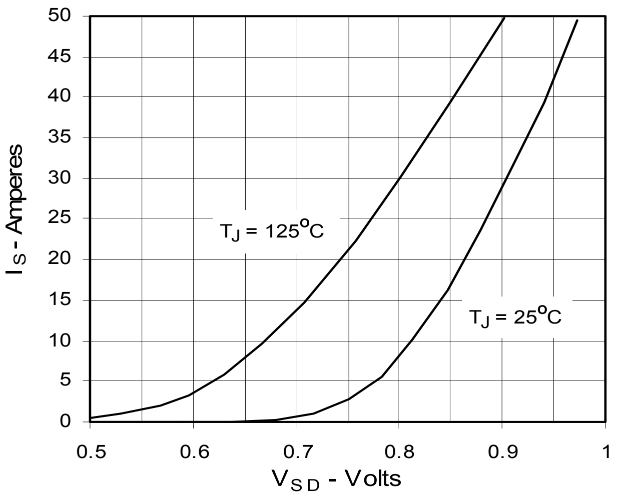


Fig. 10. Gate Charge

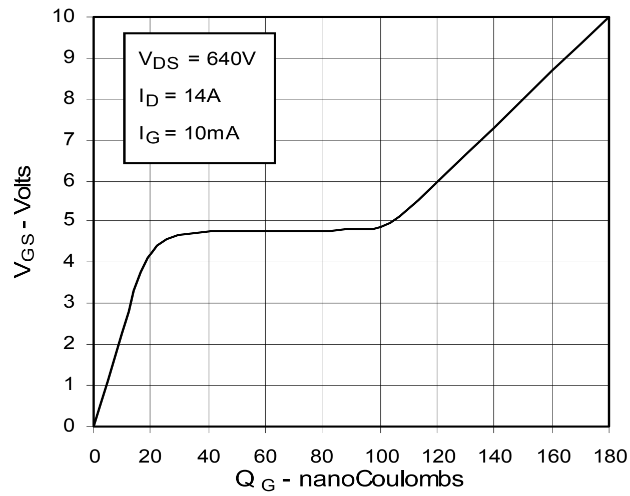


Fig. 11. Capacitance

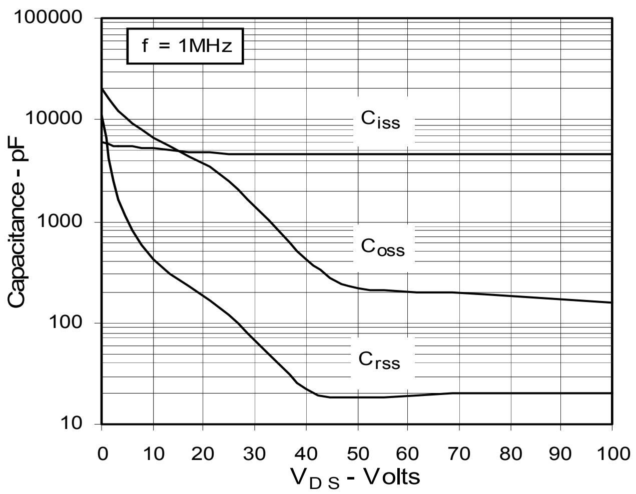
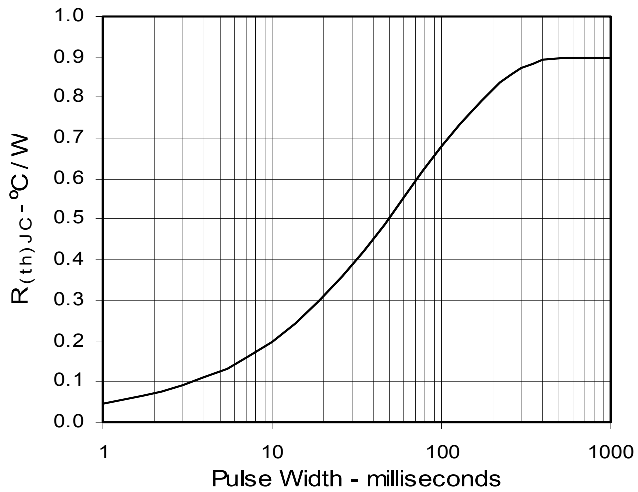


Fig. 12. Maximum Transient Thermal Resistance



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343 6,583,505 4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1 6,683,344